

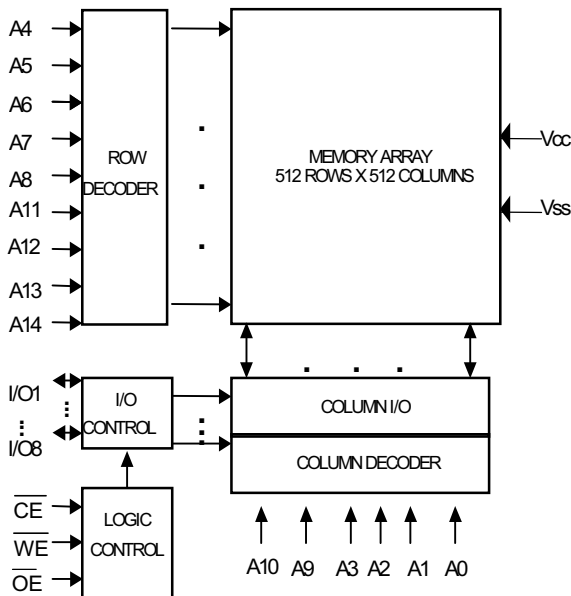


FEATURES

- Fast access time : 10/12/15 ns (max.)
- Low operating power consumption : 60 mA (typical)
- Single 3.3V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Three state outputs
- Package : 28-pin 300 mil SOJ
28-pin 8mm×13.4mm

STSOP

FUNCTIONAL BLOCK DIAGRAM



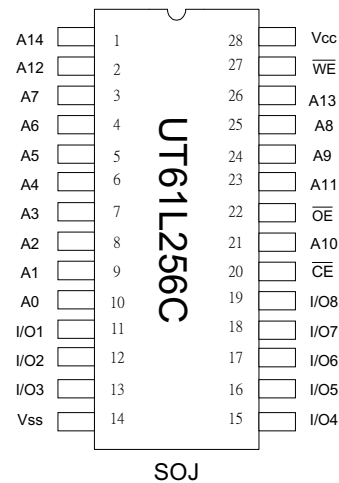
GENERAL DESCRIPTION

The UT61L256C is a 262,144-bit high-speed CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using high performance, high reliability CMOS technology.

The UT61L256C is designed for high-speed system applications. It is particularly suited for use in high-speed system applications.

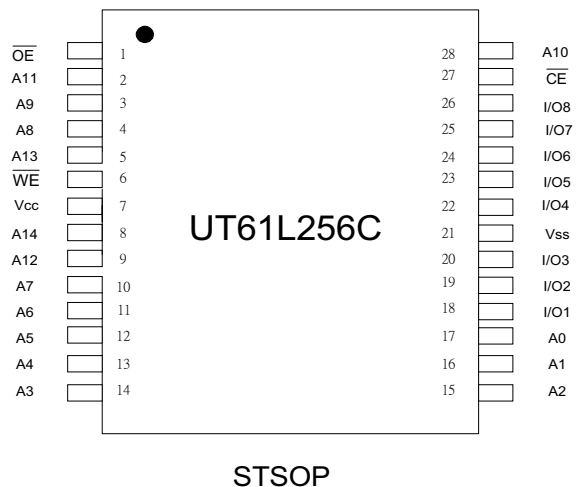
The UT61L256C operates from a single 3.3V power supply and all inputs and outputs are fully TTL compatible.

PIN CONFIGURATION



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
I/O1 - I/O8	Data Inputs/Outputs
\overline{CE}	Chip Enable Input
\overline{WE}	Write Enable Input
\overline{OE}	Output Enable Input
V _{CC}	Power Supply
V _{SS}	Ground



**ABSOLUTE MAXIMUM RATINGS***

PARAMETER	SYMBOL	RATING	UNIT
Terminal Voltage with Respect to V _{SS}	V _{TERM}	-0.5 to +4.5	V
Operating Temperature	T _A	0 to +70	°C
Storage Temperature	T _{STG}	-65 to +150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA
Soldering Temperature (under 10 sec)	T _{solder}	260	°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	\overline{CE}	\overline{OE}	\overline{WE}	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High - Z	I _{SB} , I _{SB1}
Output Disable	L	H	H	High - Z	I _{CC}
Read	L	L	H	D _{OUT}	I _{CC}
Write	L	X	L	D _{IN}	I _{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 3.1V~3.6V , T_A = 0°C to 70°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	MAX.	UNIT	
Input High Voltage	V _{IH}		2	-	V	
Input Low Voltage	V _{IL}		-	0.8	V	
Input Leakage Current	I _{LI}	V _{SS} ≤ V _{IN} ≤ V _{CC}	- 1	1	μA	
Output Leakage Current	I _{LO}	V _{SS} ≤ V _{I/O} ≤ V _{CC} $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$	- 1	1	μA	
Output High Voltage	V _{OH}	I _{OH} = - 4mA	2.0	-	V	
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	0.4	V	
Operating Power Supply Current	I _{CC}	$\overline{CE} = V_{IL}$, I _{I/O} = 0mA Cycle=Min.	- 10	-	75	mA
			- 12	-	60	mA
			- 15	-	50	mA
Standby Power Supply Current	I _{SB}	$\overline{CE} = V_{IH}$	-	15	mA	
	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$	-	3	mA	

**CAPACITANCE** ($T_A=25^{\circ}\text{C}$, $f=1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L=30\text{pF}$, $I_{OH}/I_{OL}=-4\text{mA}/8\text{mA}$

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 3.1\text{V}\sim 3.6\text{V}$, $T_A = 0^{\circ}\text{C}$ to 70°C)**(1) READ CYCLE**

PARAMETER	SYMBOL	UT61L256C-10		UT61L256C-12		UT61L256C-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	12	-	15	-	ns
Address Access Time	t_{AA}	-	10	-	12	-	15	ns
Chip Enable Access Time	t_{ACE}	-	10	-	12	-	15	ns
Output Enable Access Time	t_{OE}	-	5	-	6	-	7	ns
Chip Enable to Output in Low Z	t_{CLZ}^*	2	-	3	-	4	-	ns
Output Enable to Output in Low Z	t_{OLZ}^*	0	-	0	-	0	-	ns
Chip Disable to Output in High Z	t_{CHZ}^*	-	5	-	6	-	7	ns
Output Disable to Output in High Z	t_{OHZ}^*	-	5	-	6	-	7	ns
Output Hold from Address Change	t_{OH}	1	-	3	-	3	-	ns

(2) WRITE CYCLE

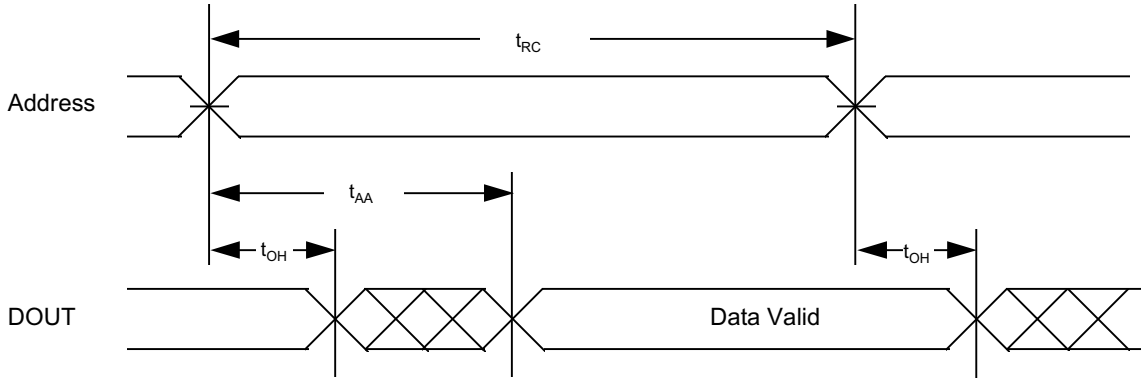
PARAMETER	SYMBOL	UT61L256C-10		UT61L256C-12		UT61L256C-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	12	-	15	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	12	-	ns
Chip Enable to End of Write	t_{CW}	8	-	10	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	8	-	9	-	10	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}^*	2	-	3	-	4	-	ns
Write to Output in High Z	t_{WHZ}^*	-	1	-	7	-	8	ns

*These parameters are guaranteed by device characterization, but not production tested.

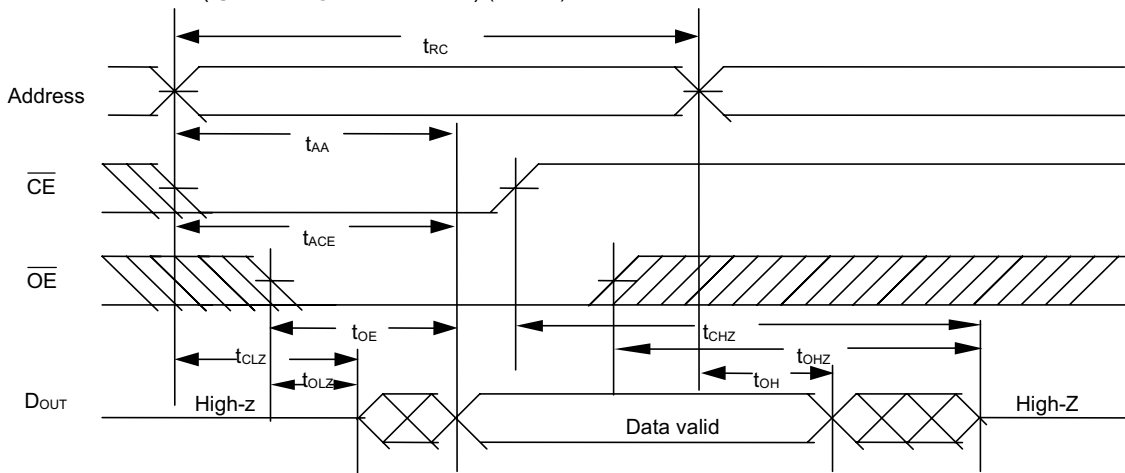


TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2,4)



READ CYCLE 2 (\overline{CE} and \overline{OE} Controlled) (1,3,5,6)

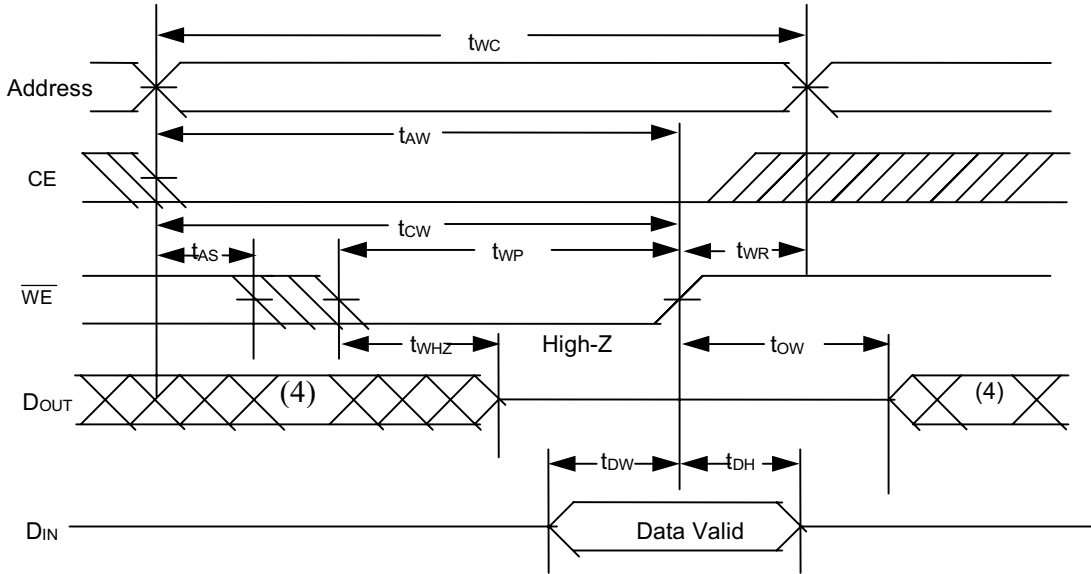


Notes :

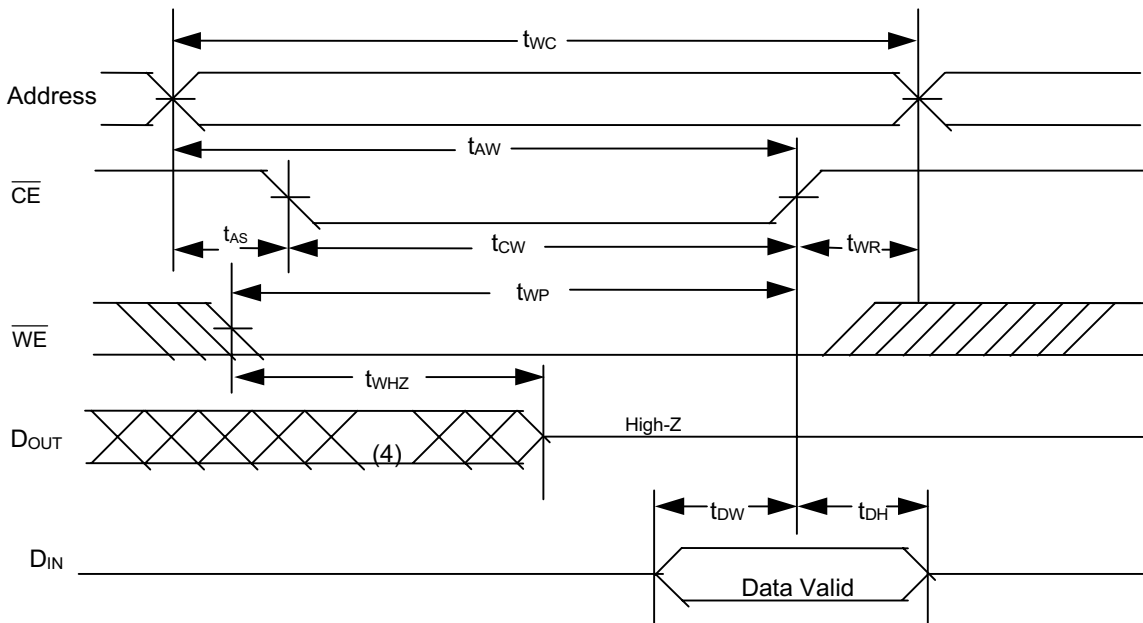
1. \overline{WE} is HIGH for read cycle.
2. Device is continuously selected $\overline{CE} = V_{IL}$.
3. Address must be valid prior to or coincident with \overline{CE} transition; otherwise t_{AA} is the limiting parameter.
4. \overline{OE} is LOW.
5. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.
6. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .



WRITE CYCLE 1 (\overline{WE} Controlled) (1,2,3,5)



WRITE CYCLE 2 (\overline{CE} Controlled) (1,2,5)



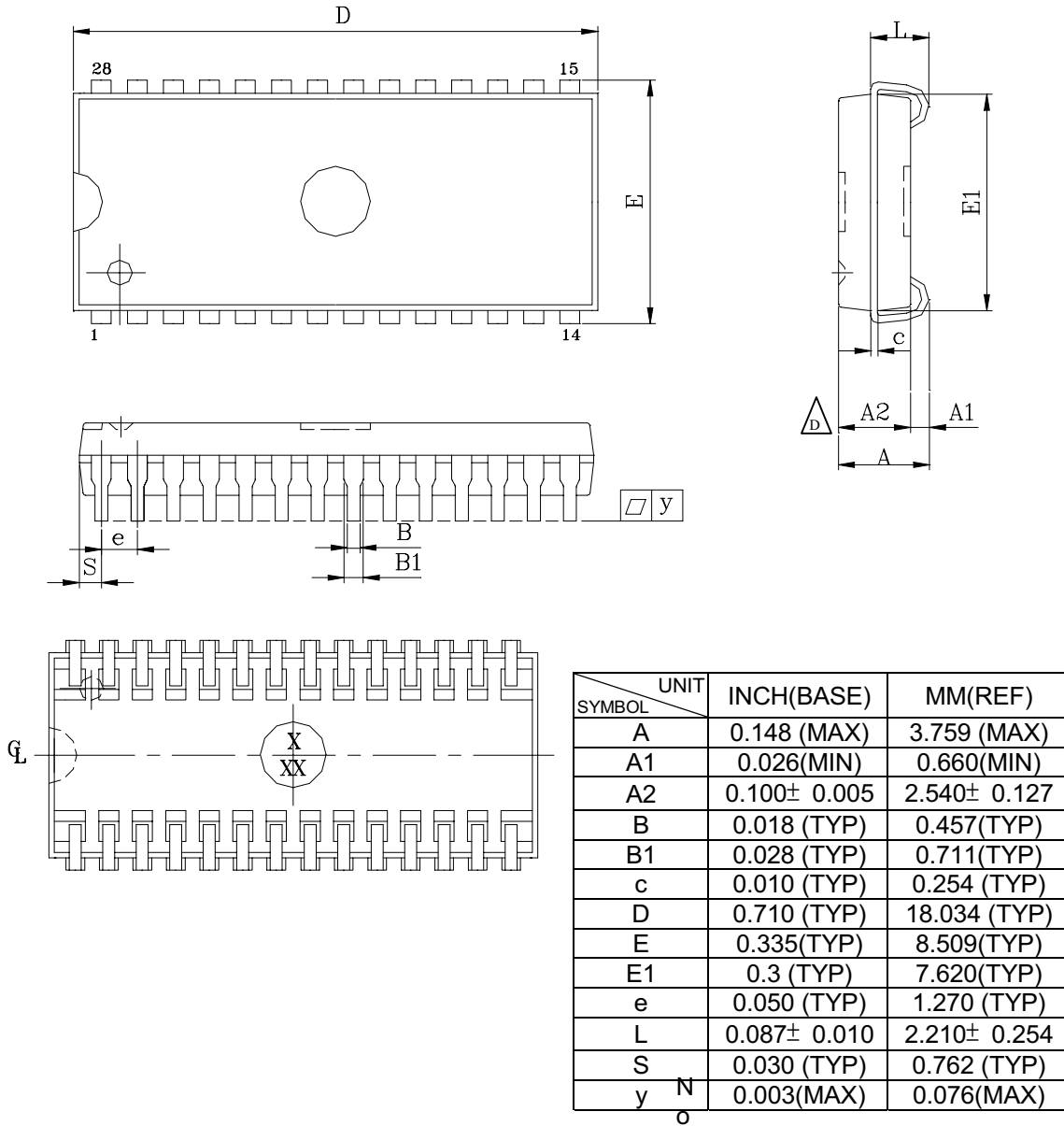
Notes :

1. \overline{WE} or \overline{CE} must be HIGH during all address transitions.
2. A write occurs during the overlap of a low \overline{CE} and a low \overline{WE} .
3. During a \overline{WE} controlled with write cycle with \overline{OE} LOW, t_{wp} must be greater than $t_{whz}+t_{dw}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the \overline{CE} LOW transition occurs simultaneously with or after \overline{WE} LOW transition, the outputs remain in a high impedance state.
6. t_{ow} and t_{whz} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.



PACKAGE OUTLINE DIMENSION

28 pin 300 mil SOJ Package Outline Dimension

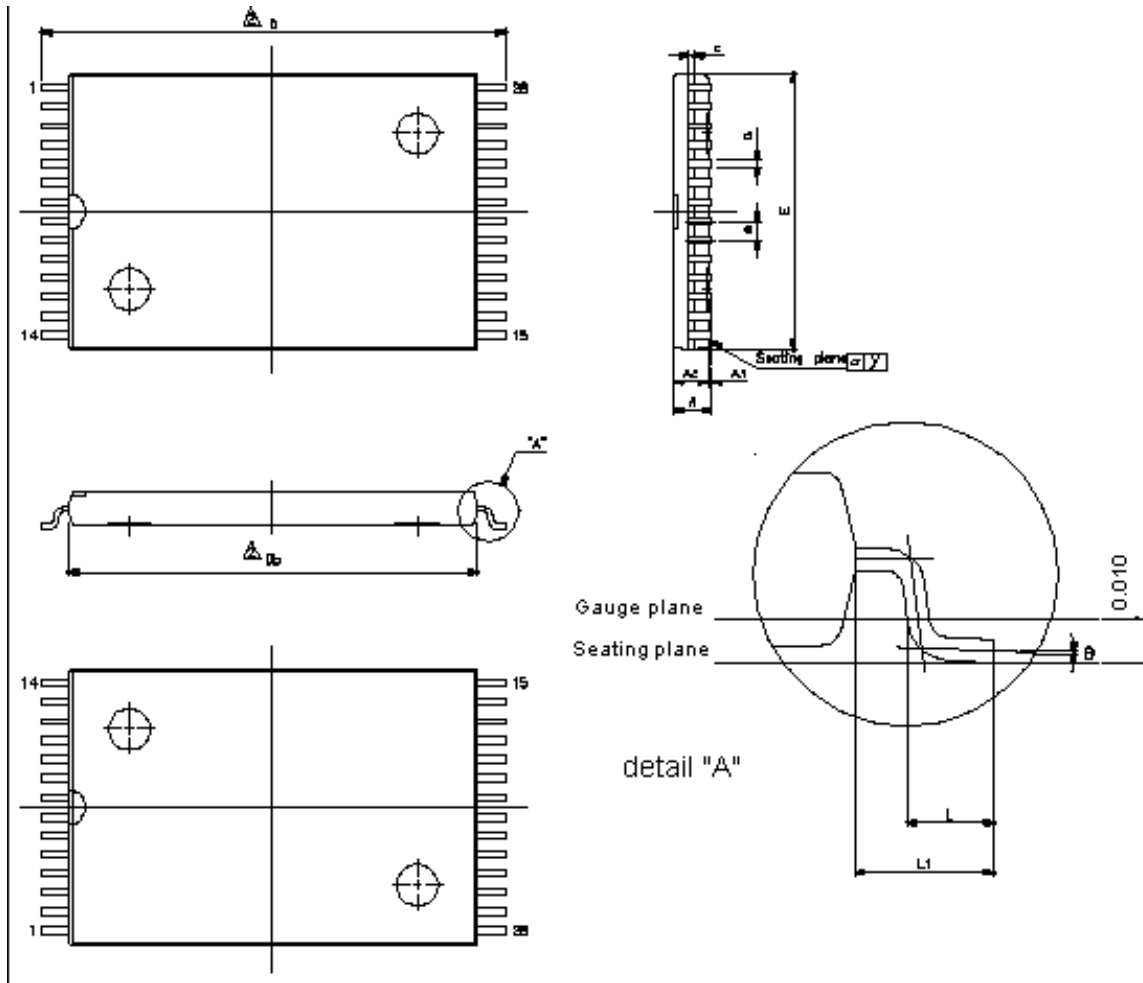


note:

1. S/E/D DIM. NOT INCLUDING MOLD FLASH.
2. THE END FLASH IN PACKAGE LENGTHWISE IS NOT MORE THAN 10 MILS EACH SIDE.



28 pin 8mmx13.4mm STSOP Package Outline Dimension



Note :
 E dimension is not including end flash
 The total of both sides' end flash is
 Not above 0.3mm.



UNIT SYMBOL	INCH(BASE)	MM(REF)
A	0.047 (MAX)	1.20 (MAX)
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.006 (TYP)	0.15(TYP)
c	0.010 (TYP)	0.254(TYP)
Db	0.465± 0.004	11.80± 0.10
E	0.315± 0.004	8.00± 0.10
e	0.022 (TYP)	0.55(TYP)
D	0.528± 0.008	13.40± 0.20
L	0.020± 0.004	0.50± 0.10
L1	0.0315± 0.004	0.80± 0.10
y	0.08(MAX)	0.003(MAX)
θ	0°~5°	0°~5°



UTRON

Rev. 1.0

UT61L256C

32K X 8 BIT HIGH SPEED CMOS SRAM

ORDERING INFORMATION

PART NO.	ACCESS TIME (ns)	PACKAGE
UT61L256CJC-10	10	28PIN SOJ
UT61L256CJC-12	12	28PIN SOJ
UT61L256CJC-15	15	28PIN SOJ
UT61L256CLS-10	10	28PIN STSOP
UT61L256CLS-12	12	28PIN STSOP
UT61L256CLS-15	15	28PIN STSOP



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32K X 8 BIT HIGH SPEED CMOS SRAM

REVISION HISTORY

REVISION	DESCRIPTION	DATE
Preliminary Rev. 0.1	Original	May 4,2001
Rev. 1.0	Sample ready and release	Jul 13,2001



UTRON

Rev. 1.0

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32K X 8 BIT HIGH SPEED CMOS SRAM

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