AN3338
Application note

SLLIMM™
small low-loss intelligent molded module

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Introduction

In recent years the variable speed motor control market has required high performance solutions able to satisfy the increasing energy saving requirements, compactness, reliability, and system costs in home appliances, such as washing machines, dish washers, refrigerators, air conditioning compressor drives, and in low power industrial applications, such as sewing machines, pumps, tools, etc. To meet these market needs, STMicroelectronics has developed a new family of compact, high efficiency, dual-in-line intelligent power modules, with optional extra features, called small low-loss intelligent molded module (SLLIMM™).

The SLLIMM product family combines optimized silicon chips, integrated in three main inverter blocks:

- power stage
  - six short-circuit rugged IGBTs
  - six freewheeling diodes
- driving network
  - three high voltage gate drivers
  - discrete gate resistors
  - three bootstrap diodes
- protection and optional features
  - op amps for advanced current sensing
  - comparators for fault protection against overcurrent and short-circuit
  - NTC sensor for temperature control
  - smart shutdown function
  - dead time, interlocking function and undervoltage lockout.

Thanks to the state of art DBC mounting technology, the fully isolated SLLIMM package (SDIP) offers extremely low thermal resistance with optimum cost-effectiveness and quality level.

Compared to discrete-based inverters, including power devices, and driver and protection circuits, the SLLIMM family provides a high integrated level that means simplified circuit design, reduced component count, smaller weight, and high reliability.

The aim of this application note is to provide a detailed description of SLLIMM products, providing guidelines to motor drive designers for an efficient, reliable, and fast design when using the new ST SLLIMM family.

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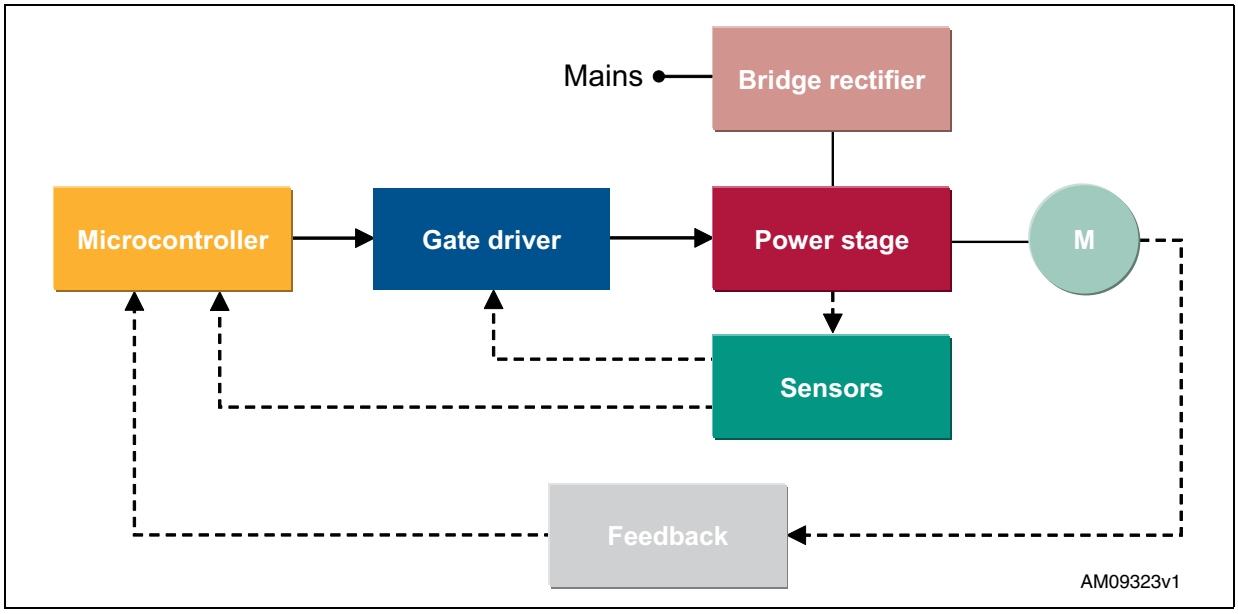
1 Inverter design concept and SLLIMM solution

Motor drive applications, ranging from a few tens of watts to mega watts, are mainly based on the inverter concept thanks to the fact that this solution can meet efficiency, reliability, size, and cost constraints required in a number of markets.

As shown in *Figure 1*, an inverter for motor drive applications is basically composed of a power stage, mainly based on IGBTs and freewheeling diodes; a driving stage, based on high voltage gate drivers; a control unit, based on microcontrollers or DSPs; some optional sensors for protections and feedback signals for controls.

The approach of this solution with discrete devices produces high manufacturing costs associated with high reliability risks, bigger size and higher weight, a considerable number of components and the significant stray inductances and dispersions in the board layout.

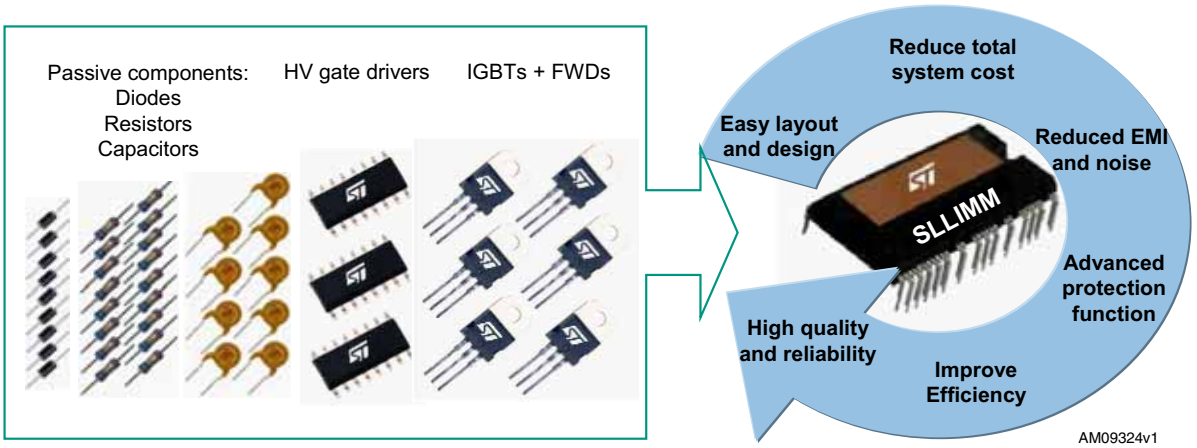
Figure 1. Inverter motor drive block diagram



In recent years, the use of intelligent power modules has rapidly increased thanks to the benefits of greater integration levels. The new ST SLLIMM family is able to replace more than 30 discrete devices in a single package. *Figure 2* shows a comparison between a discrete-based inverter and the SLLIMM solution, the advantages of SLLIMM can be easily understood and can be summarized in a significantly improved design time, reduced manufacturing efforts, higher flexibility in a wide range of applications, and increased reliability and quality level.

In addition, the optimized silicon chips in both control and power stages and the optimized board layout provide maximized efficiency, reduced EMI and noise generation, higher levels of protection, and lower propagation delay time.

Figure 2. Discrete-based inverter vs. SLLIMM solution comparison



1.1 Product synopsis

The SLLIMM family has been designed to satisfy the requirements of a wide range of final applications in the range of 300 W - 2.0 kW, such as:

- washing machines
- dish washers
- refrigerators
- air conditioning compressor drives
- sewing machines
- pumps
- tools
- low power industrial applications

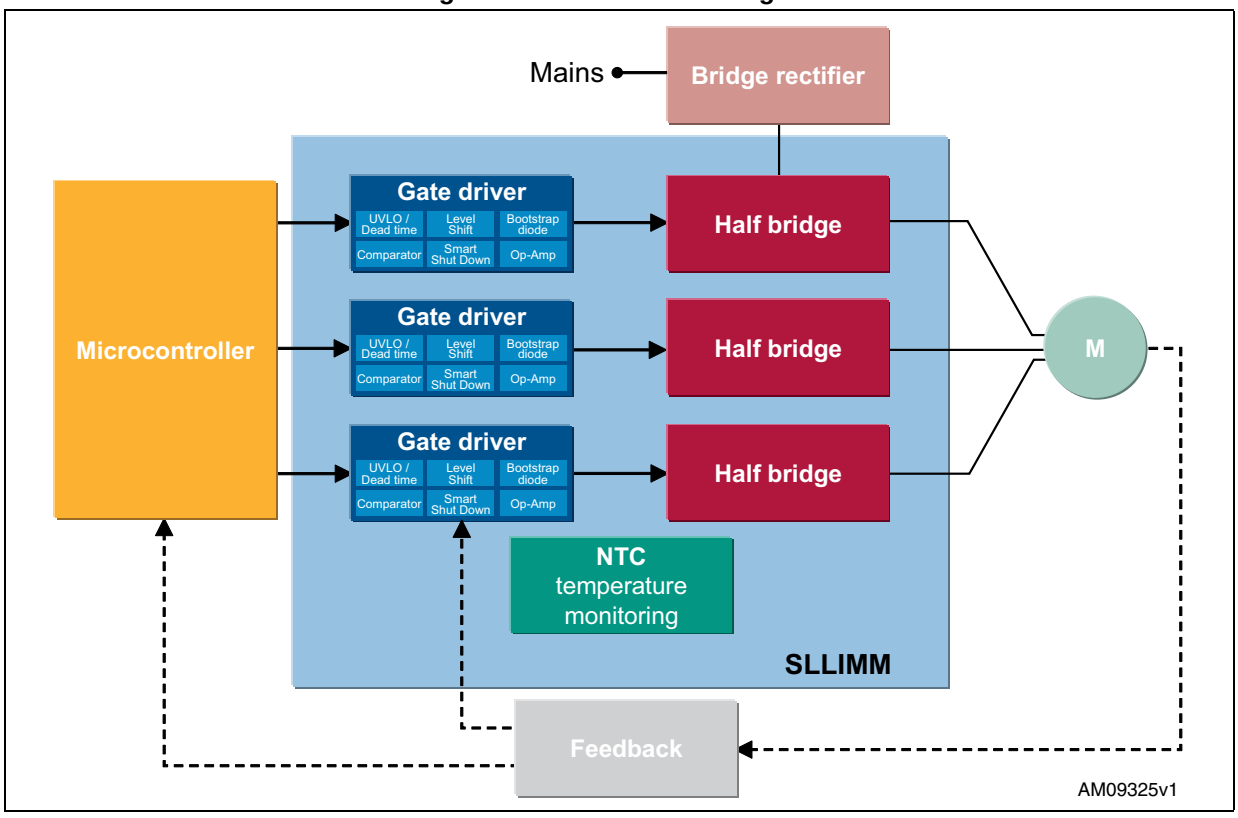
The main features and integrated functions can be summarized as follows:

- 600 V, 10 - 30 A ratings
- 3-phase IGBT inverter bridge including:
  - six low-loss and short-circuit protected IGBTs
  - six low forward voltage drop and soft recovery freewheeling diodes
- three control ICs for gate driving and protection including:
  - smart shutdown function
  - comparator for fault protection against overcurrent and short-circuit
  - op amps for advanced current sensing
  - three integrated bootstrap diodes
  - interlocking function
  - undervoltage lockout

- NTC thermistor for temperature monitor
- open emitter configuration for individual phase current sensing
- DBC fully isolated package for enhanced thermal behavior
- isolation voltage rating of 2500 V_{RMS}
- several passive components for IGBT switching speed optimum setting
- gate driver proper biasing and noise filtering.

Figure 3 shows the block diagram of SLLIMM included in the inverter solution

Figure 3. SLLIMM block diagram



The power devices (IGBTs and freewheeling diodes), incorporated in the half bridge block, are tailored for a motor drive application delivering the greatest overall efficiency, thanks to the optimized trade-off between conduction and switching power losses and very low EMI generation, as a result of reduced dV/dt and di/dt.

The IC gate drivers have been selected in order to meet two levels of functionality giving the designers more freedom to choose: a basic version which includes the essential features for a cost-effective solution and a fully featured version which provides advanced options for a sophisticated control method.

The fully isolated SDIP package is available in a 25-lead version (SDIP-25L) and 38-lead version (SDIP-38L) and offers excellent heat dissipation characteristics, thanks to the state of the art DBC mounting technology, ensuring at the same time, very high voltage isolation rating (2500 V_{RMS}), compact size and high reliability.

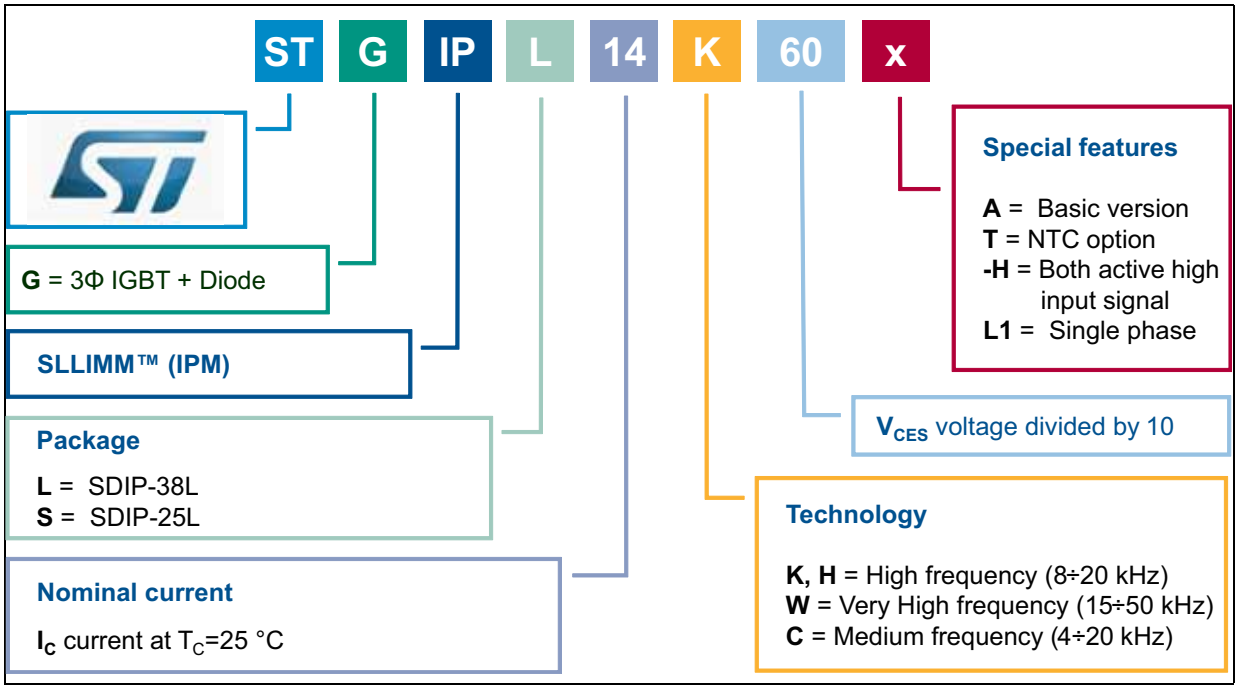
1.2 Product line-up and nomenclature

Table 1. SLLIMM line-up(1)

Features	Basic version	Fully featured version			
	STGIPS10K60A	STGIPS14K60	STGIPL14K60	STGIPS20K60	STGIPL20K60
Voltage (V)	600	600	600	600	600
Current @ T_C=25 °C (A)	10	14	15	18	20
R_{thJC} max. single IGBT (°C/W)	3.8	3	2.8	2.4	2.2
Package type	SDIP-25L	SDIP-25L	SDIP-38L	SDIP-25L	SDIP-38L
Package size (mm) X, Y, Z	44.4x22.0x5.4	44.4x22.0x5.4	49.6x24.5x5.4	44.4x22.0x5.4	49.6x24.5x5.4
DBC substrate	Yes	Yes	Yes	Yes	Yes
NTC	Yes	No	Yes	No	Yes
Integrated bootstrap diode	Yes	Yes	Yes	Yes	Yes
SD function	No	Yes	Yes	Yes	Yes
Comparator for fault protection	No	Yes (1 pin)	Yes (3 pins)	Yes (1 pin)	Yes (3 pins)
Smart shutdown function	No	Yes	Yes	Yes	Yes
Op amps for advanced current sensing	No	No	Yes	No	Yes
Interlocking function	Yes	Yes	Yes	Yes	Yes
Undervoltage lockout	Yes	Yes	Yes	Yes	Yes
Open emitter configuration	Yes (3 pins)	Yes (3 pins)	Yes (3 pins)	Yes (3 pins)	Yes (3 pins)
3.3 / 5 V input interface compatibility	Yes	Yes	Yes	Yes	Yes
High side IGBT input signal	Active High	Active High	Active High	Active High	Active High
Low side IGBT input signal	Active High	Active Low	Active Low	Active Low	Active Low

1. For additional information and the complete product portfolio, refer to www.st.com/modules.

Figure 4. SLLIMM nomenclature



1.3 Internal circuit

Figure 5. Internal circuit of STGIPS10K60A

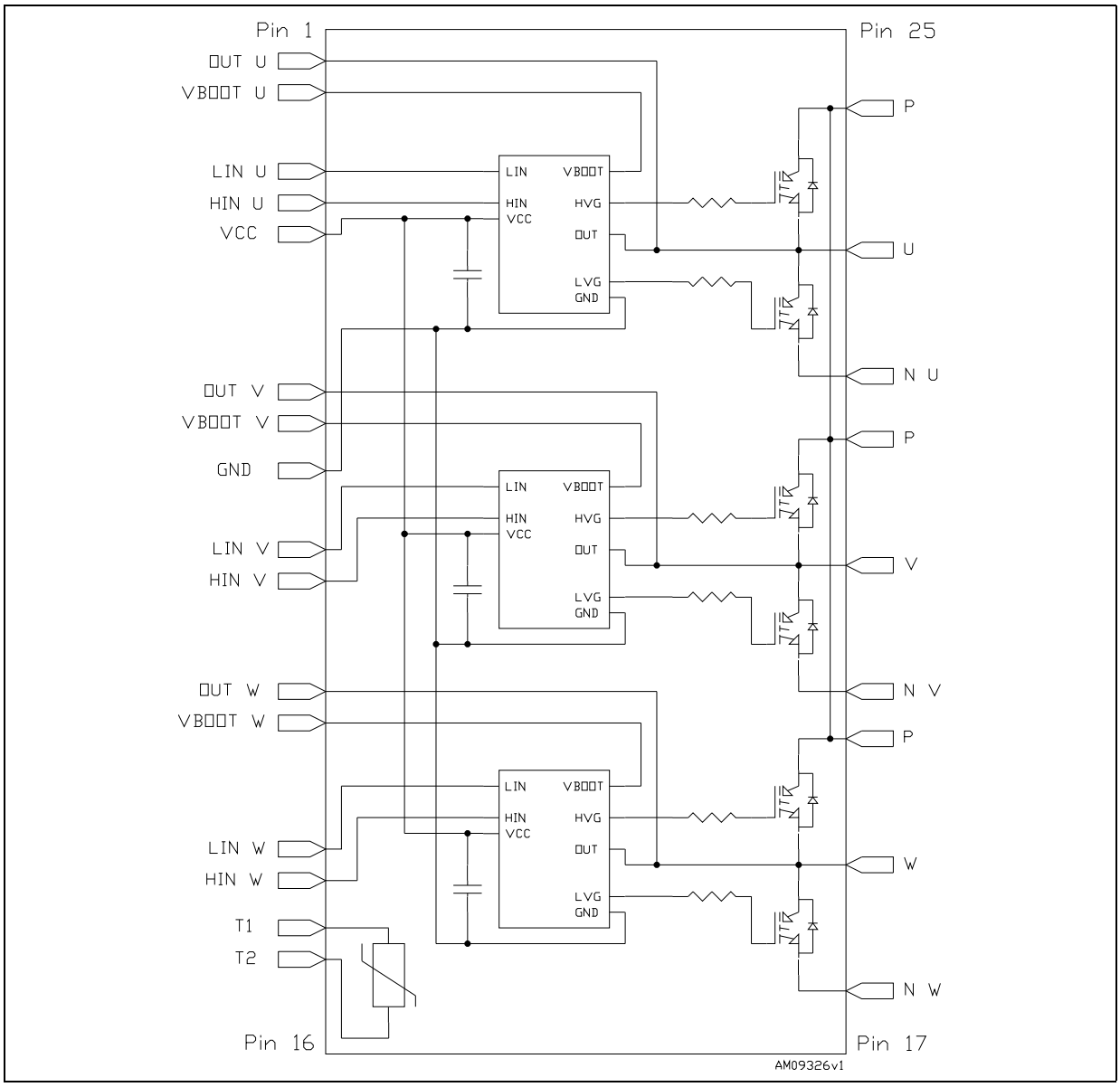


Figure 6. Internal circuit of STGIPS14K60 and STGIPS20K60

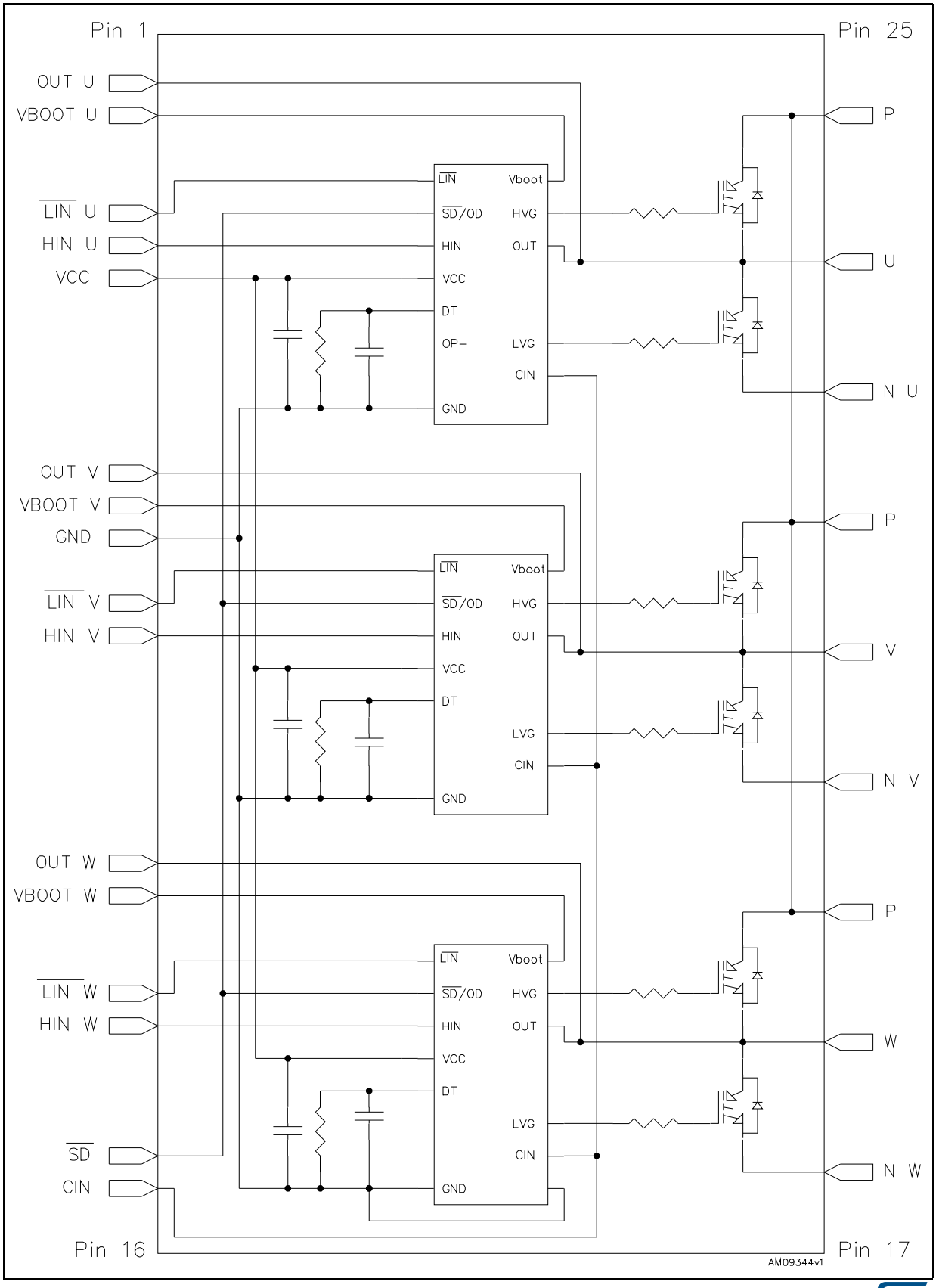
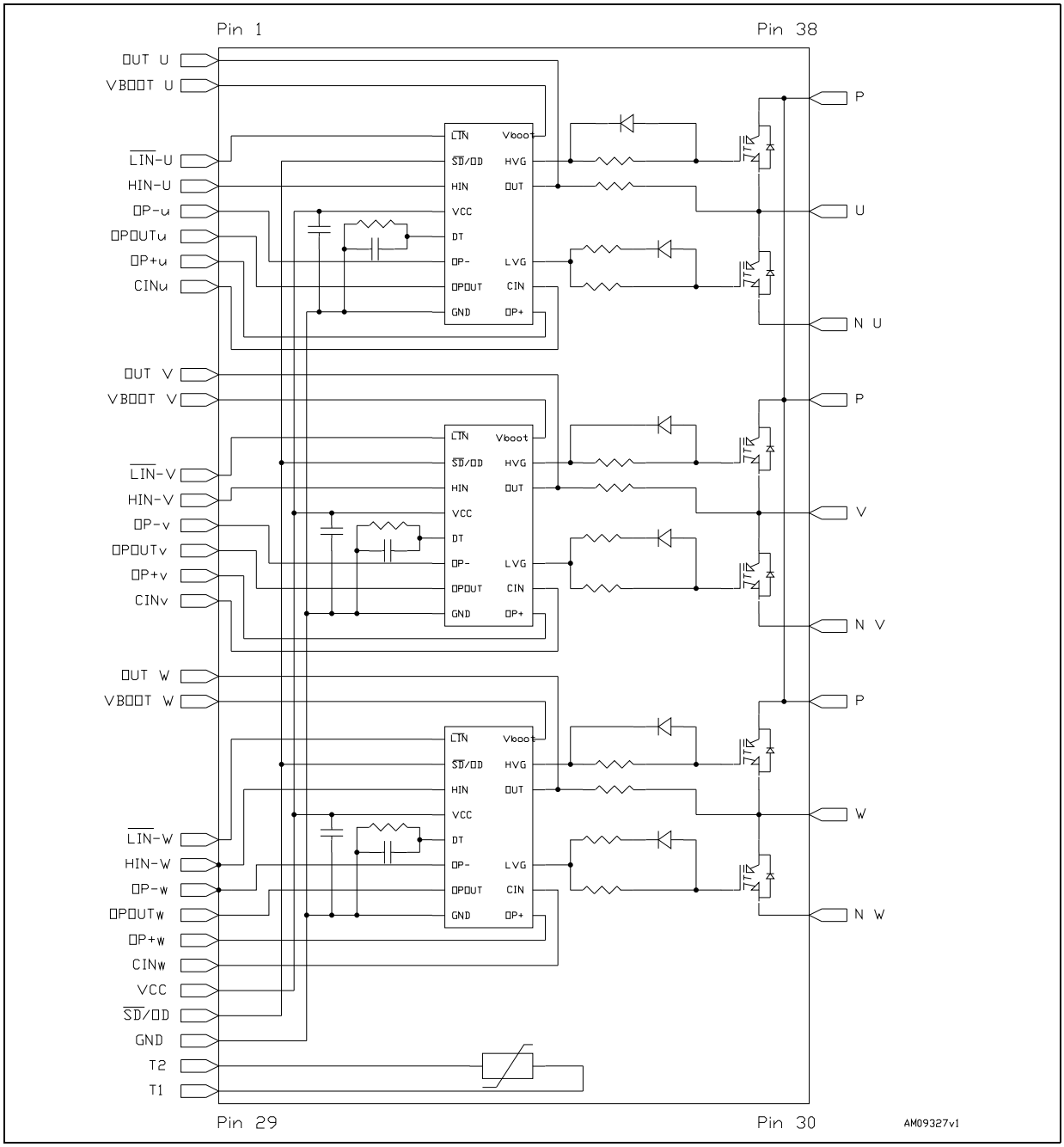


Figure 7. Internal circuit of STGIPL14K60 and STGIPL20K60



1.4 Absolute maximum ratings

The absolute maximum ratings represent the extreme capability of the device and they can be normally used as a worst limit design condition. It is important to note that the absolute maximum value is given according to a set of testing conditions such us temperature, frequency, voltage, and so on. The device performances can change according to the applied condition.

The SLLIMM specifications are described below by using the STGIPL14K60 datasheet as an example. Please refer to the respective product datasheets for a detailed description of other types.

Table 2. Inverter part of STGIPL14K60

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage applied between P-N_U, N_V, N_W	450	V
$V_{PN(surge)}$	Supply voltage (surge) applied between P-N_U, N_V, N_W	500	V
V_{CES}	Collector emitter voltage (V_{IN}(1)=0)	600	V
$\pm I_C$(2)	Each IGBT continuous collector current at T_C=25 °C	15	A
$\pm I_C$(3)	Each IGBT pulsed collector current	30	A
P_{TOT}	Each IGBT total dissipation at T_C=25 °C	44	W
t_{SCW}	Short-circuit withstand time, V_{CE}=0.5· $V_{(BR)CES}$, T_j=125 °C, V_{CC}=V_{boot}=15 V, V_{IN}(1)=0÷5 V	5	µs

1. Applied between HIN_U, HIN_V, HIN_W; $\overline{LIN}_U$, $\overline{LIN}_V$, $\overline{LIN}_W$ and GND.
2. Calculated according to the iterative *Equation 1*.
3. Pulse width limited by max. junction temperature.

Equation 1

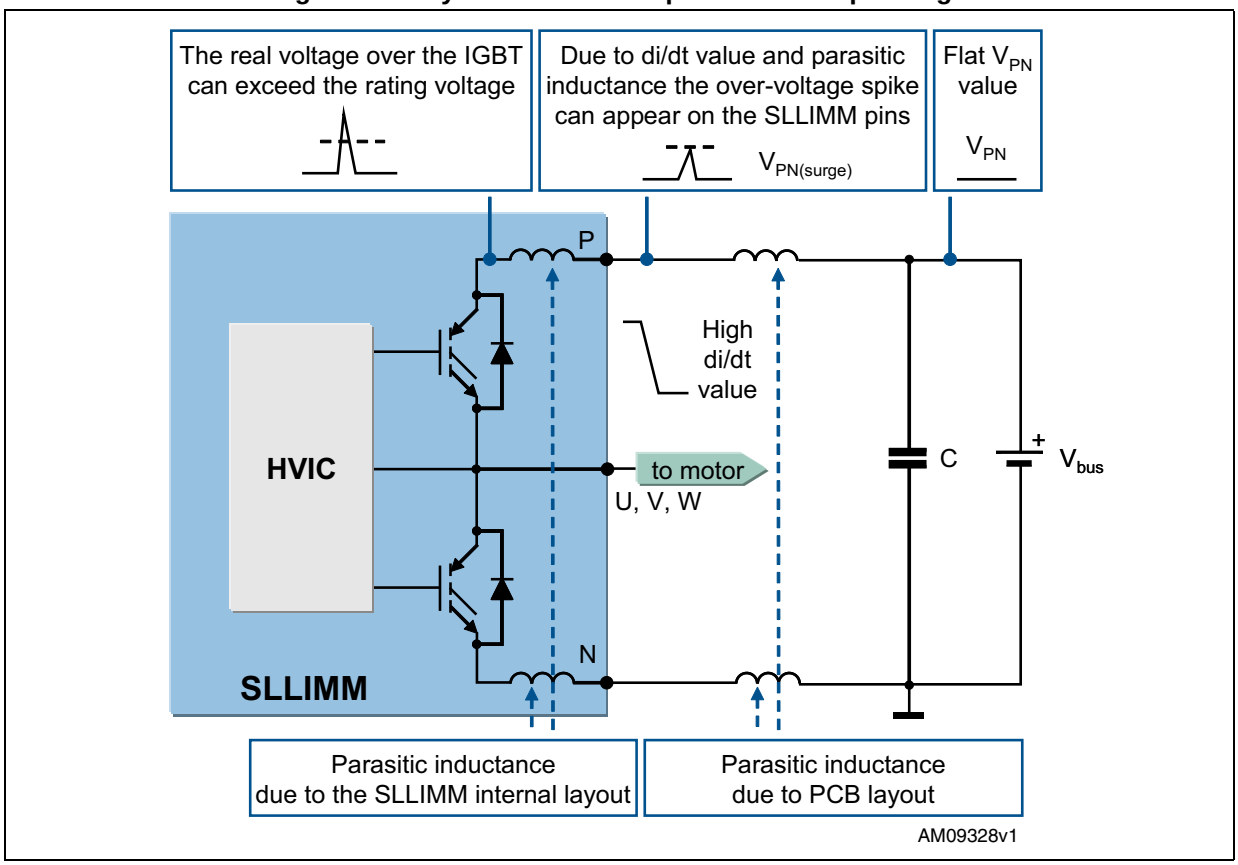
$$I_C(T_C) = \frac{T_{jmax} - T_C}{R_{th(j-c)} \cdot V_{CE(sat)(max)}(@T_{jmax}, I_C(T_C))}$$

- V_{PN}: supply voltage applied between P-N_U, N_V, N_W
- $V_{PN(surge)}$: supply voltage (surge) applied between P-N_U, N_V, N_W
- V_{CES}: collector emitter voltage

The power stage of SLLIMM is based on IGBTs (and freewheeling diodes) having 600 V V_{CES} rating. Considering the SLLIMM internal stray inductances during the commutations, which can generate up to 100 V of surge voltage, the maximum surge voltage between P-N ($V_{PN(surge)}$) allowed is 500 V. At the same time, the maximum supply voltage (in steady-state) applied between P-N (V_{PN}) allowed is 450 V because of an additional 50 V of surge voltage generated by the stray inductance between the SLLIMM and the DC-link capacitor.

Figure 8 shows the parasitic inductances of the output stage. It is possible to note that there are two major components, the first is due to the internal layout of SLLIMM, while the second is due to the layout of the board.

Figure 8. Stray inductance components of output stage



- $\pm I_C$: each IGBT continuous collector current

The allowable DC current continuously flowing at collector electrode (T_C = 25 °C). The I_C parameter is calculated according to *Equation 1*.

- t_{SCW}: short-circuit withstand time

The IGBTs incorporated inside the SLLIMM are tailored for a motor control application, therefore, short-circuit self-protection is one of the main module features.

t_{SCW} represents the short-circuit, non-repetitive, withstand time. If the short-circuit conditions exceed the above specifications, the lifetime of the device is drastically shortened. It is strongly recommended that the SLLIMM should not be operated under these conditions.

Table 3. Control part of STGIPL14K60

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage applied between OUT_U, OUT_V, OUT_W, and GND (V_{CC}=15 V)	V_{boot} -21 to V_{boot} +0.3	V
V_{CC}	Low voltage power supply	-0.3 to 21	V
V_{CIN}	Comparator input voltage	-0.3 to V_{CC} +0.3	V
V_{boot}	Bootstrap voltage	-0.3 to 620	V
V_{IN}	Logic input voltage applied between HIN, $\overline{LIN}$ and GND	-0.3 to 15	V
$V_{\overline{SD}/OD}$	Open drain voltage	-0.3 to 15	V
dV_{OUT}/dt	Allowed output slew rate	50	V/ns

- V_{CC}: low voltage power supply

V_{CC} represents the supply voltage of the control part. A local filtering is recommended to enhance the SLLIMM noise immunity. Generally, the use of one electrolytic capacitor (with a greater value but not negligible ESR) and a good quality (low ESR, low ESL) filter capacitor (hundreds of nF), faster than the electrolytic one to provide current, is suggested. Small filter capacitors are already connected inside the SLLIMM, directly on the involved pins (see internal circuits *Figure 5*, *6*, and *7*).

Please refer to *Table 4* in order to properly drive the SLLIMM.

Table 4. Supply voltage and operation behavior

V_{CC} voltage (typ. value) (1)	Operating behavior
< 12 V	As the voltage is lower than the UVLO threshold the control circuit is not fully turned on. A perfect functionality cannot be guaranteed.
12 V – 13.5 V	IGBTs can work, however conduction and switching losses increase due to low voltage gate signal.
13.5 V – 18 V	Recommended value (see relevant datasheets).
18 V – 21 V	IGBTs can work. Switching speed is faster and saturation current higher, increasing short-circuit broken risk and EMI issues.
> 21 V	Control circuit is destroyed. Absolute max. rating is 21 V.

1. Except for STGIPS10K60A. For further information please refer to the relevant datasheet.

Table 5. Total STGIPL14K60 system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstands voltage applied between each pin and heatsink plate (AC voltage, t = 60 sec.)	2500	V
T_j	Operating junction temperature	-40 to 150	°C
T_C	Module case operation temperature	-40 to 125	°C

2 Electrical characteristics and functions

In this section the main electrical characteristics of the power stage are discussed, together with a detailed description of all the SLLIMM functions.

2.1 IGBTs

The SLLIMM achieves power savings in the inverter stage thanks to the use of IGBTs manufactured with the proprietary advanced PowerMESH™ process.

These power devices, optimized for the typical motor control switching frequency, offer an excellent trade-off between voltage drop ($V_{CE(sat)}$) and switching speed (t_{fall}), and therefore minimize the two major sources of energy loss, conduction and switching, reducing the environmental impact of daily-use equipment. A full analysis on the power losses of the complete system is reported in *Section 4: Power losses and dissipation*.

This IGBT family is capable of surviving short-circuits lasting up to 5 microseconds, as expected by targeted applications.

2.2 Freewheeling diodes

The Turbo 2 ultrafast high voltage diodes have been adequately selected for the SLLIMM family and carefully tuned to achieve the best t_{rr}/V_F trade-off and softness as freewheeling diodes in order to further improve the total performance of the inverter and significantly reduce the electromagnetic interference (EMI) in motor control applications which are quite sensitive to this phenomena.

2.3 High voltage gate drivers

The SLLIMM is equipped with a versatile high voltage gate driver IC (HVIC), designed using BCD offline (Bipolar, CMOS, and DMOS) technology (see *Figure 9*) and particularly suited to field oriented control (FOC) motor driving applications, able to provide all the functions and current capability necessary for high side and low side IGBT driving. This driver can be used in all applications where high voltage shifted control is necessary and it includes a patented internal circuitry which replaces the external bootstrap diode.

Each high voltage gate driver chip controls two IGBTs in half bridge topology, offering the basic functions such as dead time, interlocking, integrated bootstrap diode, and also the advanced features such as smart shutdown (patented), fault comparator, and a dedicated high performance op amp for advanced current sensing. A schematic summary of the features by device are listed in *Table 1*.

In this application note the main characteristics of a high voltage gate drive related to the SLLIMM are discussed. For a greater understanding, please refer to the AN2738 application note.

Figure 9. High voltage gate drive die image

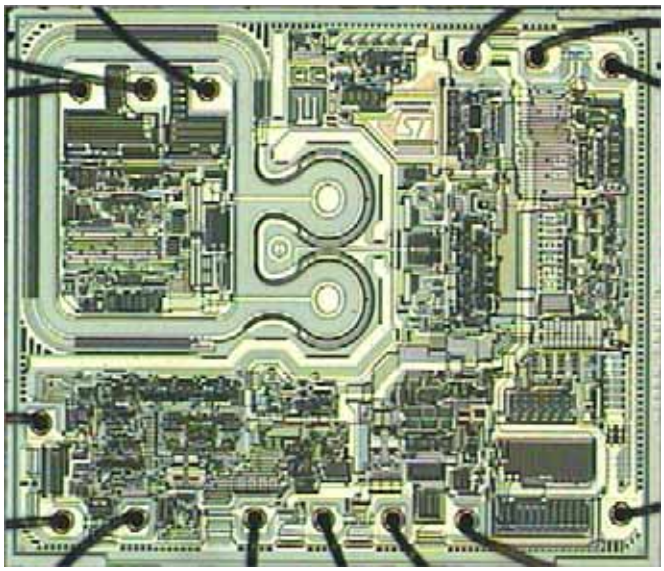
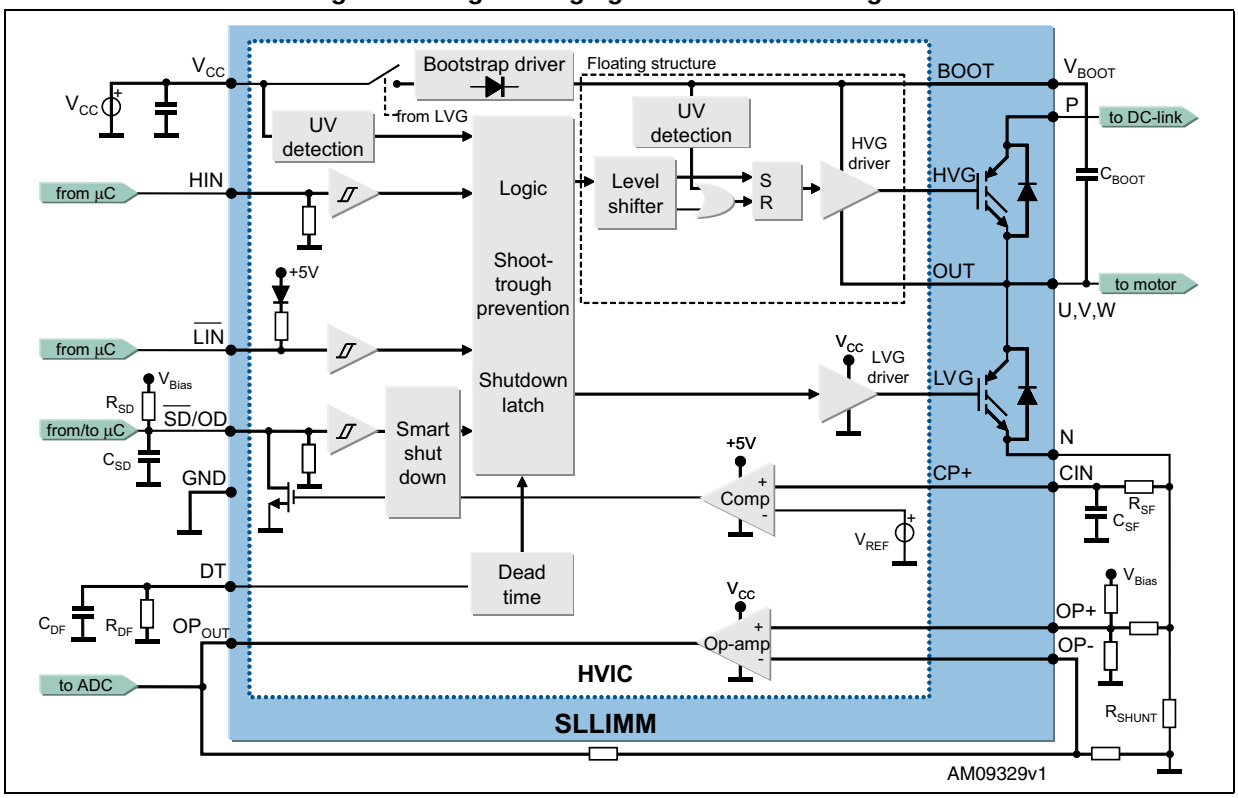


Figure 10. High voltage gate driver block diagram



2.3.1 Logic inputs

The high voltage gate driver IC has two logic inputs, HIN and LIN, to separately control the high side and low side outputs, HVG and LVG. Please refer to *Table 1* for the input signal logics by device.

In order to prevent any cross conduction between high side and low side IGBT a safety time (dead time) is introduced (see *Section 2.3.4: Dead time and interlocking function management* for further details).

All the logic inputs are provided with hysteresis (~1 V) for low noise sensitivity and are TTL/CMOS 3.3 V compatible. Thanks to this low voltage interface logic compatibility, the SLLIMM can be used with any kind of high performance controller, such as microcontrollers, DSPs or FPGAs.

As shown in the block diagrams of *Figure 11* and *Figure 12*, the logic inputs have internal pull-down (or pull-up) resistors in order to set a proper logic level in case of interruption in the logic lines. If logic inputs are left floating, the gate driver outputs LVG and HVG are set to low level. This simplifies the interface circuit by eliminating the six external resistors and, therefore saving cost, board space and number of components.

Figure 11. Logic input configuration for STGIPS10K60A

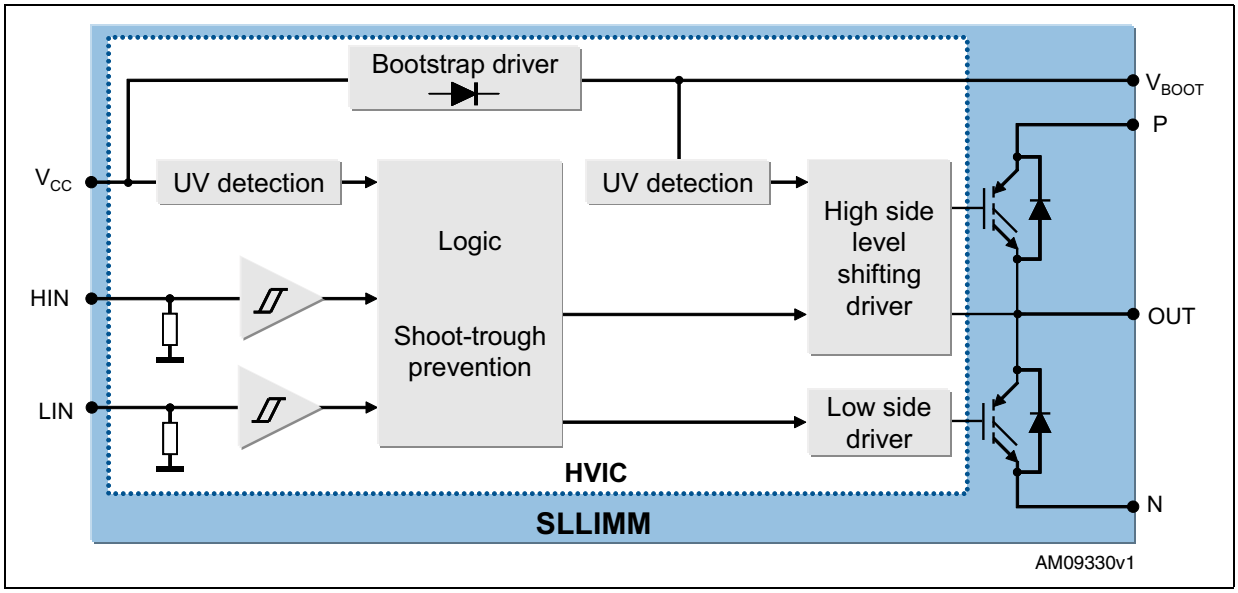
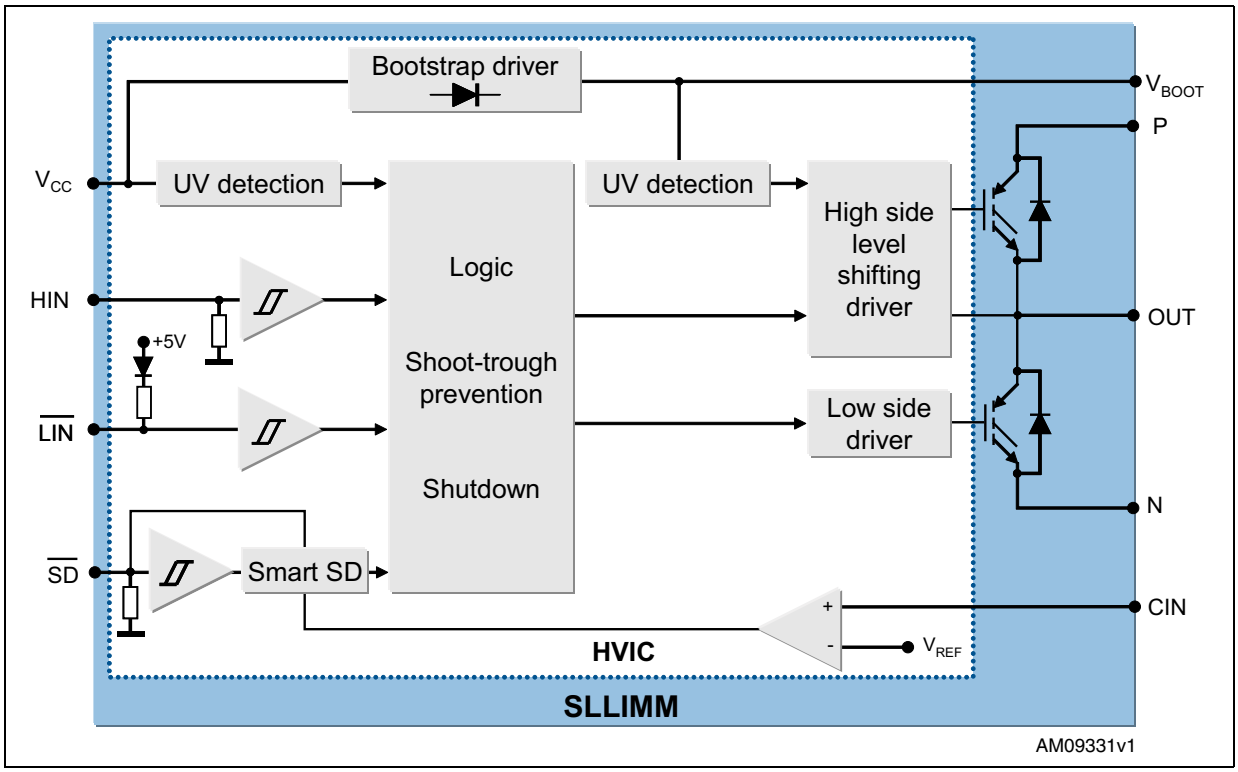


Figure 12. Logic input configuration for STGIPS14K60, STGIPL14K60, STGIPS20K60, and STGIPL20K60



The typical values of the integrated pull-up/down resistors are shown in *Table 6*:

Table 6. Integrated pull-up/down resistor values

Input pin	PN	Input pin logic	Internal pull-up	Internal pull-down
High side gate driving HIN_U, HIN_V, HIN_W	STGIPS10K60A	Active high		500 kΩ
Low side gate driving LIN_U, LIN_V, LIN_W	STGIPS10K60A	Active high		500 kΩ
High side gate driving HIN_U, HIN_V, HIN_W	STGIPS14K60 STGIPL14K60 STGIPS20K60 STGIPL20K60	Active high		85 kΩ
Low side gate driving $\overline{LIN}_U$, $\overline{LIN}_V$, $\overline{LIN}_W$	STGIPS14K60 STGIPL14K60 STGIPS20K60 STGIPL20K60	Active low	720 kΩ	
$\overline{SD}$ / OD shutdown	STGIPS14K60 STGIPL14K60 STGIPS20K60 STGIPL20K60	Active low		125 kΩ

2.3.2 High voltage level shift

The built-in high voltage level shift allows direct connection between the low voltage control inputs and the high voltage power half bridge in any power application up to 600 V. It is obtained thanks to the BCD offline technology which integrates, in the same die bipolar devices, low and medium voltage CMOS for analog and logic circuitry and high voltage DMOS transistors with a breakdown voltage in excess of 600 V. This key feature eliminates the need for external optocouplers, resulting in significant savings regarding component count and power losses. Other advantages are high-frequency operation and short input-to-output delays.

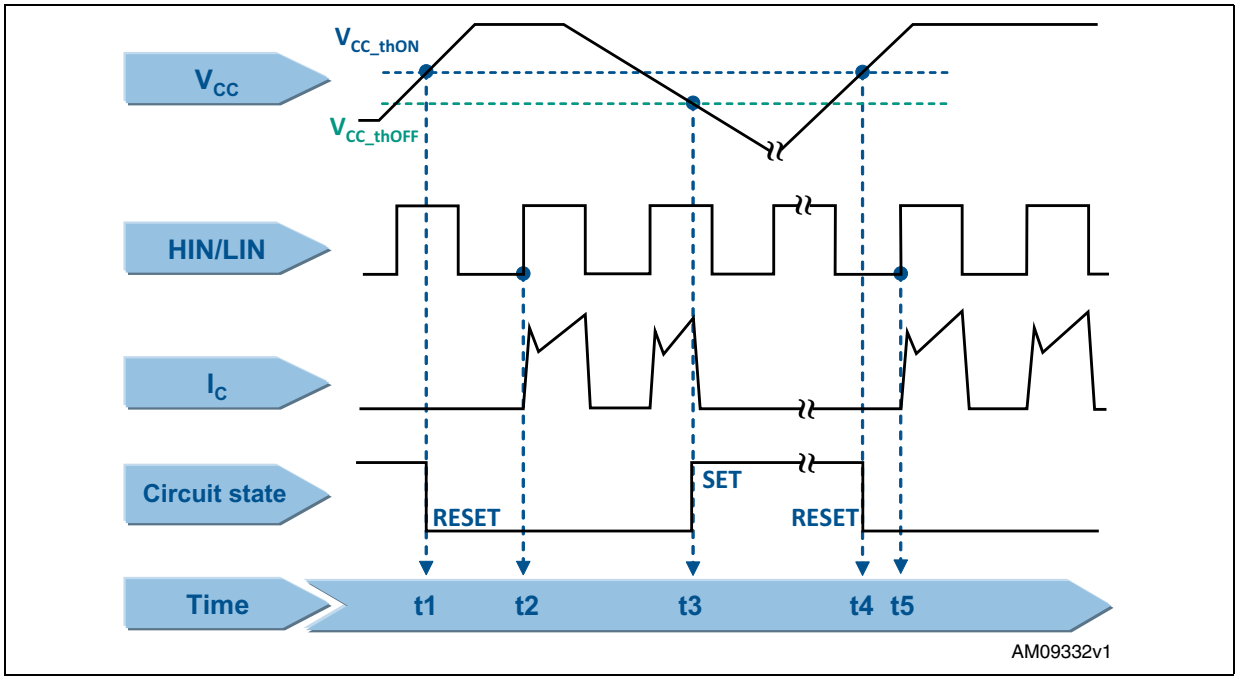
2.3.3 Undervoltage lockout

The SLLIMM supply voltage V_{CC} is continuously monitored by an undervoltage lockout (UVLO) circuitry which turns off the gate driver outputs when the supply voltage goes below the V_{CC_thOFF} threshold specified on the datasheet and turns on the IC when the supply voltage goes above the V_{CC_thON} voltage. A hysteresis of about 1.5 V is provided for noise rejection purposes. The high voltage floating supply V_{boot} is also provided with a similar undervoltage lockout circuitry. When the driver is in UVLO condition, both gate driver outputs are set to low level, setting the half bridge power stage output to high impedance.

The timing chart of undervoltage lockout, plotted in *Figure 13*, is based on the following steps:

- t1: when the V_{CC} supply voltage raises the V_{CC_thON} threshold, the gate driver starts to work after the next input signal HIN/LIN is on. The circuit state becomes RESET.
- t2: input signal HIN/LIN is on and the IGBT is turned on.
- t3: when the V_{CC} supply voltage goes below the V_{CC_thOFF} threshold, the UVLO event is detected. The IGBT is turned off in spite of input signal HIN/LIN. The state of the circuit is now SET.
- t4: the gate driver re-starts once the V_{CC} supply voltage again raises the V_{CC_thON} threshold.
- t5: input signal HIN/LIN is on and the IGBT is turned on again.

Figure 13. Timing chart of undervoltage lockout function



2.3.4 Dead time and interlocking function management

In order to prevent any possible cross-conduction between high side and low side IGBTs, the SLLIMM provides both the dead time and the interlocking functions. The interlocking function is a logic operation which sets both the outputs to low level when the inputs are simultaneously active. The dead time function is a safety time introduced by the device between the falling edge transition of one driver output and the rising edge of the other output. If the rising edge set externally by the user occurs before the end of this dead time, it is ignored and results as delayed until the end of the dead time.

Table 7. Interlocking function truth table of STGIPS10K60A

Condition	Logic input (V_I)		Outputs	
	LIN	HIN	LVG	HVG
Interlocking half bridge tri-state	H	H	L	L
0 “logic state” half bridge tri-state	L	L	L	L
1 “logic state” low side direct driving	H	L	H	L
1 “logic state” high side direct driving	L	H	L	H

The dead time is internally set at 320 ns as the typical value of STGIPS10K60A.

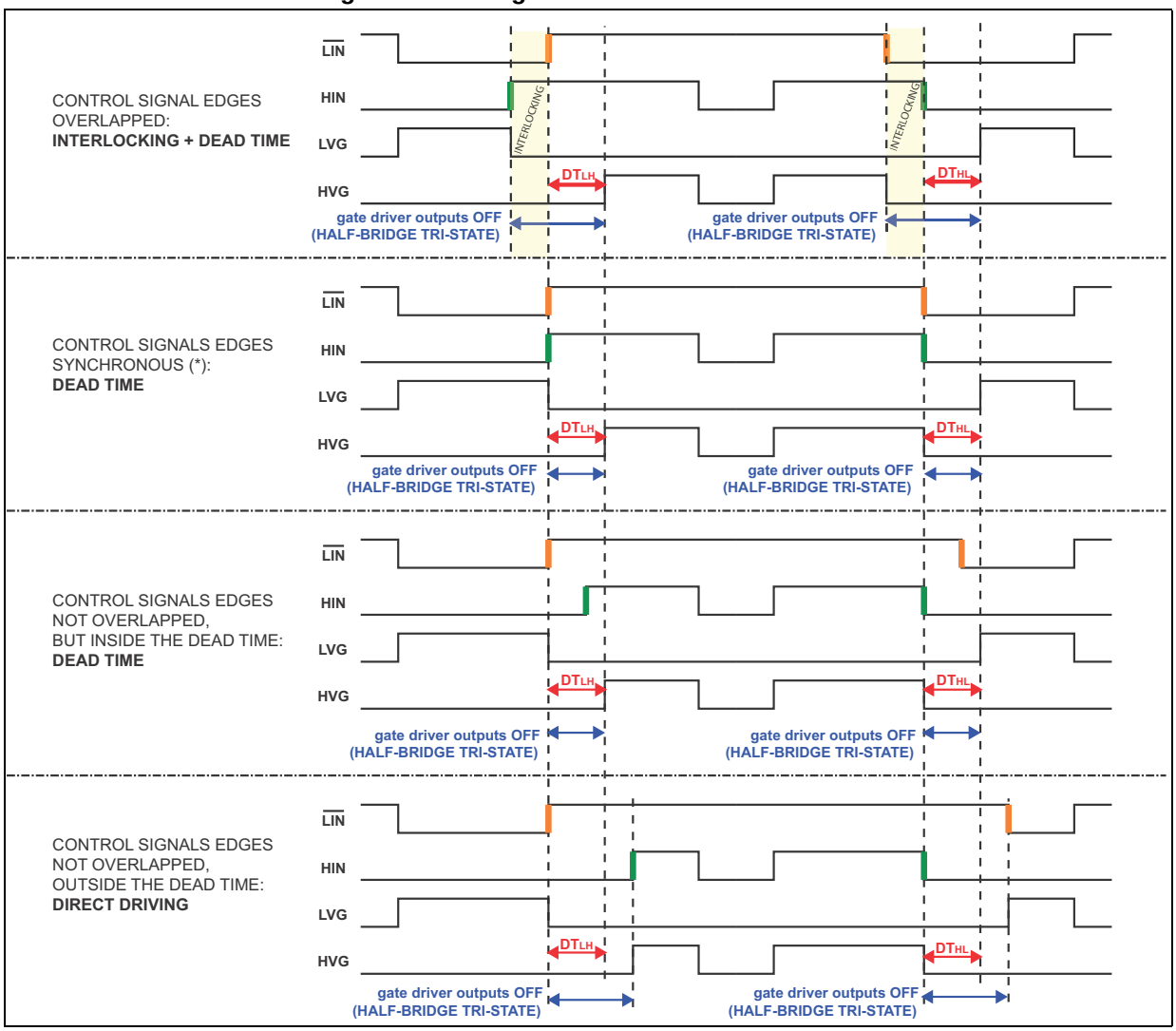
Table 8. Interlocking function truth table of STGIPS14K60, STGIPL14K60, STGIPS20K60, and STGIPL20K60

Condition	Logic input (V_I)			Outputs	
	$\overline{SD}$	$\overline{LIN}$	HIN	LVG	HVG
Shutdown enable half bridge tri-state	L	X	X	L	L
Interlocking half bridge tri-state	H	L	H	L	L
0 “logic state” half bridge tri-state	H	H	L	L	L
1 “logic state” low side direct driving	H	L	L	H	L
1 “logic state” high side direct driving	H	H	H	L	H

Note: X: not important.

The dead time is internally set at 600 ns as typical value. In *Figure 14* the details of dead time and interlocking function management of the STGIPS14K60, STGIPL14K60, STGIPS20K60, and STGIPL20K60 products are described.

Figure 14. Timing chart of dead time function



2.3.5 Comparators for fault sensing

The SLLIMM family integrates up to three comparators (with reference to the product line-up in *Table 1*) intended for advanced fault protection, such as overcurrent, overtemperature or any other type of fault measurable via a voltage signal. Each comparator has an internal reference voltage V_{REF}, specified in the datasheet, on its inverting input (see *Figure 10*), while the non-inverting input is available on C_{IN} pins (one per half bridge). The comparators input can be connected to an external shunt resistor, in order to implement a simple overcurrent or short-circuit detection function, as discussed in detail in *Section 2.3.6: Short-circuit protection and smart shutdown function*. Nevertheless, in the case of three internal comparators, they can be separately used in order to implement three independent controls.

2.3.6 Short-circuit protection and smart shutdown function

The SLLIMM is able to monitor the output current and provide protection against overcurrent and short-circuit conditions in a very short time (comparator triggering to high/low side driver turn-off propagation delay t_{isd} = 200 ns), thanks to the smart shutdown function. This feature is based on an innovative patented circuitry which provides an intelligent fault management operation and greatly reduces the protection intervention delay independently on the protection time duration which can be set as desired by the device user.

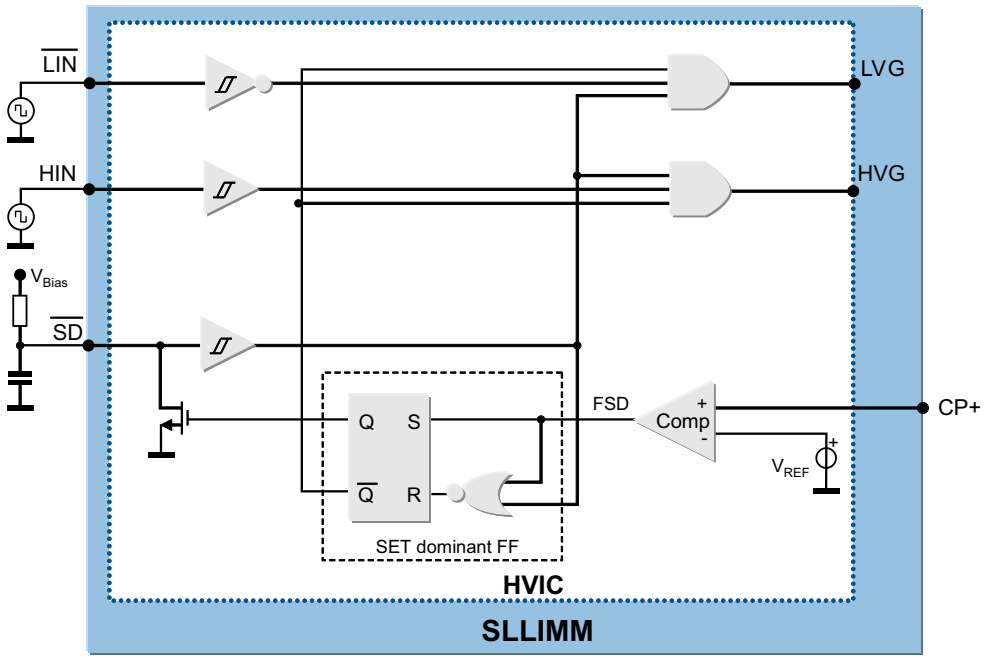
As already mentioned in *Section 2.3.5: Comparators for fault sensing* and shown in *Figure 10*, each comparator input can be connected to an external shunt resistor, R_{SHUNT}, in order to implement a simple overcurrent detection function. An RC filter network (R_{SF} and C_{SF}) is necessary to prevent erroneous operation of the protection. The output signal of the comparators is fed to an integrated MOSFET with the open drain available on the $\overline{SD}$/OD pin, shared with the $\overline{SD}$ input. When the comparator triggers, the device is set in shutdown state and all its outputs are set to low level, leaving the half bridge in tri-state. In common overcurrent protection architectures, usually the comparator output is connected to the SD input and an external RC network (R_{SD} and C_{SD}) is connected to this $\overline{SD}$/OD line in order to provide a mono-stable circuit which implements a protection time when a fault condition occurs.

Contrary to common fault detection systems, the new smart shutdown structure allows to immediately turn off the output gate driver in the case of fault, without waiting for the external capacitor to be discharged. This strategy minimizes the propagation delay between the fault detection event and the actual outputs switch off. In fact, the time delay between the fault and outputs disabling is not dependent on the RC value of the external SD circuitry but, thanks to the new architecture, has a preferential path internally in the driver. Then the device immediately turns off the driver outputs and latches the turn-on of the open drain switch, until the SD signal has reached its lower threshold. After the SD signal goes below the lower threshold, the open drain is switched off (see *Figure 16*).

The smart shutdown system provides the possibility to increase the value of the external RC network across the SD pin (sized to fix the disable time generated after the fault event) as much as desired by the user without compromising the intervention time delay of the SLLIMM protection.

A block diagram of the smart shutdown architecture is depicted in *Figure 15*.

Figure 15. Smart shutdown equivalent circuitry



In normal operation the outputs follow the commands received from the respective input signals.

When a fault detection event occurs, the fault signal (FSD) is set to high by the fault detection circuit output and the FF receives a SET input signal. Consequently, the FF outputs set the SLLIMM output signals to low level and, at the same time, turn on the open drain MOSFET which works as active pull-down for the $\overline{SD}$ signal. Note that the gate driver outputs stay at low level until the $\overline{SD}$ pin has experienced both a falling edge and a rising edge, although the fault signal could be returned to low level immediately after the fault sensing. In fact, even if the FF is reset by the falling edge of the $\overline{SD}$ input, the $\overline{SD}$ signal also works as enable for the outputs, thanks to the two AND ports. Moreover, once the internal open drain transistor has been activated, due to the latch, it cannot be turned off until the $\overline{SD}$ pin voltage reaches the low logic level. Note that, since the FF is SET dominant, oscillations of the $\overline{SD}$ pin are avoided if the fault signal remains steady at high level.

2.3.7 Timing chart of short-circuit protection and smart shutdown function

With reference to *Figure 16*, the short-circuit protection is based on the following steps:

- t1: when the output current is lower than the max. allowed level, the SLLIMM is working in normal operation.
- t2: when the output current reaches the max. allowed level (I_{SC}), the overcurrent/short-circuit event is detected and the protection is activated. The voltage across the shunt resistor, and then on the C_{IN} pin, exceeds the V_{REF} value, the comparator triggers, setting the device in shutdown state and both its outputs are set to low level leading the half bridge to tri-state. The smart shutdown switches off the IGBT gate (HVG, LVG) through a preferential path (200 ns as typical internal delay time) and, at the same time, it switches on the M1 internal MOSFET. The SD signal starts the discharge phase and its value drops with a time constant τ_A. The time constant τ_A value is given by:

Equation 2

$$\tau_A = (R_{ON\_OD} // R_{SD}) \cdot C_{SD}$$

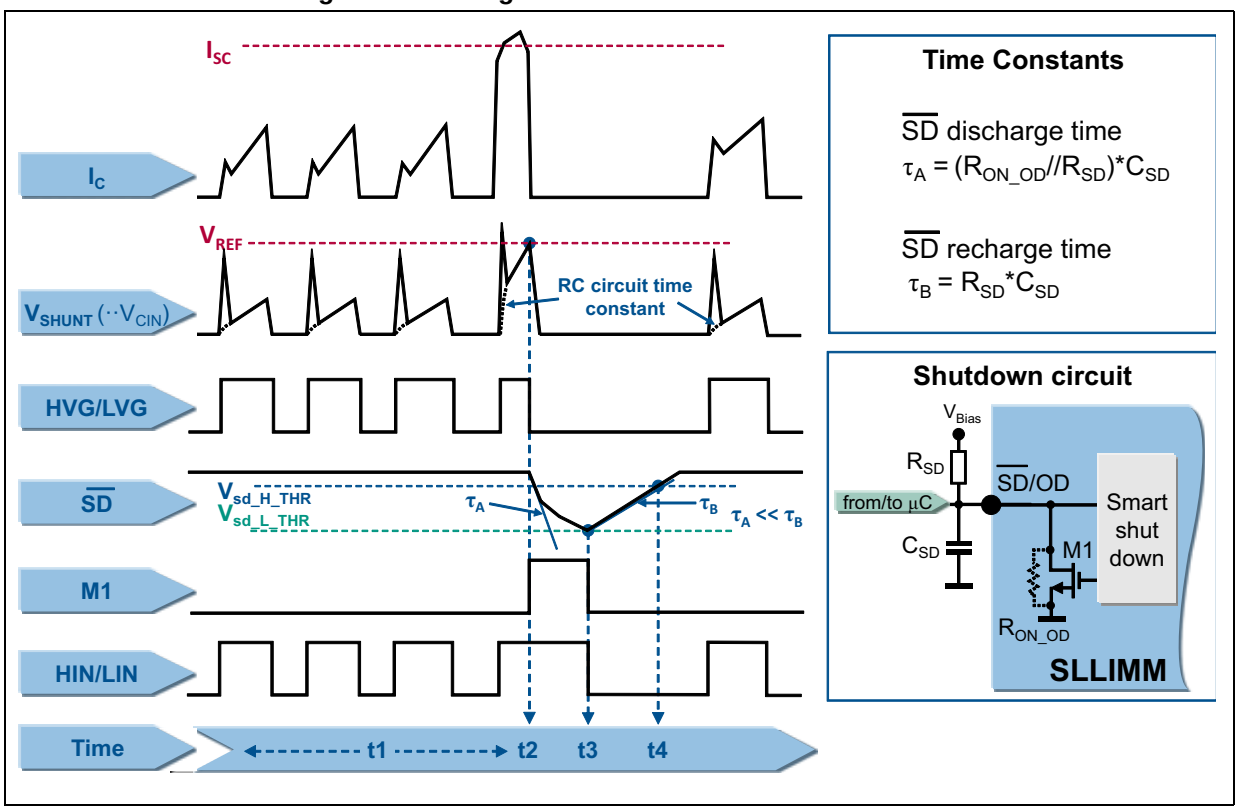
- t3: the SD signal reaches the lower threshold $V_{sd\_L\_THR}$ and the control unit switches off the input HIN and LIN. The smart shutdown is disabled (M1 off) and SD can rise up with a time constant τ_B, given by:

Equation 3

$$\tau_B = R_{SD} \cdot C_{SD}$$

- t4: when the SD signal reaches the upper threshold $V_{sd\_H\_THR}$, the system is re-enabled.

Figure 16. Timing chart of smart shutdown function



2.3.8 Current sensing shunt resistor selection

As previously discussed, the shunt resistors R_{SHUNT} externally connected between the N pin and ground (see *Figure 10*) are used to realize the overcurrent detection.

When the output current exceeds the short-circuit reference level (I_{SC}), the C_{IN} signal overtakes the V_{REF} value and the short-circuit protection is active. For a reliable and stable operation the current sensing resistor should be a high quality, low tolerance non-inductive type. In fact, stray inductance in the circuit, which includes the layout, the RC filter, and also the shunt resistor, must be minimized in order to avoid undesired short-circuit detection.

For these reasons, the shunt resistor and the filtering components must be placed as close as possible to the SLLIMM pins, for additional suggestions refer to *Section 5.1: Layout suggestions*.

The value of the current sense resistor can be calculated by following different guidelines, functions of the design specifications, or requirements. A common criterion is presented here based on the following steps:

- Defining of the overcurrent threshold value (I_{OC_th}). For example, it can be fixed considering the IGBT typical working current in the application and adding 20-30% as overcurrent.
- Calculation of the shunt resistor value according to the conditioning network. An example of the conditioning network is shown in *Figure 22*. Further details can be found in the user manuals listed (see References *7*, References *8*, and References *9*).
- Selection of the closest shunt resistor commercial value.
- Calculation of the power rating of the shunt resistor, taking into account that this parameter is strongly temperature dependent. Therefore, the power derating ratio of the shunt resistor, $\Delta P(T)\%$, shown in the manufacturer's datasheet, must be considered in the calculation as follows:

Equation 4

$$P_{SHUNT}(T) = \frac{R_{SHUNT} \cdot I_{RMS}^2}{\Delta P(T)\%}$$

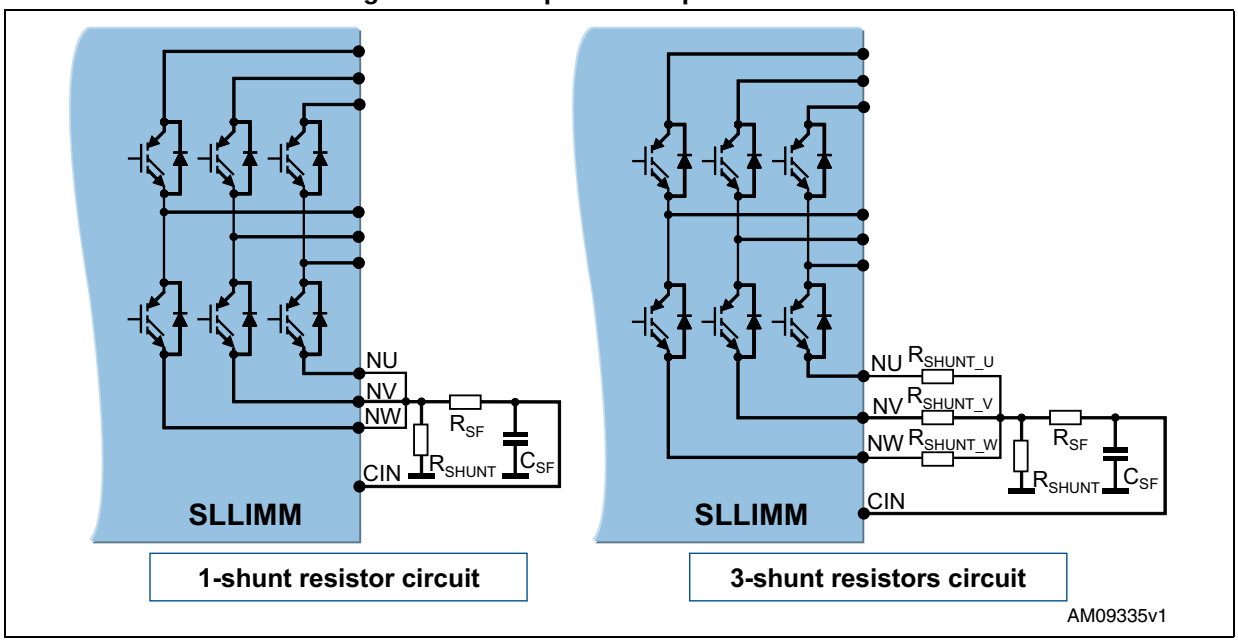
where I_{RMS} is the IGBT RMS working current.

For a proper selection of the shunt resistor, a safety margin of at least 30% is recommended on the calculated power rating.

2.3.9 RC filter network selection

Two options of shunt (1- or 3-shunt) resistor circuit can be adopted in order to implement different control technique and short-circuit protection, as shown in *Figure 17*.

Figure 17. Examples of SC protection circuit



A RC filter network is required to prevent undesired short-circuit operation due to the noise on the shunt resistor.

Both solutions allow to detect the total current in all three phases of the inverter. The filter is based on the R_{SF} and C_{SF} network and its time constant is given by:

Equation 5

$$t_{SF} = R_{SF} \cdot C_{SF}$$

In addition to the RC time constant, the turn-off propagation delay of the gate driver, t_{isd} (specified in the datasheet) and the IGBT turn-off time (in the range of tens of ns), must be considered in the total delay time (t_{Total}), which is the time necessary to completely switch off the IGBT once the short-circuit event is detected. Therefore, the t_{Total} is calculated as follows:

Equation 6

$$t_{Total} = t_{SF} + t_{isd} + t_{off}$$

also considering that the IGBT short-circuit withstand time (t_{SC}) is 5 µs, the t_{SF} is recommended to be set in the range of 1~2 µs.

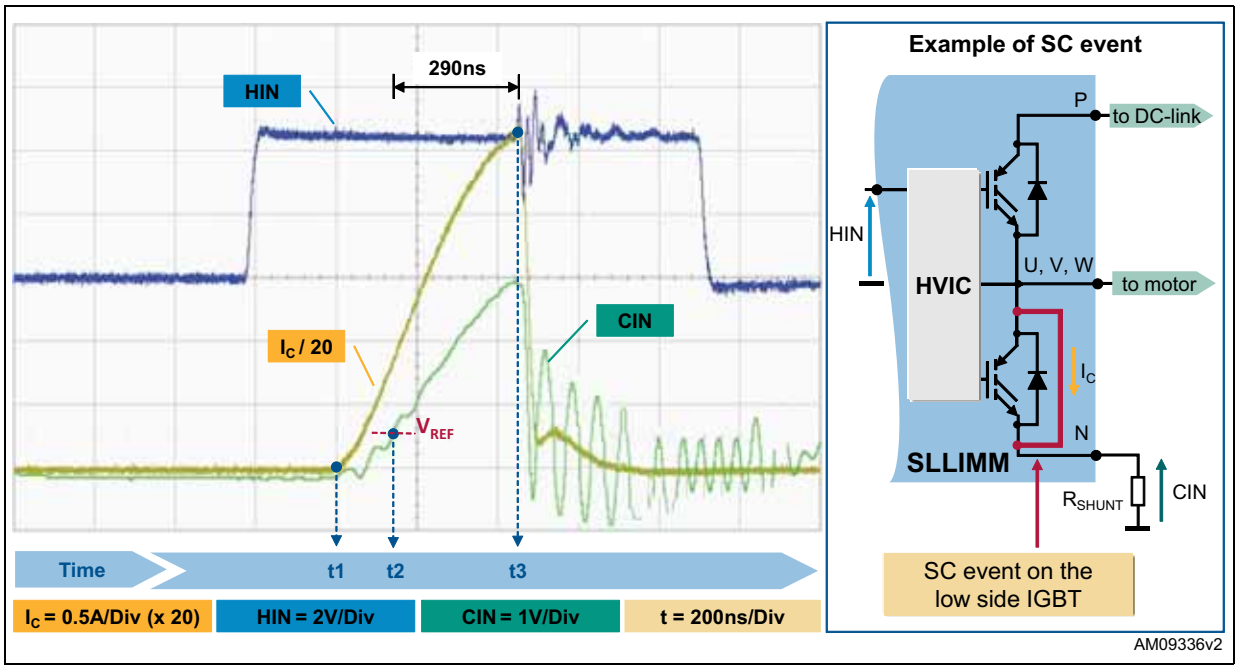
In the case of a 3-shunt resistors circuit, a specific control technique can be implemented by using the three shunt resistors (R_{SHUNT_U}, R_{SHUNT_V} and R_{SHUNT_W}) able to monitor each phase current.

An example of a short-circuit event is shown in *Figure 18*, where it is possible to note the very fast protection, thanks to the smart shutdown function, against fault events. The main steps are:

- t1: collector current I_C starts to rise. SC event is not detected yet due to the RC network on the C_{IN} pin
- t2: voltage on V_{CIN} reaches the V_{REF}. SC event is detected and the smart shutdown starts to turn off the SLLIMM.
- t3: the SLLIMM is definitively turned off in less than 300 ns (including the $t_{d(off)}$ time of IGBT) from SC detection.

Finally, the total disable time is t3-t2 and the total SC action time is t3-t1.

Figure 18. Example of SC event



2.3.10 Overtemperature protection

STGIPS10K60A, STGIPL14K60, and STGIPL20K60 are equipped with a negative temperature coefficient (NTC) thermistor for an easy overtemperature protection, in the case of slow case temperature drift or just for the temperature measurements, sending this information to the microcontroller in real-time. Due to the thermal impedance of SLLIMM and its own time constant, the NTC thermistor is not suited to detect rapid junction temperature rise of the power devices directly. Therefore, it cannot be used for short-circuit or overcurrent protection, but only for slow changes in temperature monitoring.

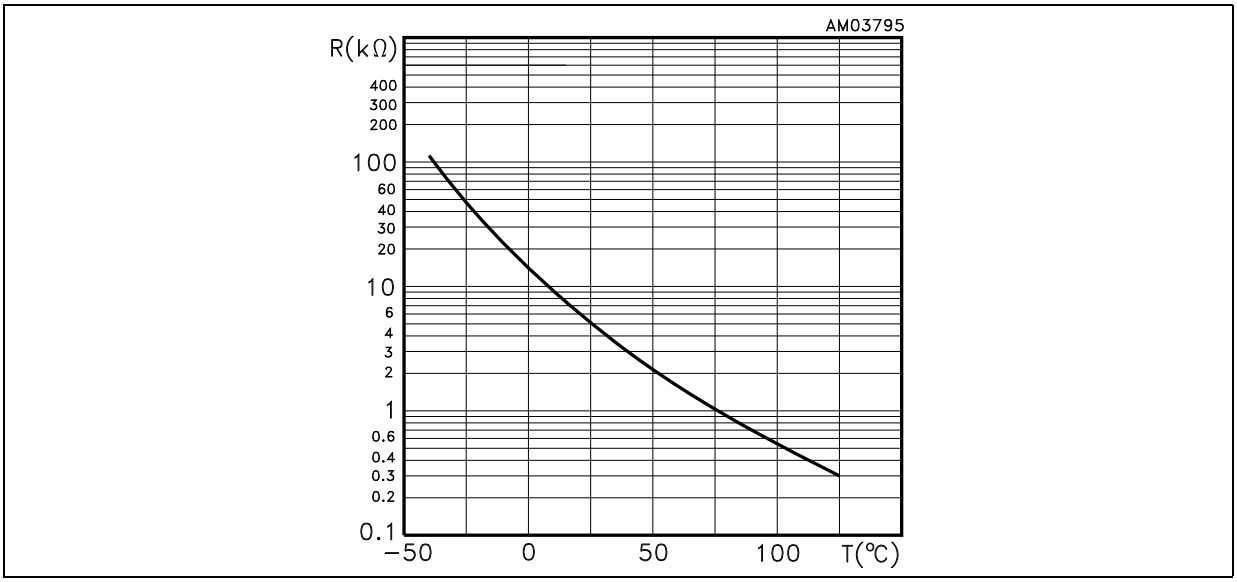
The resistance versus temperature characteristic of NTC thermistor, represented in *Figure 19*, is non-linear and is described by the following expression:

Equation 7

$$R(T) = R_{25} \cdot e^{B\left(\frac{1}{T} - \frac{1}{298}\right)}$$

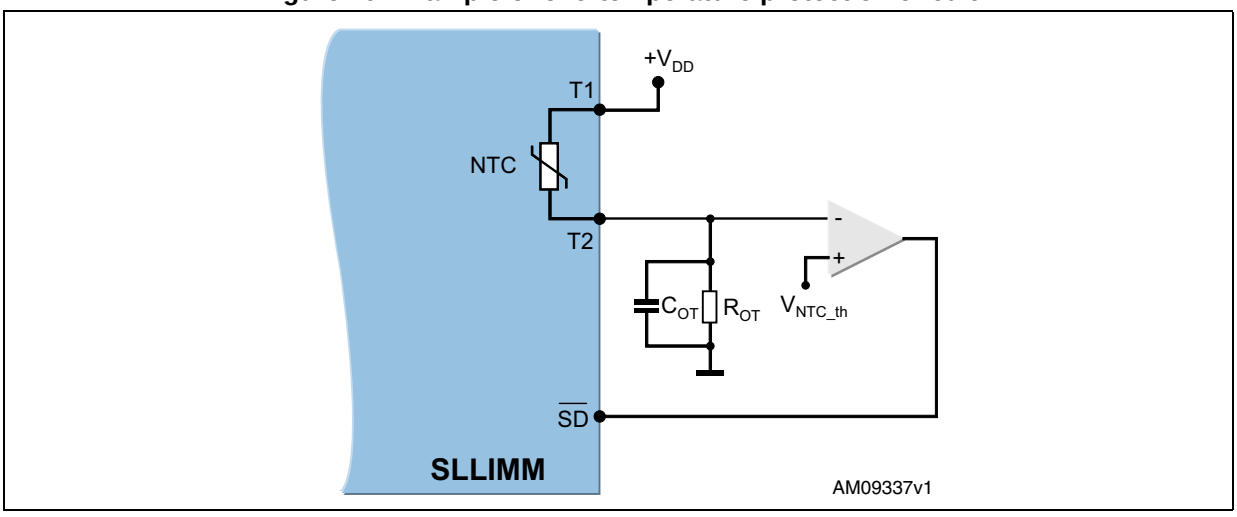
where T is the temperature in Kelvin, B and R_{25}, respectively, are a constant value in the SLLIMM working range and the resistance value at 25 °C, both parameters are shown in the datasheet.

Figure 19. NTC resistance vs. temperature curve



An easy circuit, using a voltage divider, for both overtemperature protection and temperature monitoring, is shown in *Figure 20*:

Figure 20. Example of overtemperature protection circuit



The external comparator is used to send a shutdown signal to the SLLIMM in case of overtemperature. The V_{NTC_th} is a threshold voltage, fixed by design, and connected on the non inverting input, whilst the inverting input is connected on a voltage divider based on the NTC and R_{OT} resistors. When voltage on the inverting input exceeds the V_{NTC_th} value the comparator triggers, pulling down the $\overline{SD}$ and, consequently, switching off the IGBTs.

For a proper sizing of the voltage divider, first of all the maximum allowed temperature level (T_{OT_Max}) must be fixed, consequently the thermistor resistance is given by *Equation 7*, as well as by *Figure 19*. The value of R_{OT} resistance can be calculated by using the voltage divider formula:

Equation 8

$$V^{-}(T) = \frac{R_{OT}}{R_{NTC}(T) + R_{OT}} \cdot V_{DD}$$

taking into account that, if $T = T_{OT\_Max}$ then $V^{-}(T_{OT\_Max}) = V_{NTC\_th}$.

The maximum allowed power on the thermistor should not exceed 50 mW in all the operating range, in order to guarantee a safe working condition and avoid power consumption affecting the temperature measurement through self-heating. Therefore, considering ($T = T_{OT\_Max}$), it must be:

Equation 9

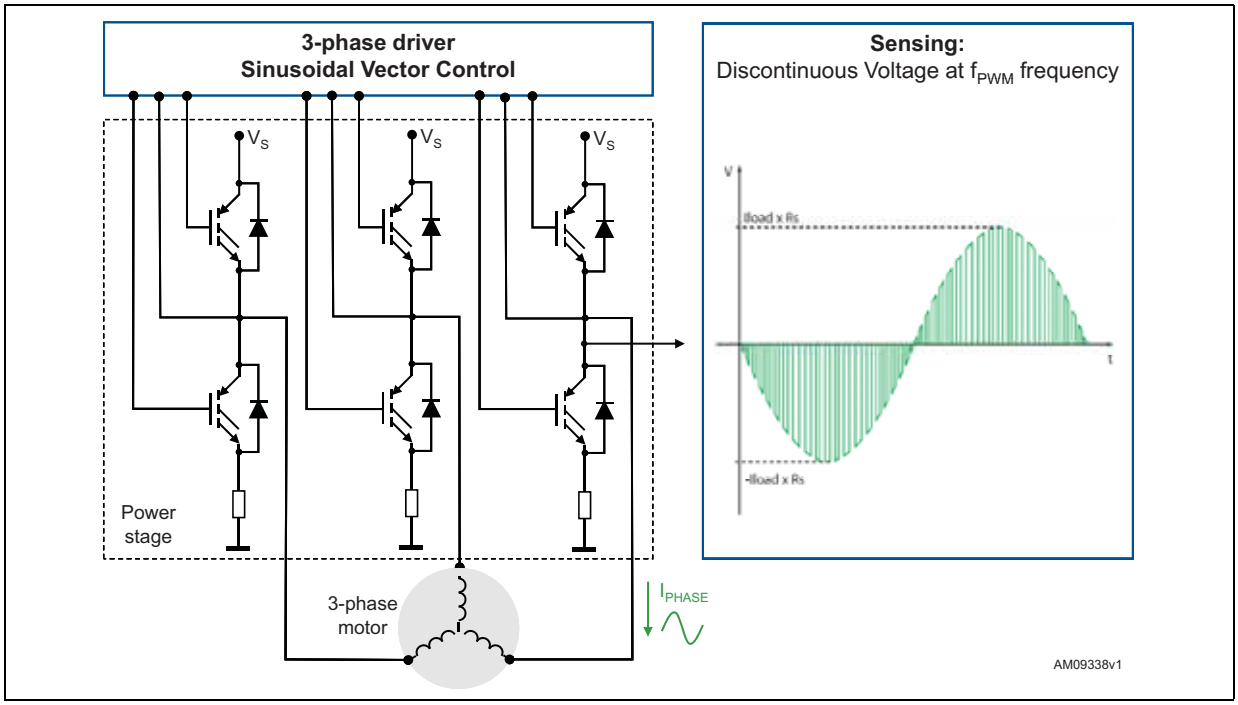
$$R_{NTC} \cdot I^2 = R_{NTC} \cdot \left(\frac{V_{DD}}{R_{NTC} + R_{OT}} \right)^2 \leq 50\text{mW}$$

Finally, to increase the noise immunity of the NTC thermistor, it is recommended to parallel a decoupling capacitor (C_{OT}), whose value must be between 10 to 100 nF.

2.3.11 Op amps for advanced current sensing

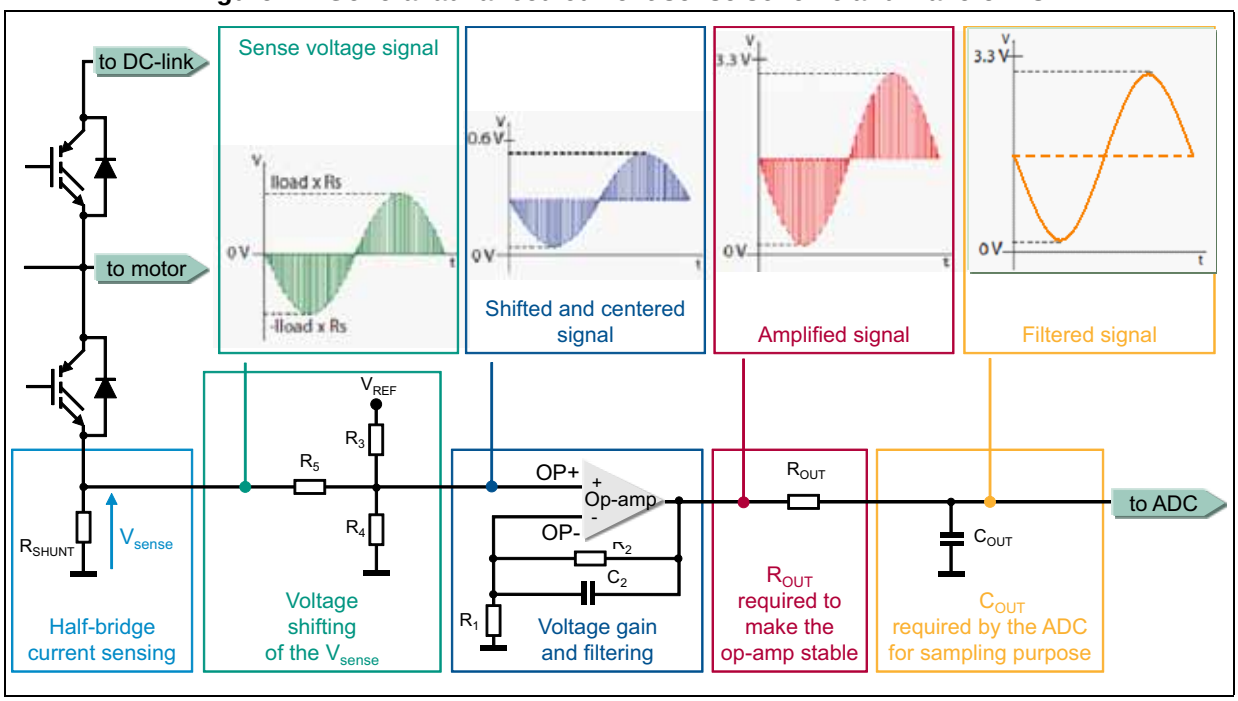
The SLLIMM devices, in the SDIP-38L package, integrate also three operational amplifiers optimized for field oriented control (FOC) applications. In a typical FOC application the currents in the three half bridges are sensed using a shunt resistor. The analog current information is transformed into a discontinuous sense voltage signal, having the same frequency as the PWM signal driving the bridge. The sense voltage is a bipolar analog signal, whose sign depends on the direction of the current (see *Figure 21*):

Figure 21. 3-phase system



The sense voltage signals must be provided to an A/D converter. They are usually shifted and amplified by dedicated op amps in order to exploit the full range of the A/D converter. The typical scheme and principle waveforms are shown in *Figure 22*:

Figure 22. General advanced current sense scheme and waveforms



ADCs used in vector control applications have a typical full scale range (FSR) of about 3.3 V. The sense signals must be shifted and centered on FSR/2 voltage (about 1.65 V) and amplified with a gain which provides the matching between the maximum value of the sensed signal and the FSR of the ADC. Some typical examples of sense network sizing can be found in the user manuals listed (see References *7*, References *8*, and References *9*).

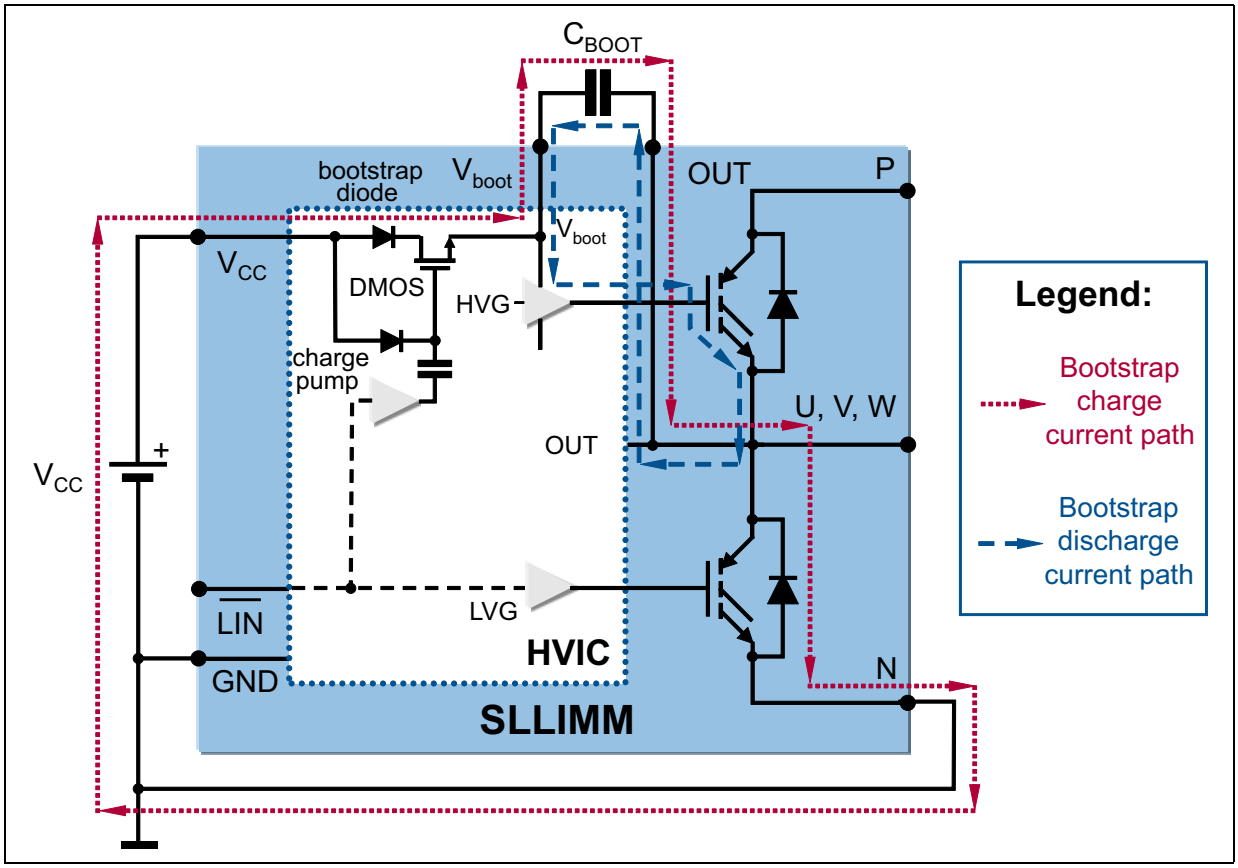
2.3.12 Bootstrap circuit

In the 3-phase inverter the emitters of the low side IGBTs are connected to the negative DC bus (V_{DC-}) as common reference ground, which allows all low side gate drivers to share the same power supply, while, the emitter of high side IGBTs is alternately connected to the positive (V_{DC+}) and negative (V_{DC-}) DC bus during the running conditions.

A bootstrap method is a simple and cheap solution to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode. The SLLIMM family includes a patented integrated structure that replaces the external diode. It is realized with a high voltage DMOS driven synchronously with the low side driver (LVG) and a diode in series. An internal charge pump provides the DMOS driving voltage.

The operation of the bootstrap circuit is shown in *Figure 23*. The floating supply capacitor C_{BOOT} is charged, from the V_{CC} supply, when the V_{OUT} voltage is lower than the V_{CC} voltage (e.g. low side IGBT is on), through the bootstrap diode and the DMOS path with reference to the “bootstrap charge current path”. During the high side IGBT on phase, the bootstrap circuit provides the right gate voltage to properly drive the IGBT (see “bootstrap discharge current path”). This circuit is iterated for all three half bridges.

Figure 23. Bootstrap circuit



The value of the C_{BOOT} capacitor should be calculated according to the application condition and must take the following into account:

- voltage across C_{BOOT} must be maintained at a value higher than the undervoltage lockout level for the IC driver. This enables the high side IGBT to work with a correct gate voltage (lower dissipation and better overall performances). Bear in mind that if a voltage below the UVLO threshold is applied on the bootstrap channel, the IC disables itself (no output) without any fault signal.
- the voltage across C_{BOOT} is affected by different components such as drop across the integrated bootstrap structure, drop across the low side IGBT, and others.
- when the high side IGBT is on, the C_{BOOT} capacitor discharges mainly to provide the right IGBT gate charge but other phenomena must be considered such as leakage currents, quiescent current, etc.

2.3.13 Bootstrap capacitor selection

A simple method to properly size the bootstrap capacitor considers only the amount of charge that is needed when the high voltage side of the driver is floating and IGBT gate is driven once. This approach does not take into account either the duty cycle of the PWM, or the fundamental frequency of the current.

During the bootstrap capacitor charging phase, the low side IGBT is on and the voltage across C_{BOOT} (V_{CBOOT}) can be calculated as follows:

Equation 10

$$V_{CBOOT} = V_{CC} - V_F - V_{RDS(on)} - V_{CE(sat)max}$$

where:

V_{CC}: supply voltage of gate driver

V_F: bootstrap diode forward voltage drop

$V_{CE(sat)max}$: maximum emitter collector voltage drop of low side IGBT

$V_{RDS(on)}$: DMOS voltage drop

The dimension of the bootstrap capacitance C_{BOOT} value is based on the minimum voltage drop (ΔV_{CBOOT}) to guarantee when the high side IGBT is on, and must be:

Equation 11

$$\Delta V_{CBOOT} = V_{CC} - V_F - V_{RDS(on)} - V_{GE(min)} - V_{CE(sat)max}$$

under the condition:

Equation 12

$$V_{CBOOT(min)} > V_{BS\_thON}$$

where:

$V_{GE(min)}$: minimum gate emitter voltage of high side IGBT

V_{BS_thON}: bootstrap turn-on undervoltage threshold (maximum value, see datasheet)

Considering the factors contributing to V_{CBOOT} decreasing, the total charge supplied by the bootstrap capacitor (during high side on phase) is:

Equation 13

$$Q_{TOT} = Q_{GATE} + \left(I_{LKGE} + I_{QBO} + I_{LK} + I_{LKDiode} + I_{LKCap}\right) \cdot t_{Hon} + Q_{LS}$$

where:

Q_{GATE}: total IGBT gate charge

I_{LKGE}: IGBT gate emitter leakage current

I_{QBO}: bootstrap circuit quiescent current

I_{LK}: bootstrap circuit leakage current

$I_{LKDiode}$: bootstrap diode leakage current

I_{LKCap}: bootstrap capacitor leakage current (relevant when using an electrolytic capacitor but can be ignored if other types of capacitors are used)

t_{Hon}: high side on time

Q_{LS}: charge required by the internal level shifters

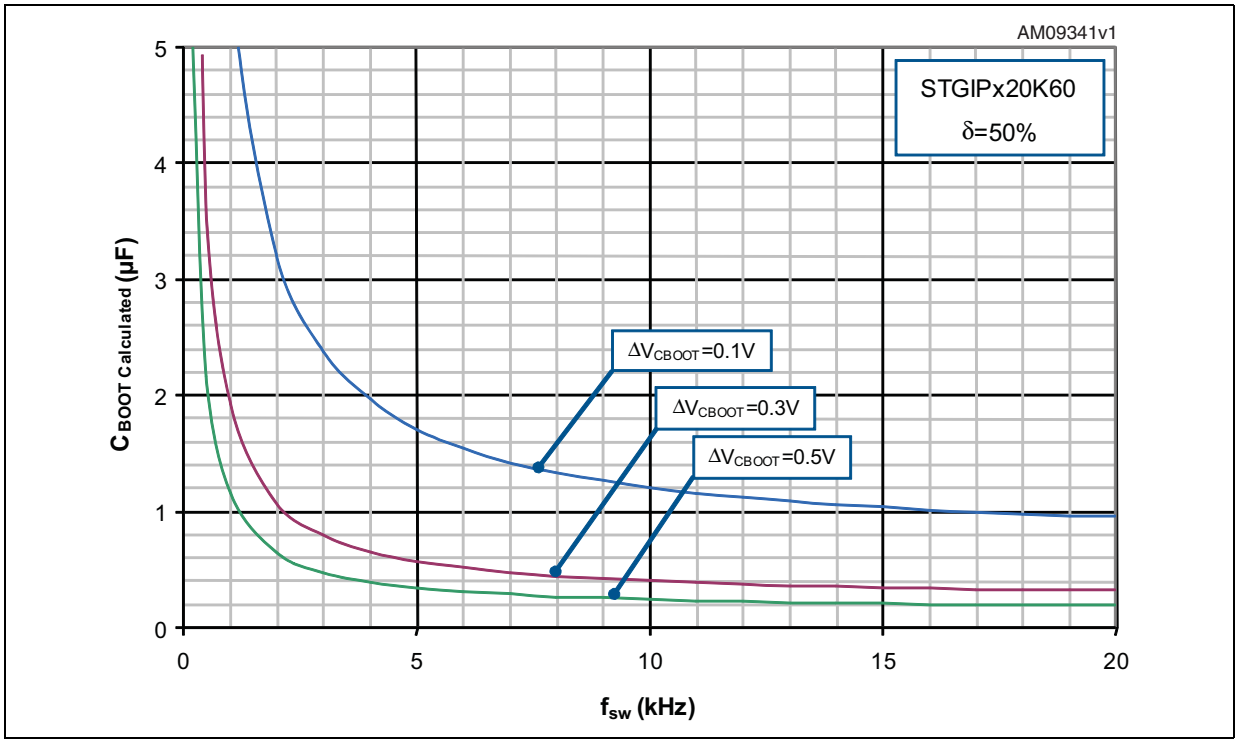
Finally, the minimum size of the bootstrap capacitor is:

Equation 14

$$C_{BOOT} = \frac{Q_{TOT}}{\Delta V_{CBOOT}}$$

For an easier selection of bootstrap capacitor, *Figure 24* shows the behavior of C_{BOOT} (calculated) versus switching frequency (f_{sw}), with different values of ΔV_{CBOOT}, corresponding to *Equation 14* for a continuous sinusoidal modulation and for STGIPS20K60 and STGIPL20K60 (worst case) and a duty cycle δ = 50%. For all the other devices the bootstrap capacitor can be calculated using the same curve.

Figure 24. Bootstrap capacitor vs. switching frequency



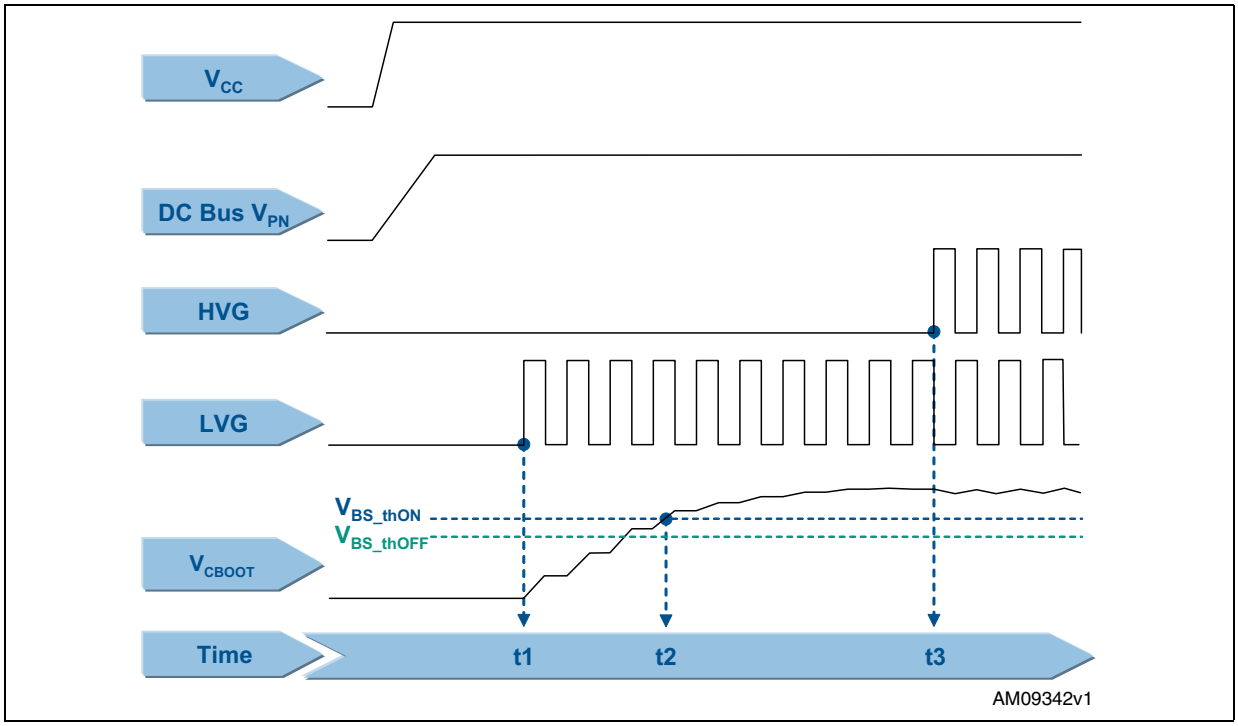
Considering the limit cases during the PWM control and further leakages and dispersions in the board layout, the capacitance value to use in the bootstrap circuit must be selected two or three times higher than the C_{BOOT} calculated in the graph of *Figure 24*. The bootstrap capacitor should be with a low ESR value for a good local decoupling, therefore, in case an electrolytic capacitor is used, a good quality (low ESR, low ESL) filter capacitor placed directly on the SLLIMM pins is strictly recommended.

2.3.14 Initial bootstrap capacitor charging

During the startup phase, the bootstrap capacitor must be charged for a suitable time to complete the initial charging time (t_{CHARGE}), which is, at least, the time V_{CBOOT} needs to exceed the turn-on undervoltage threshold V_{BS_thON}, as already stated in *Equation 12*. For a normal operation, the voltage across the bootstrap capacitor must never drop down to the turn-off undervoltage threshold V_{BS_thOFF} throughout the working conditions. For the period of startup, only the low side IGBT is switched on and, just after this phase, the PWM is run, as shown in the following steps of *Figure 25*:

- t1: the bootstrap capacitor starts to charge through the low side IGBT (LVG)
- t2: the voltage across the bootstrap capacitor (V_{CBOOT}) reaches its turn-on undervoltage threshold V_{BS_thON}.
- t3: the bootstrap capacitor is fully charged, this enables the high side IGBT and the C_{BOOT} capacitor starts to discharge in order to provide the right IGBT gate charge. The bootstrap capacitor recharges during the on state of low side IGBT (LVG).

Figure 25. Initial bootstrap charging time



The initial charging time is given by *Equation 15* and must be, for safety reasons, at least three times longer than the calculated value.

Equation 15

$$t_{CHARGE} \geq \frac{C_{BOOT} \cdot R_{DS(on)}}{\delta} * \ln\left(\frac{V_{CC}}{\Delta V_{CBOOT}}\right)$$

where δ is the duty cycle of the PWM signal and $R_{DS(on)}$ is 120 Ω typical value, as shown in the datasheet.

A practical example can be done by considering a motor drive application where the PWM switching frequency is 12.5 kHz, with a duty cycle of 50%, and ΔV_{CBOOT} = 0.1 V (that means, a gate driver supply voltage V_{CC} = 17.6 V). From the graph in *Figure 24* the bootstrap capacitance is 1.5 µF, therefore, the C_{BOOT} can be selected by using a value between 3.0 and 4.5 µF. According to the commercial value the bootstrap capacitor can be 3.3 µF. From *Equation 15*, the initial charging time is:

Equation 16

$$t_{CHARGE} \geq \frac{3.3 \cdot 10^{-6} \cdot 120}{0.5} \cdot \ln\left(\frac{17.6}{0.1}\right) = 4ms$$

For safety reasons, the initial charging time must be at least 12 ms.

3 Package

The SLLIMM benefits from a compact package while providing high power density, the best thermal performance, and great electrical isolation (> 2500 V_{RMS}).

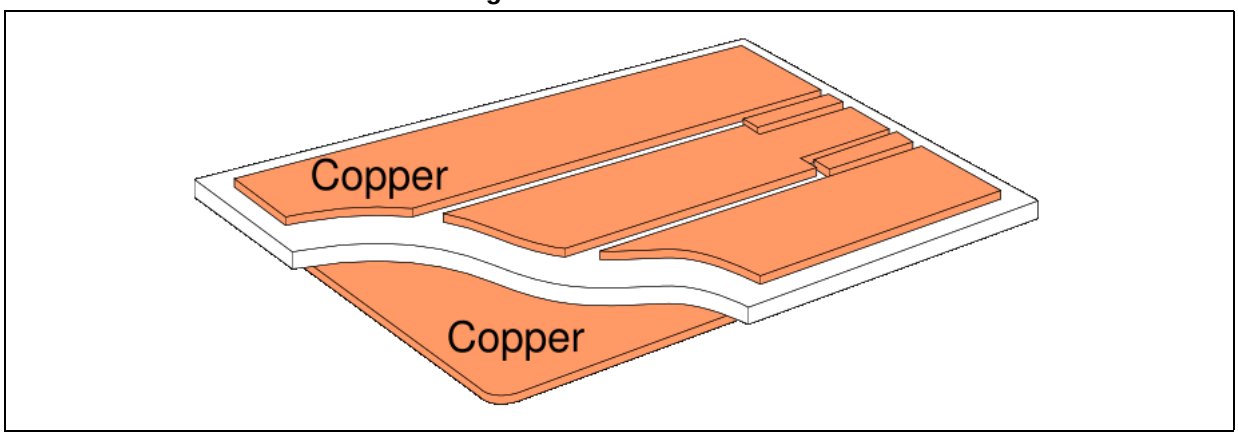
The SDIP is a dual-in-line transfer mold package, available in 25-lead version (SDIP-25L) and 38-lead version (SDIP-38L) and based on the state of the art DBC mounting technology for the power stage, whilst the control stage is assembled on a PCB layer. A vacuum soldering process is used to avoid any gas inclusion (voids) during the soldering process that could cause potential hot spots. It results in a further increase in the reliability of the SLLIMM family due to the improved thermal and electrical conductivity.

This technology makes it possible to achieve extremely low thermal resistance values, high stability in thermal cycling, small size with optimum cost-effectiveness, and quality level.

3.1 DBC substrate

DBC means direct bonded copper and denotes a process in which copper and a ceramic material are directly bonded, as shown in *Figure 26*. Direct bonded copper substrates have been proven for many years to be an excellent solution for electrical isolation and thermal management of high power semiconductor modules.

Figure 26. DCB structure



The advantages of DBC substrates are, firstly, high current-carrying capability, due to thick copper metallization, and secondly, a thermal expansion coefficient close to the silicon one at the copper surface.

DBC has two layers of copper that are directly bonded onto an aluminum-oxide (Al_2O_3) ceramic base. The DBC process yields a super-thin base and eliminates the need for thick, heavy copper bases that were used prior to this process. Because SLLIMM with DBC bases has fewer layers, it has much lower thermal resistance values than those based on different materials.

The main properties of DBC ceramic substrates

The main properties of DBC include good mechanical strength, mechanically stable shape, good adhesion and corrosion resistance, and also offer:

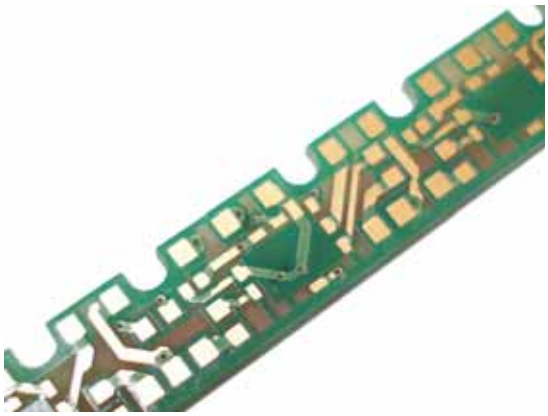
- Excellent electrical isolation
- Very good thermal conductivity
- The thermal expansion coefficient is close to that of silicon, so no interface layers are required
- Good heat spreading
- May be structured just like printed circuit boards or “IMS substrates”
- Environmentally clean

3.2 PCB

A PCB (printed circuit board) is used to mechanically support the gate driver ICs and to electrically connect those using conductive pathways.

Thanks to the internal PCB it is possible to realize various electric configurations, necessary to add advanced features, and to insert several passive components, such as resistors or capacitors, to properly bias the gate drivers. The insertion of filter capacitors, directly across the gate driver pins, improves the SLLIMM noise immunity and helps users to work in a safer condition. *Figure 27* shows the internal PCB detail.

Figure 27. PCB structure



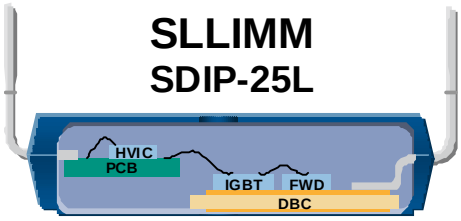
3.3 Package structure

Figure 28 and *Figure 29* contain images and an internal structure illustration of the SDIP-25L and SDIP-38L package.

Figure 28. Images and internal view of SDIP-25L package

Top view

Bottom view



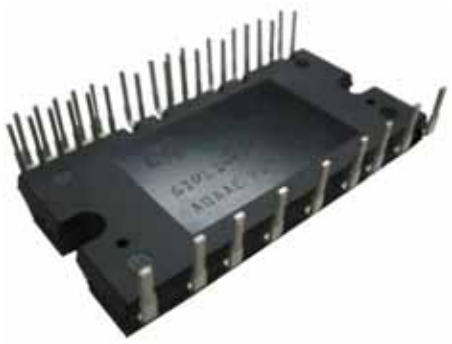
Internal view

Main dimensions

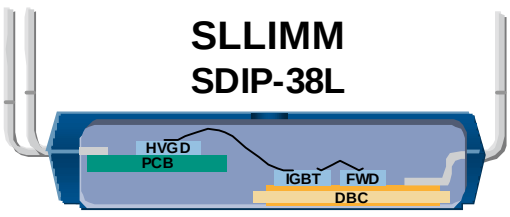
x = 44.4 mm
y_1 = 22 mm (body only)
y_2 = 25.22 mm (including leads)
z_1 = 5.4 mm (body only)
z_2 = 11.6 mm (including leads)

Figure 29. Images and internal view of SDIP-38L package

Top view



Bottom view



Internal view

Main dimensions

x = 49.6 mm
y_1 = 24.5 mm (body only)
y_2 = 29.1 mm (including leads)
z_1 = 5.4 mm (body only)
z_2 = 10.91 mm (including leads)

3.4 Package outline and dimensions

Figure 30. Outline drawing of SDIP-25L package

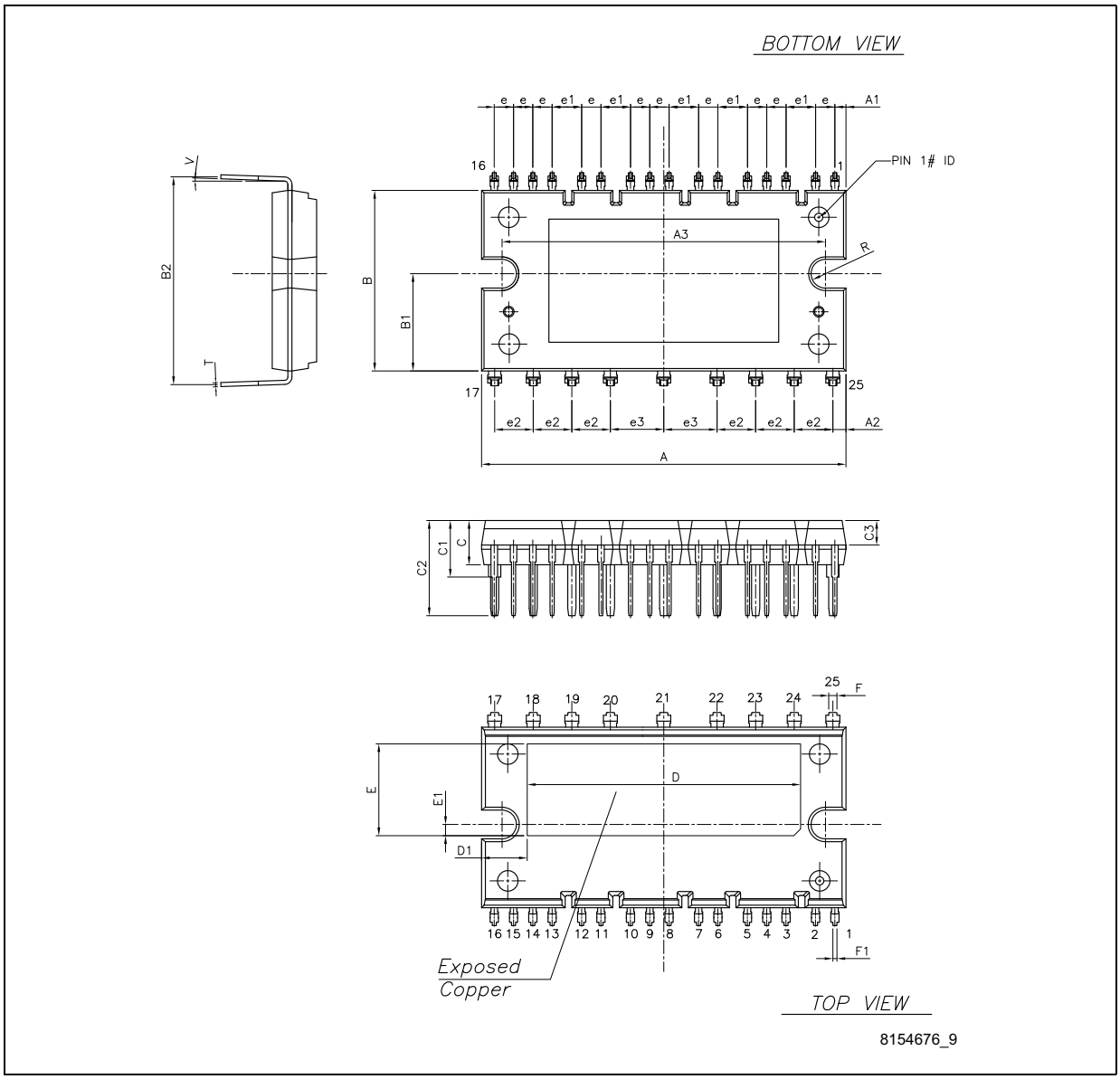


Table 9. SDIP-25L mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	43.90	44.40	44.90
A1	1.15	1.35	1.55
A2	1.40	1.60	1.80
A3	38.90	39.40	39.90
B	21.50	22.00	22.50
B1	11.25	11.85	12.45
B2	24.83	25.23	25.63
C	5.00	5.40	6.00
C1	6.50	7.00	7.50
C2	11.20	11.70	12.20
C3	2.90	3.00	3.10
e	2.15	2.35	2.55
e1	3.40	3.60	3.80
e2	4.50	4.70	4.90
e3	6.30	6.50	6.70
D		33.30	
D1		5.55	
E		11.20	
E1		1.40	
F	0.85	1.00	1.15
F1	0.35	0.50	0.65
R	1.55	1.75	1.95
T	0.45	0.55	0.65
V	0°		6°

Figure 31. Outline drawing of SDIP-38L package

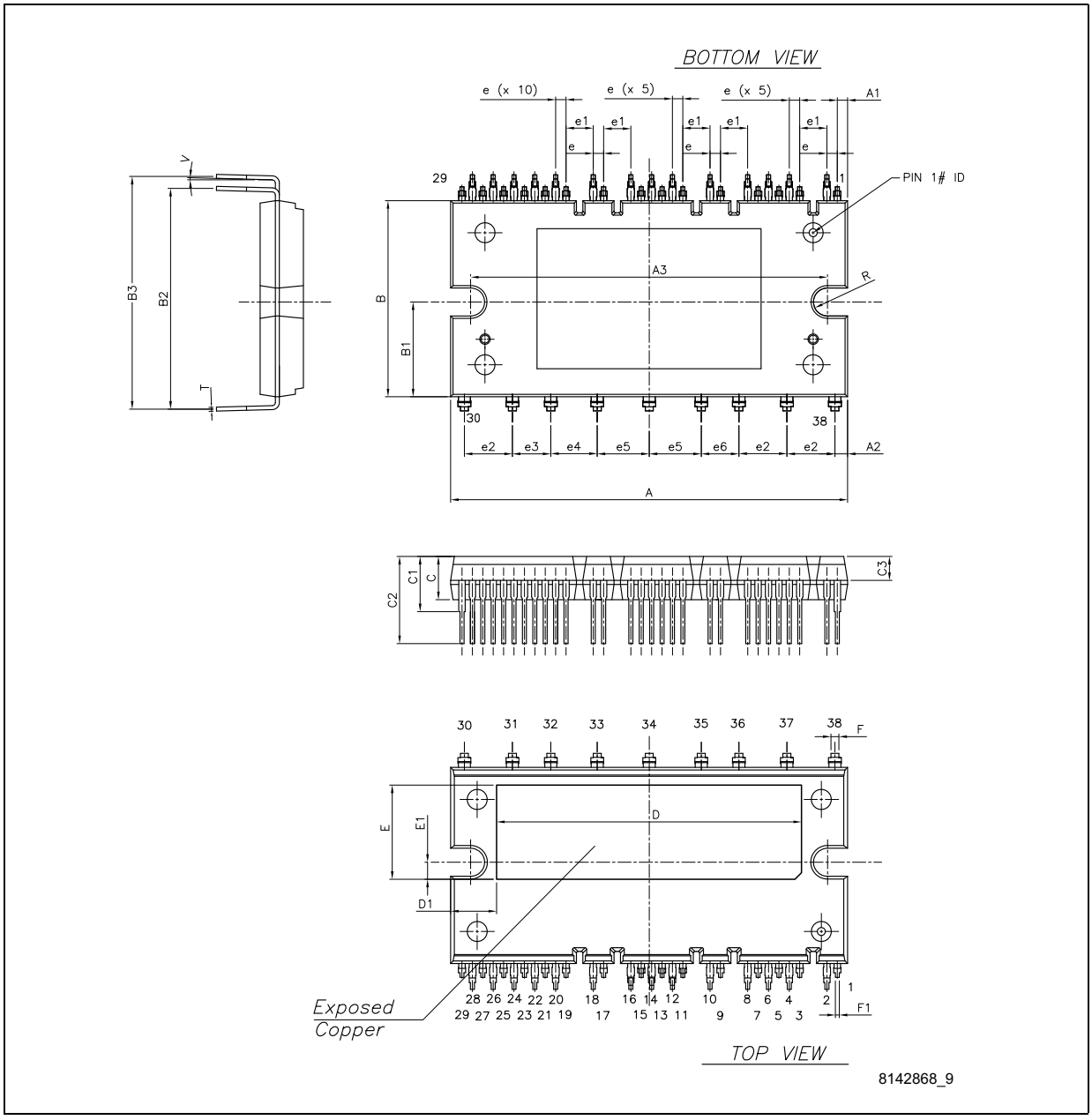


Table 10. SDIP-38L mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	49.10	49.60	50.10
A1	1.10	1.30	1.50
A2	1.40	1.60	1.80
A3	44.10	44.60	45.10
B	24.00	24.50	25.00
B1	11.25	11.85	12.45
B2	27.10	27.60	28.10
B3	28.60	29.10	29.60
C	5.00	5.40	6.00
C1	6.50	7.00	7.50
C2	10.35	10.85	11.35
C3	2.90	3.00	3.10
e	1.10	1.30	1.50
e1	3.20	3.40	3.60
e2	5.80	6.00	6.20
e3	4.60	4.80	5.00
e4	5.60	5.80	6.00
e5	6.30	6.50	6.70
e6	4.50	4.70	4.90
D		38.10	
D1		5.75	
E		11.80	
E1		2.15	
F	0.85	1.00	1.15
F1	0.35	0.50	0.65
R	1.55	1.75	1.95
T	0.45	0.55	0.65
V	0°		6°

3.5 Input and output pins description

This paragraph defines the input and output pins of SLLIMM. For a more accurate description and layout suggestions, please consult the relevant sections.

Figure 32. Pinout of SDIP-25L package (bottom view)

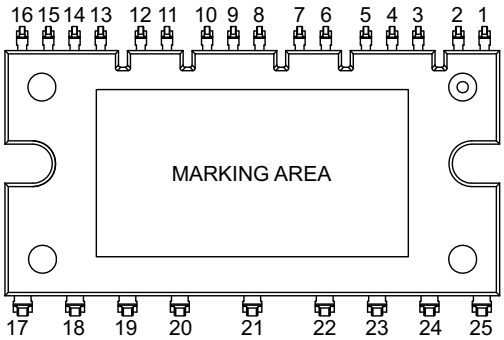


Table 11. Input and output pins of SDIP-25L package

Pin #	Name		Description	
	STGIPS10K60A	STGIPS14K60 STGIPS20K60	STGIPS10K60A	STGIPS14K60 STGIPS20K60
1	OUT_U		High side reference output for U phase	
2	V_{bootU}		Bootstrap voltage for U phase	
3	LIN_U	$\overline{LIN}_U$	Low side logic input for U phase (active high)	Low side logic input for U phase (active low)
4	HIN_U		High side logic input for U phase	
5	V_{CC}		Low voltage power supply	
6	OUT_V		High side reference output for V phase	
7	V_{bootV}		Bootstrap voltage for V phase	
8	GND		Ground	
9	LIN_V	$\overline{LIN}_V$	Low side logic input for V phase (active high)	Low side logic input for V phase (active low)
10	HIN_V		High side logic input for V phase	
11	OUT_W		High side reference output for W phase	
12	V_{bootW}		Bootstrap voltage for W phase	
13	LIN_W	$\overline{LIN}_W$	Low side logic input for W phase (active high)	Low side logic input for W phase (active low)
14	HIN_W		High side logic input for W phase	
15	T_1	$\overline{SD}$ / OD	NTC thermistor terminal 1	SD logic input (active low) / open drain (comp output)
16	T_2	CIN	NTC thermistor terminal 2	Comparator input
17	N_W		Negative DC input for W phase	
18	W		W phase output	
19	P		Positive DC input	
20	N_V		Negative DC input for V phase	

Table 11. Input and output pins of SDIP-25L package (continued)

Pin #	Name		Description	
	STGIPS10K60A	STGIPS14K60 STGIPS20K60	STGIPS10K60A	STGIPS14K60 STGIPS20K60
21	V		V phase output	
22	P		Positive DC input	
23	N_U		Negative DC input for U phase	
24	U		U phase output	
25	P		Positive DC input	

Figure 33. Pinout of SDIP-38L package (bottom view)

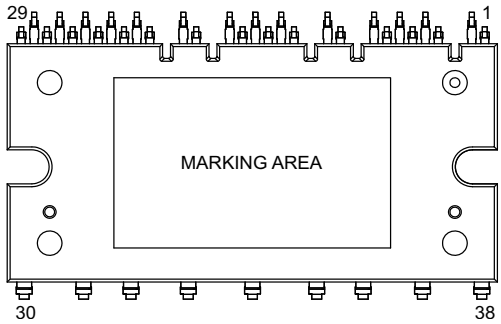


Table 12. Input and output pins of SDIP-38L package

Pin #	STGIPL14K60 STGIPL20K60	
	Name	Description
1	OUT_U	High side reference output for U phase
2	V_{bootU}	Bootstrap voltage for U phase
3	$\overline{LIN}_U$	Low side logic input for U phase (active low)
4	HIN_U	High side logic input for U phase
5	OP_{-U}	Op amp inverting input for U phase
6	OP_{OUTU}	Op amp output for U phase
7	OP_{+U}	Op amp non inverting input for U phase
8	CIN_U	Comparator input for U phase
9	OUT_V	High side reference output for V phase
10	V_{bootV}	Bootstrap voltage for V phase
11	$\overline{LIN}_V$	Low side logic input for V phase (active low)
12	HIN_V	High side logic input for V phase

Table 12. Input and output pins of SDIP-38L package (continued)

Pin #	STGIPL14K60 STGIPL20K60	
	Name	Description
13	OP_{-V}	Op amp inverting input for V phase
14	OP_{OUTV}	Op amp output for V phase
15	OP_{+V}	Op amp non inverting input for V phase
16	CIN_V	Comparator input for V phase
17	OUT_W	High side reference output for W phase
18	V_{bootW}	Bootstrap voltage for W phase
19	$\overline{LIN}_W$	Low side logic input for W phase (active low)
20	HIN_W	High side logic input for W phase
21	OP_{-W}	Op amp inverting input for W phase
22	OP_{OUTW}	Op amp output for W phase
23	OP_{+W}	Op amp non inverting input for W phase
24	CIN_W	Comparator input for W phase
25	V_{CC}	Low voltage power supply
26	$\overline{SD}$ / OD	Shutdown logic input (active low) / open drain (comparator output)
27	GND	Ground
28	T_2	NTC thermistor terminal 2
29	T_1	NTC thermistor terminal 1
30	N_W	Negative DC input for W phase
31	W	W phase output
32	P	Positive DC input
33	N_V	Negative DC input for V phase
34	V	V phase output
35	P	Positive DC input
36	N_U	Negative DC input for U phase
37	U	U phase output
38	P	Positive DC input

High-Side bias voltage pins /high-side bias voltage reference

Pins: V_{bootU}-OUT_U, V_{bootV}-OUT_V, V_{bootW}-OUT_W

- The bootstrap section is designed to realize a simple and efficient floating power supply, in order to provide the gate voltage signal to the high-side IGBTs.
- The SLLIMM family integrates the bootstrap diodes. This helps customer to save cost, board space, and number of components.
- The advantage of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs.
- Each bootstrap capacitor is charged from the V_{CC} supply during the on-state of the corresponding low side IGBT.
- To prevent malfunctions caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.
- The value of bootstrap capacitors is strictly related to the application conditions. Please consult *Section 2.3.12: Bootstrap circuit*.

Gate driver bias voltage

Pin: V_{CC}

- Control supply pin for the built-in ICs.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to this pin.

Gate drive supply ground

Pin: GND

- Ground reference pin for the built-in ICs.
- To avoid noise influences, the main power circuit current should not be allowed to flow through this pin (see *Section 5.1: Layout suggestions*).

Signal input

Pins: HIN_U, HIN_V, HIN_W; LIN_U, LIN_V, LIN_W; $\overline{LIN}_U$, $\overline{LIN}_V$, $\overline{LIN}_W$

- These pins control the operation of the built-in IGBTs.
- The signal logic of HIN_U, HIN_V, HIN_W, LIN_U, LIN_V, and LIN_W pins is active high. The IGBT associated with each of these pins is turned on when a sufficient logic (higher than a specific threshold) voltage is applied to these pins.
- The signal logic of $\overline{LIN}_U$, $\overline{LIN}_V$, $\overline{LIN}_W$ pins is active low. The IGBT associated with each of these pins is turned on when a logic voltage (lower than a specific threshold voltage) is applied to these pins.
- The wiring of each input should be as short as possible to protect the SLLIMM against noise influences.

Internal comparator non-inverting

Pins: CIN_U, CIN_V, CIN_W

- The current sensing shunt resistor, connected on each phase leg, could be used by the internal comparator (pins CIN_U, CIN_V and CIN_W) to detect short-circuit current.
- The shunt resistor should be selected to meet the detection levels matched for the specific application.
- An RC filter (typically ~ 1 µs) should be connected to the CIN_U, CIN_V, CIN_W pins to eliminate noise.
- The connection length between the shunt resistor and CIN_U, CIN_V, CIN_W pins should be minimized.
- If a voltage signal, higher than the specified V_{REF} (see datasheet), is applied to this pin, the SLLIMM automatically shuts down and the $\overline{SD}$ / OD pin is pulled down (to inform the microcontroller).

Shutdown / open drain

Pin: $\overline{SD}$ / OD

- The $\overline{SD}$ / OD pin works as an enable/disable pin.
- The signal logic of the $\overline{SD}$ / OD pin is active low. The SLLIMM shuts down if a voltage lower than a specific threshold is applied to this pin, leading each half bridge in tri-state.
- The $\overline{SD}$ / OD status is connected also to the internal comparator status (*Section 2.3.6: Short-circuit protection and smart shutdown function*). When the comparator triggers, the SD / OD pin is pulled down acting as a FAULT pin.
- The $\overline{SD}$ / OD, when pulled down by the comparator, is open drain configured. The SD / OD voltage should be pulled up to the 3.3 V or 5 V logic power supply through a pull-up resistor.

Thermistor

Pins: T_1, T_2

- A co-packaged NTC is available for temperature monitor purposes.
- A simple voltage divider (as shown in *Section 2.3.10: Overtemperature protection*) can be realized with an external resistor in order to realize a temperature dependent voltage signal.
- The NTC is not able to sense IGBT junction temperature fast variation (due to its slow dynamic).

Integrated operational amplifier (only for STGIPL14K60 and STGIPL20K60)

Pins: $OP\text{-}_U$, $OP\text{-}_V$, $OP\text{-}_W$; OP_{OUTU}, OP_{OUTV}, OP_{OUTW}; OP_U, OP_V, OP_W

- The op amps are completely uncommitted.
- The op amps performances are optimized for advanced control technique (FOC).
- Thanks to the integrated op amps it is possible to realize compact and efficient board layout, minimizing the required BOM list.

Positive DC-link

Pin: P

- These are three DC-link positive power supply pins of the inverter, which offer designers more flexibility in their approach. They are internally connected to the collectors of the high-side IGBTs.
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect decoupling capacitors close to this pin and power ground (typically, high frequency, high voltage, non-inductive capacitors of about 0.1 or 0.22 µF are used).

Negative DC-link

Pins: N_U, N_V, N_W

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low side IGBT emitters of each phase.
- The power ground of the application should be separated from the logic ground of the system and they should be reconnected at one specific point (star connection).

Inverter power output

Pins: U, V, W

- Inverter output pins for connecting to the inverter load (e.g. motor).

4 Power losses and dissipation

The total power losses in an inverter are comprised of conduction losses, switching losses, and off-state losses and they are essentially generated by the power devices of the inverter stage, such as the IGBTs and the freewheeling diodes. The conduction losses (P_{cond}) are the on-state losses during the conduction phase. The switching losses (P_{sw}) are the dynamic losses encountered during the turn-on and the turn-off. The off-state losses, due to the blocking voltage and leakage current, can be neglected.

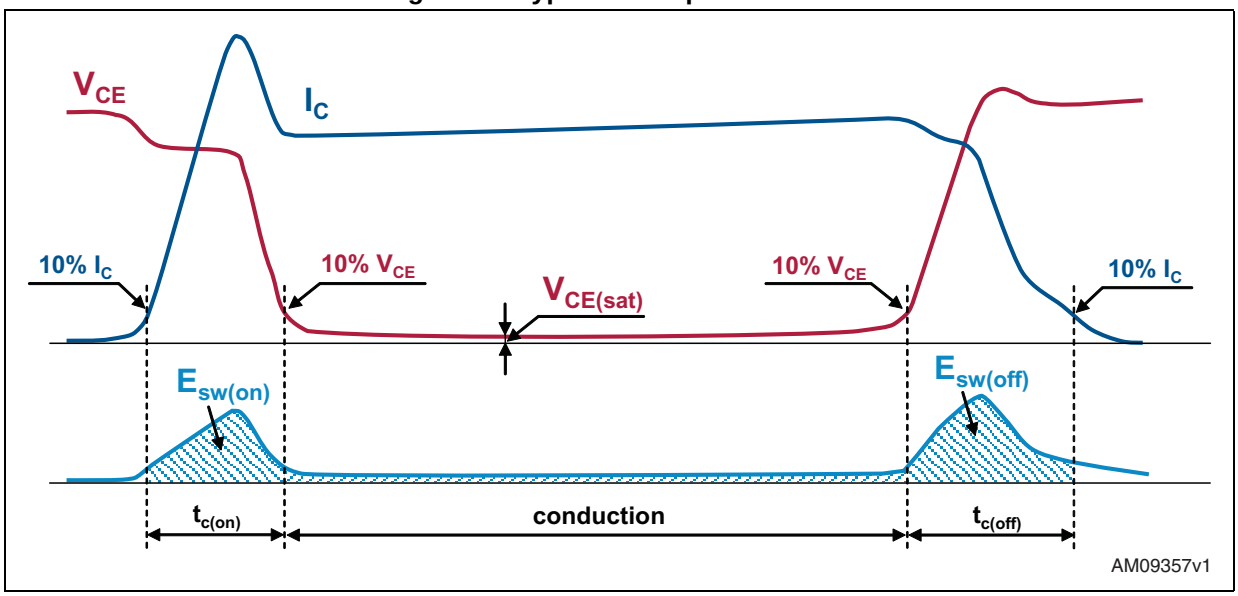
Finally, the total power losses are given by:

Equation 17

$$P_{tot} \approx P_{cond} + P_{sw}$$

Figure 34 shows a typical waveform of an inductive hard switching application such as a motor drive, where the major sources of power losses are specified.

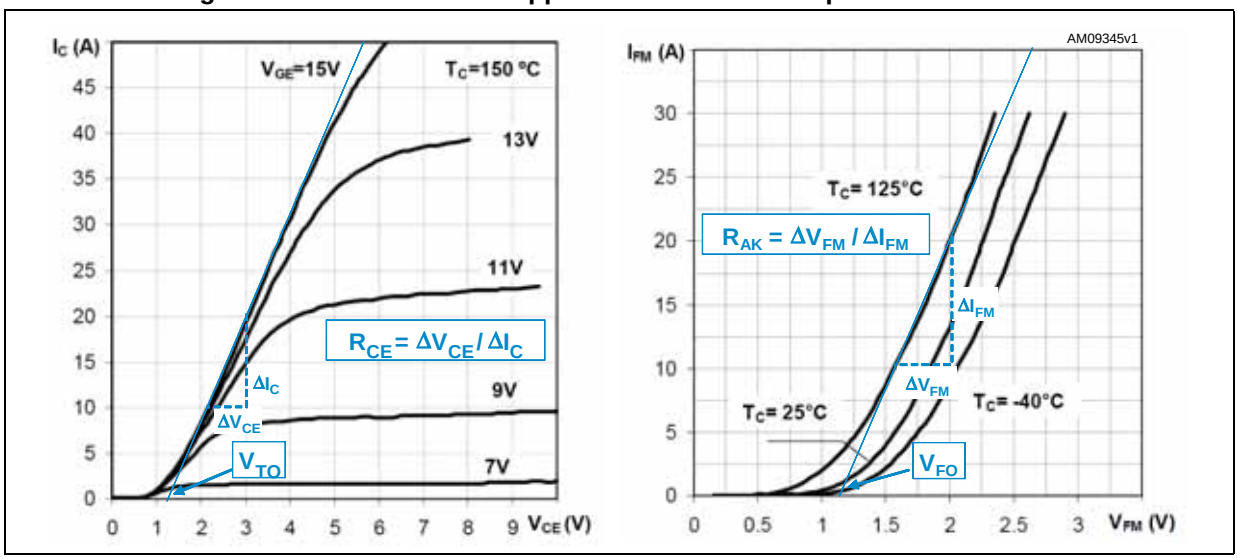
Figure 34. Typical IGBT power losses



4.1 Conduction power losses

The conduction losses are caused by IGBT and freewheeling diode forward voltage drop at rated current. They can be calculated using a linear approximation of the forward characteristics for both IGBT and diode, having a series connection of DC voltage source representing the threshold voltage, V_{TO} for IGBT, (and V_{FO} for diode) and a collector emitter on-state resistance, R_{CE}, (and anode cathode on-state resistance, R_{AK}), as shown in *Figure 35*, for reference.

Figure 35. IGBT and diode approximation of the output characteristics



Both forward characteristics are temperature dependent, and so must be considered under a specified temperature.

The linear approximations can be translated for IGBT in the following equation:

Equation 18

$$v_{ce}(i_c) = V_{TO} + R_{CE} \cdot i_c$$

and, for freewheeling diode:

Equation 19

$$v_{fm}(i_{fm}) = V_{FO} + R_{AK} \cdot i_{fm}$$

The conduction losses of IGBT and diode can be derived as the time integral of the product of conduction current and voltage across the devices, as follows:

Equation 20

$$P_{cond\_IGBT} = \frac{1}{T}\int_0^T v_{ce} \cdot i_c(t)dt = \frac{1}{T}\int_0^T \left(V_{TO} \cdot i_c(t) + R_{ce} \cdot i_c^2(t)\right)dt$$

Equation 21

$$P_{cond\_Diode} = \frac{1}{T}\int_0^T v_f \cdot i_f(t)dt = \frac{1}{T}\int_0^T \left(V_{FO} \cdot i_f(t) + R_{AK} \cdot i_f^2(t)\right)dt$$

where T is the fundamental period.

The different utilization mode of SLLIMM, modulation technique, and working conditions make the power losses very difficult to estimate, it is therefore necessary to fix some starting points.

Assuming that:

1. the application is a variable voltage variable frequency (VVVF) inverter based on sinusoidal PWM technique
2. the switching frequency is high and therefore the output currents are sinusoidal
3. the load is ideal inductive.

Under these conditions, the output inverter current is given by:

Equation 22

$$i = \hat{I}\cos(\theta - \phi)$$

where $\hat{I}$ is the current peak, θ stands for ωt and ϕ is the phase angle between output voltage and current.

The conduction power losses can be obtained as:

Equation 23

$$P_{cond\_IGBT} = \frac{V_{TO}\cdot\hat{I}}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}\xi\cos(\theta-\phi)d\theta + \frac{R_{CE}\cdot\hat{I}^2}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}\xi\cos^2(\theta-\phi)d\theta$$

Equation 24

$$P_{cond\_Diode} = \frac{V_{FO}\hat{I}}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}(1-\xi)\cos(\theta-\phi)d\theta + \frac{R_{AK}\hat{I}^2}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}(1-\xi)\cos^2(\theta-\phi)d\theta$$

where ξ is the duty cycle for this PWM technique and is given by:

Equation 25

$$\xi = \frac{1+m_a\cdot\cos\theta}{2}$$

and m_a is the PWM amplitude modulation index.

Finally, solving *Equation 23* and *Equation 24*, we have:

Equation 26

$$P_{cond\_IGBT} = V_{TO}\cdot\hat{I}\left(\frac{1}{2\pi}+\frac{m_a\cdot\cos\phi}{8}\right) + R_{CE}\cdot\hat{I}^2\left(\frac{1}{8}+\frac{m_a\cdot\cos\phi}{3\pi}\right)$$

Equation 27

$$P_{cond\_Diode} = V_{FO}\cdot\hat{I}\left(\frac{1}{2\pi}+\frac{m_a\cdot\cos\phi}{8}\right) + R_{AK}\cdot\hat{I}^2\left(\frac{1}{8}+\frac{m_a\cdot\cos\phi}{3\pi}\right)$$

and therefore, the conduction power losses of one device (IGBT and diode) are:

Equation 28

$$P_{cond} = P_{cond\_IGBT} + P_{cond\_Diode}$$

Of course, the total conduction losses per inverter are six times this value.

4.2 Switching power losses

The switching loss is the power consumption during the turn-on and turn-off transients. As already shown in *Figure 34*, it is given by the pulse of power dissipated during the turn-on (t_{on}) and turn-off (t_{off}). Experimentally, it can be calculated by the time integral of product of the collector current and collector-emitter voltage for the switching period. Anyway, the dynamic performances are strictly related to many parameters such as voltage and current, temperature, so it is necessary to use the same assumptions of conduction power losses (*Section 4.1: Conduction power losses*) to simplify the calculations.

Under these conditions, the switching energy losses are given by:

Equation 29

$$E_{on}(\theta) = \hat{E}_{on}\cos(\theta - \phi)$$

Equation 30

$$E_{off}(\theta) = \hat{E}_{off}\cos(\theta - \phi)$$

where $\hat{E}_{on}$ and $\hat{E}_{off}$ are the maximum values taken at T_{jmax} and $\hat{I}_c$, θ stands for ωt and ϕ is the phase angle between output voltage and current.

Finally, the switching power losses per device depend on the switching frequency (f_{sw}) and are calculated as follows:

Equation 31

$$P_{sw} = \frac{1}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi}(E_{IGBT} + E_{Diode})\cdot f_{sw}\,d\theta = \frac{(E_{IGBT} + E_{Diode})\cdot f_{sw}}{\pi}$$

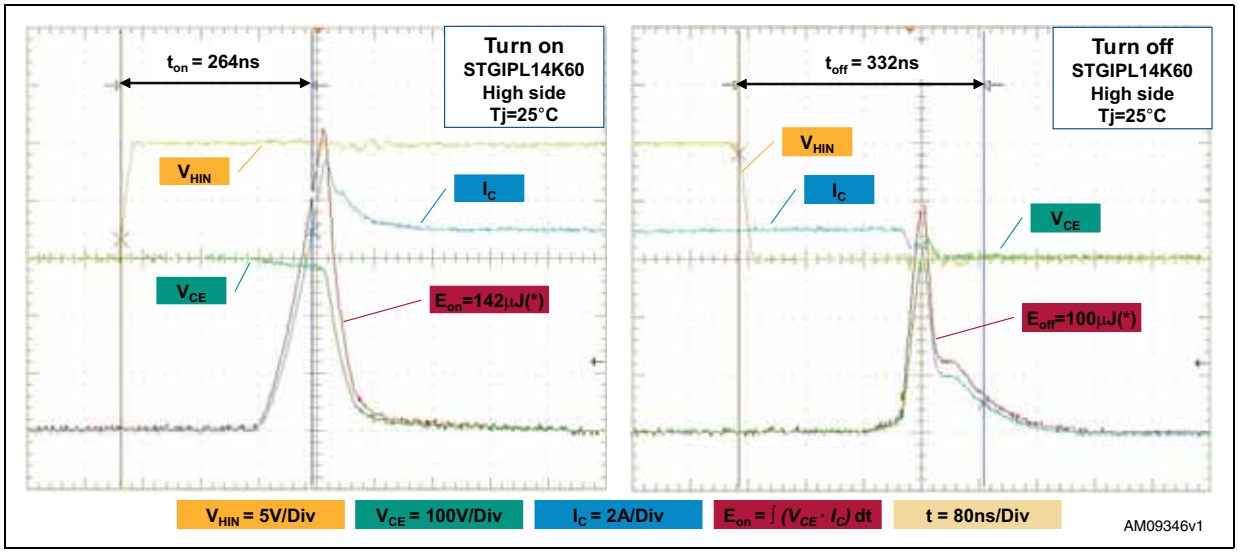
where E_{IGBT} and E_{Diode} are the total switching energy for IGBT and freewheeling diode, respectively. Also in this case, the total switching losses per inverter are six times this value.

Figure 36 shows the real turn-on and turn-off waveforms of STGIPL14K60 under the following conditions:

- V_{PN} = 300 V, I_C = 7 A, T_j = 25 °C with inductive load on full bridge topology, taken on the high side IGBT.

The red plots represent instantaneous power as a result of I_C (in blue) and V_{CE} (in green) waveforms multiplication, during the switching transitions. The areas under these plots are the switching energies computed by graphic integration thanks to the digital oscilloscope.

Figure 36. Typical switching waveforms of STGIPL14K60



E_{on} and E_{off} are the areas under the red plots.

4.3 Thermal impedance overview

During operation, power losses generate heat which elevates the temperature in the semiconductor junctions contained in the SLLIMM, limiting its performance and lifetime. To ensure safe and reliable operation, the junction temperature of power devices must be kept below the limits defined in the datasheet, therefore, the generated heat must be conducted away from the power chips and into the environment using an adequate cooling system. The most common schemes are based on one heatsink designed for free conventional air flow or, in some cases, for forced air operation. Free conventional air flow systems require bigger heatsinks (about 50% more) than a forced air based heatsink, for a given thermal resistance. Therefore, the choice of the cooling system becomes the starting point for the application designer and the thermal aspect of the system is one of the key factors in designing high efficiency and high reliability equipment. In this environment the package and its thermal resistance play a fundamental role.

Thermal resistance quantifies the capability of a given thermal path to transfer heat in the steady-state and it generically is given as the ratio between the temperature increase above the reference and the relevant power flow:

Equation 32

$$R_{th} = \frac{\Delta T}{\Delta P}$$

The thermal resistance specified in the datasheet is the junction-case $R_{th(j\text{-}c)}$ which is defined as the difference in temperature between junction and case reference divided by the power dissipation per device:

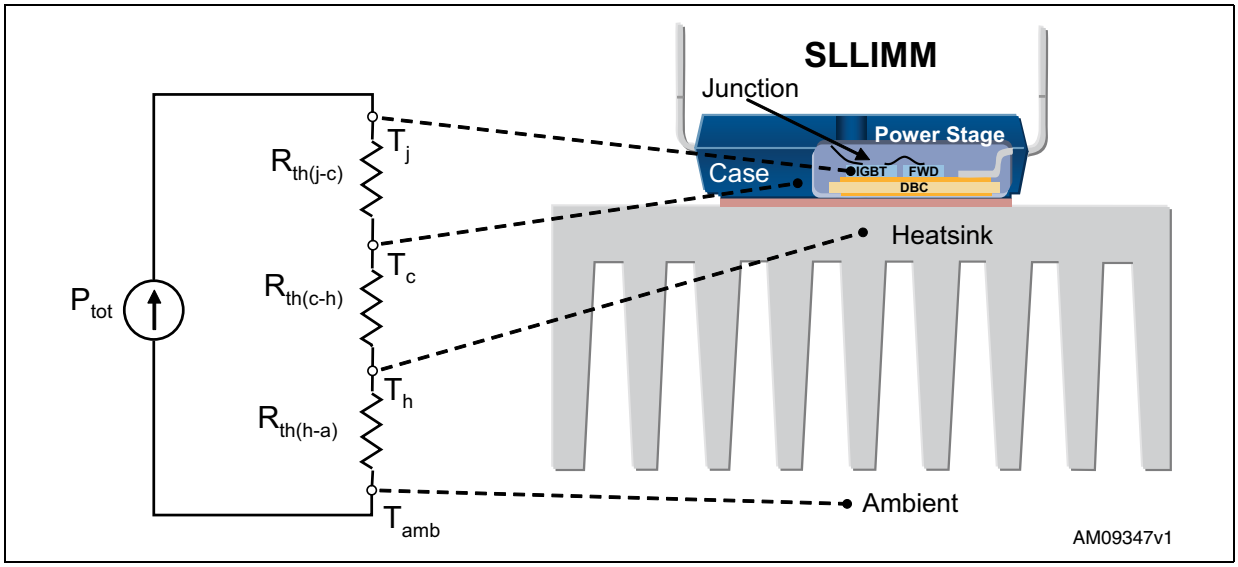
Equation 33

$$R_{th(j-c)} = \frac{T_j - T_c}{P_D}$$

The SLLIMM family benefits from the state of the art DBC substrate and therefore offers a very low $R_{th(j-c)}$ value. The backside of the DBC substrate is used as the cooling interface to the heatsink. Thermal grease or another thermal interface material between the DBC and the heatsink is used to reduce the thermal resistance of the interface ($R_{th(c-h)}$) and, of course, it depends of the material and its thickness.

Basically, the sum of the three thermal resistance components mentioned above gives the thermal resistance between junction and ambient $R_{th(j-a)}$, as shown in *Figure 37*.

Figure 37. Equivalent thermal circuit with heatsink single IGBT



As the power loss P_{tot} is cyclic, also the transient thermal impedance must be considered. It is defined as the ratio between the time dependent temperature increase above the reference, $\Delta T(t)$, and the relevant heat flow:

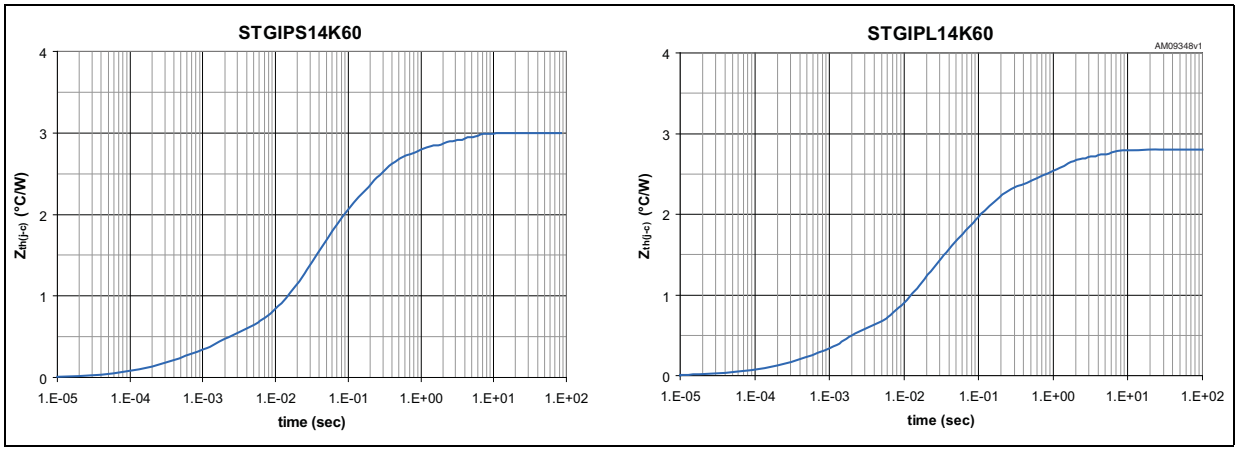
Equation 34

$$Z_{th}(t) = \frac{\Delta T(t)}{\Delta P}$$

Contrary to that already seen, regarding the thermal resistance, the thermal impedance is typically represented by an RC equivalent circuit. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature and therefore the advantage of this behavior is the short-term overload capability of the SLLIMM.

For example, *Figure 38* shows thermal impedance from junction to case curves of STGIPS14K60 (in SDIP-25L package) and STGIPL14K60 (in SDIP-38L package). As per all the other SLLIMM curves, the thermal impedance reaches saturation in about 10 seconds.

Figure 38. Thermal impedance curves (STGIPS14K60 and STGIPL14K60)



More generally, in the case of the device, power is time dependent too. The device temperature can be calculated by using the convolution integral method applied to *Equation 34Equation 34*, as follows:

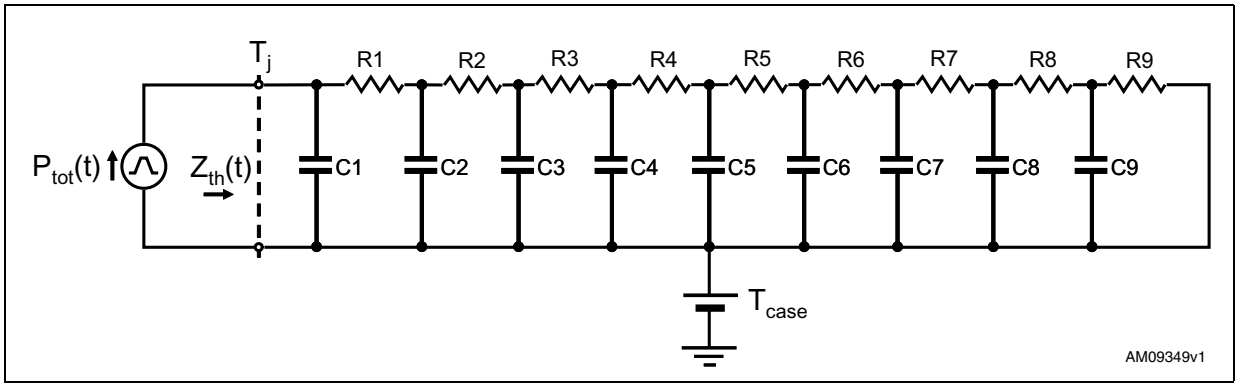
Equation 35

$$\Delta T(t) = \int_0^t Z_{th}(t-\tau)\cdot P(\tau)d\tau$$

An alternative method, very useful for the simulator tools, is the transient thermal impedance model, which provides a simple method to estimate the junction temperature rise under a transient condition.

By using the thermo-electrical analogy, the transient thermal impedance $Z_{th}(t)$ can be transformed into an electrical equivalent RC network. The number of RC sections increases the model details, therefore a ninth order model, based on the Cauer network, has been used in order to improve the accuracy of the model, as shown the *Figure 39*.

Figure 39. Thermal impedance RC Cauer thermal network



Temperatures inside the electrical RC network represent voltages, power flows represent currents, electrical resistances and capacitances represent thermal resistances and capacitances respectively. The case temperature is represented with a DC voltage source and can be interpreted as the initial junction temperature.

Transient thermal impedance models are derived by curve fitting an equation to the measured data. Values for the individual resistors and capacitors are the variables from that equation and are defined device by device in *Table 13*.

Table 13. RC Cauer thermal network elements by device

Element	STGIPS10K60A	STGIPS14K60	STGIPL14K60	STGIPS20K60	STGIPL20K60
R1 (°C/W)	8.80E-02	1.61E-02	8.15E-03	1.00E-04	3.85E-03
R2 (°C/W)	1.54E-02	9.42E-02	1.07E-01	5.00E-03	1.50E-02
R3 (°C/W)	3.16E-01	1.20E-02	5.00E-02	7.00E-02	5.17E-03
R4 (°C/W)	3.96E-03	3.50E-01	2.00E-01	1.03E-02	4.68E-02
R5 (°C/W)	8.16E-01	5.86E-01	6.57E-01	6.00E-01	4.18E-01
R6 (°C/W)	4.32E-01	1.58E-03	1.00E-02	1.15E-01	6.71E-02
R7 (°C/W)	1.23E-02	7.50E-01	8.00E-01	1.00E-03	1.27E-01
R8 (°C/W)	4.48E-01	1.60E-02	2.00E-02	1.00E-01	6.14E-01
R9 (°C/W)	1.66E+00	1.10E+00	9.50E-01	1.50E+00	0.90E+00
C1 (W·sec/°C)	3.20E-04	9.20E-04	1.00E-03	1.80E-03	1.50E-03
C2 (W·sec/°C)	6.30E-04	9.07E-05	9.96E-05	3.09E-05	9.82E-05
C3 (W·sec/°C)	9.00E-05	1.00E-03	9.59E-05	8.94E-05	9.62E-05
C4 (W·sec/°C)	5.00E-04	4.14E-05	1.85E-05	9.29E-05	9.48E-05
C5 (W·sec/°C)	5.00E-03	1.40E-02	9.68E-03	1.20E-02	9.97E-03
C6 (W·sec/°C)	1.20E-02	3.57E-05	2.00E-02	7.04E-05	7.86E-05
C7 (W·sec/°C)	1.49E-03	3.00E-03	1.76E-03	2.93E-04	2.91E-03
C8 (W·sec/°C)	8.09E-04	5.75E-04	8.27E-04	9.43E-04	5.50E-02
C9 (W·sec/°C)	1.20E-01	1.54E-01	5.00E-01	1.00E-01	6.21E-02

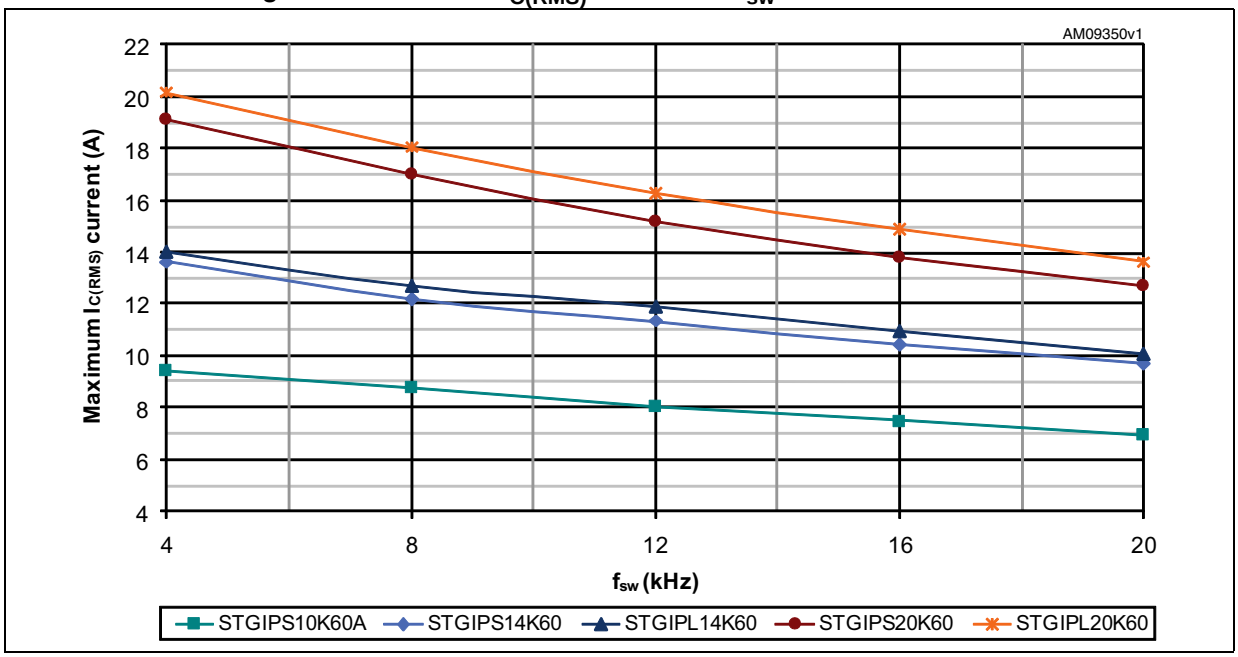
4.4 Power losses calculation example

As a result of power loss calculation and thermal aspects, fully treated in the previous sections, we are able to simulate the maximum $I_{C(RMS)}$ current versus switching frequency curves for a VVVF inverter using a 3-phase continuous PWM modulation to synthesize sinusoidal output currents.

The curves graphed in *Figure 40* represent the maximum current managed by SLLIMM in safety conditions, when the junction temperature rises to the maximum junction temperature of 150 °C and case temperature is 100 °C, which is a typical operating condition to guarantee the reliability of the system. These curves, functions of the motor drive typology and control scheme, are simulated under the following conditions:

- V_{PN} = 300 V, m_a = 0.8, cos = 0.6, T_j = 150 °C, T_c = 100 °C, f_{SINE} = 60 Hz, max. value of $R_{th(j-c)}$, typical $V_{CE(sat)}$ and E_{tot} values.

Figure 40. Maximum $I_{C(RMS)}$ current vs. f_{sw} simulated curves



5 Design and mounting guidelines

In this section the main layout suggestions for an optimized design and major mounting recommendations, to appropriately handle and assemble the SLLIMM family, are introduced.

5.1 Layout suggestions

Optimization of PCB layout for high voltage, high current and high switching frequency applications is a critical point. PCB layout is a complex matter as it includes several aspects, such as length and width of track and circuit areas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements in the PCB area.

A good layout can help the application to properly function and achieve expected performance. On the other hand, PCB without a careful layout can generate EMI issues (both induced and perceived by the application), can provide overvoltage spikes due to parasitic inductances along the PCB traces, and can produce higher power loss and even malfunction in the control and sensing stages.

The compactness of the SLLIMM solution, which offers optimized gate driving network and reduced parasitic elements, allows designers to focus only on some specific issues, such as the ground issue or noise filter. Anyhow, in order to avoid all the aforementioned conditions, the following general guidelines and suggestions must be followed in PCB layout for 3-phase applications.

5.1.1 General suggestions

- PCB traces should be designed to be as short as possible and the area of the circuit (power or signal) should be minimized to avoid the sensitivity of such structures to surrounding noise.
- Ensure a good distance between switching lines with high voltage transitions and the signal line sensitive to electrical noise. Specifically, the tracks of each OUT phase, bringing significant currents and high voltages, should be separated from the logic lines and analog sensing circuit of op amps and comparators.
- Place the R_{SENSE} resistors as close as possible to the low side pins of the SLLIMM (N_U, N_V and N_W). Parasitic inductance can be minimized by connecting the ground line (also called driver ground) of the SLLIMM directly to the cold terminal of sense resistors. Use of a low inductance type resistor, such as an SMD resistor instead of long-lead type resistors, can help to further decrease the parasitic inductance.
- Avoid any ground loop. Only a single path must connect two different ground nodes.
- Place each RC filter as close as possible to the SLLIMM pins in order to increase their efficiency.
- In order to prevent surge destruction, the wiring between the decoupling capacitor and the P pin and power ground should be as short as possible. The use of a high

frequency, high voltage non-inductive capacitor about 0.1 or 0.22 µF between the P and N pins is recommended.

- Fixed voltage tracks, such as GND or HV lines, can be used to shield the logic and analog lines from the electrical noise produced by the switching lines (e.g. OUT_U, OUT_V and OUT_W).
- Generally it is recommended to connect each half bridge ground in a star configuration and the three R_{SENSE} very close to each other and to the power ground.

In *Figure 41* and *Figure 42* the general suggestions for all SLLIMM products are summarized.

Figure 41. General suggestions 1

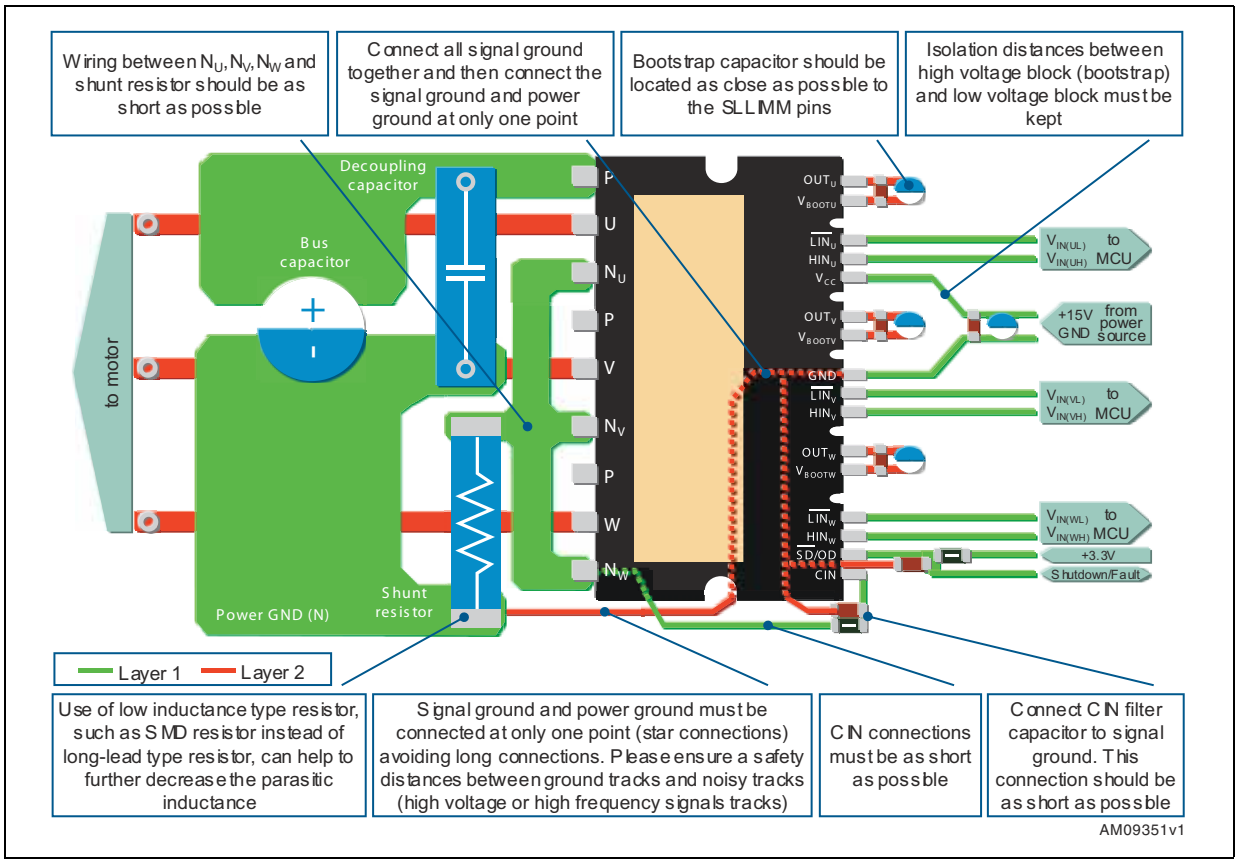
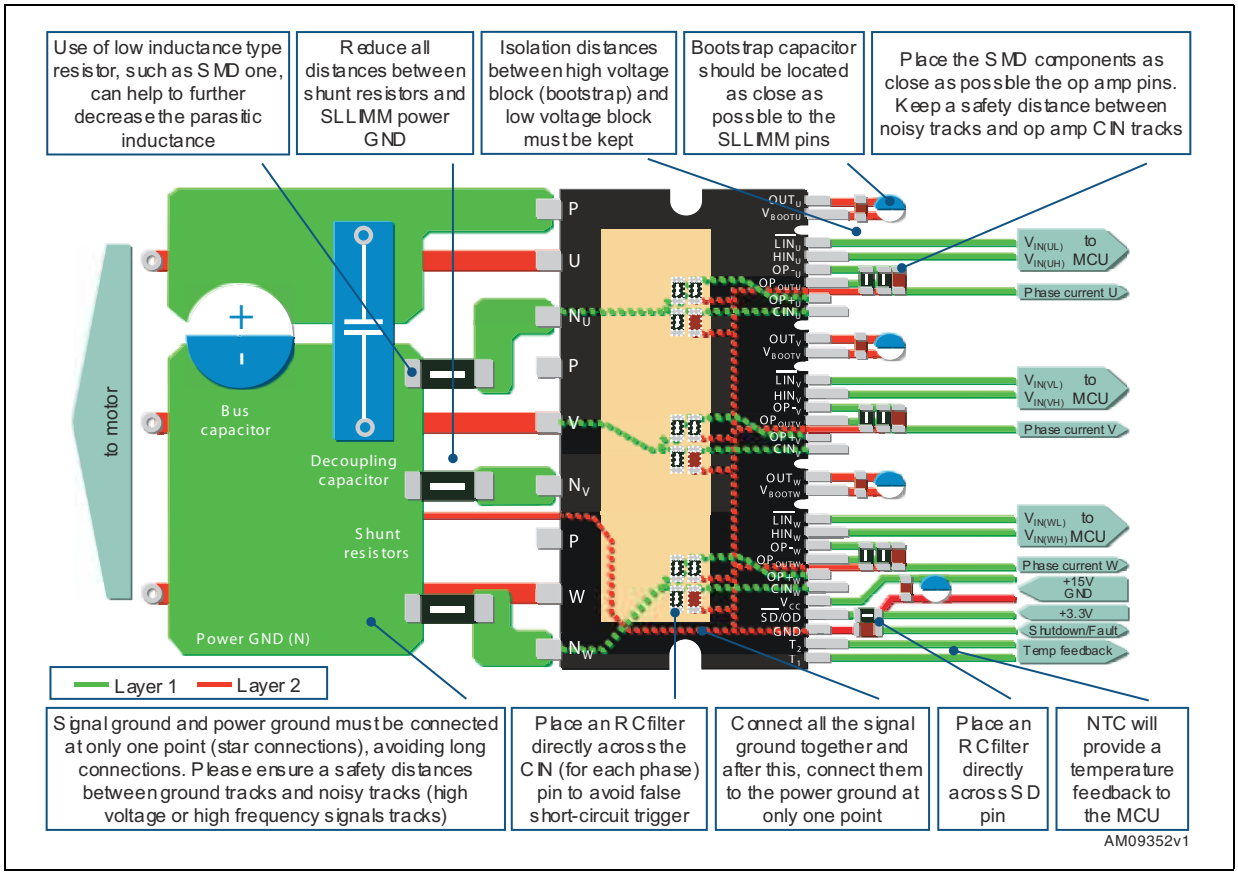


Figure 42. General suggestions 2



Special attention must be paid to some wrong layouts. In *Figure 43* and *Figure 44* some common PCB mistakes are shown.

Figure 43. Example 1 of a possible wrong layout

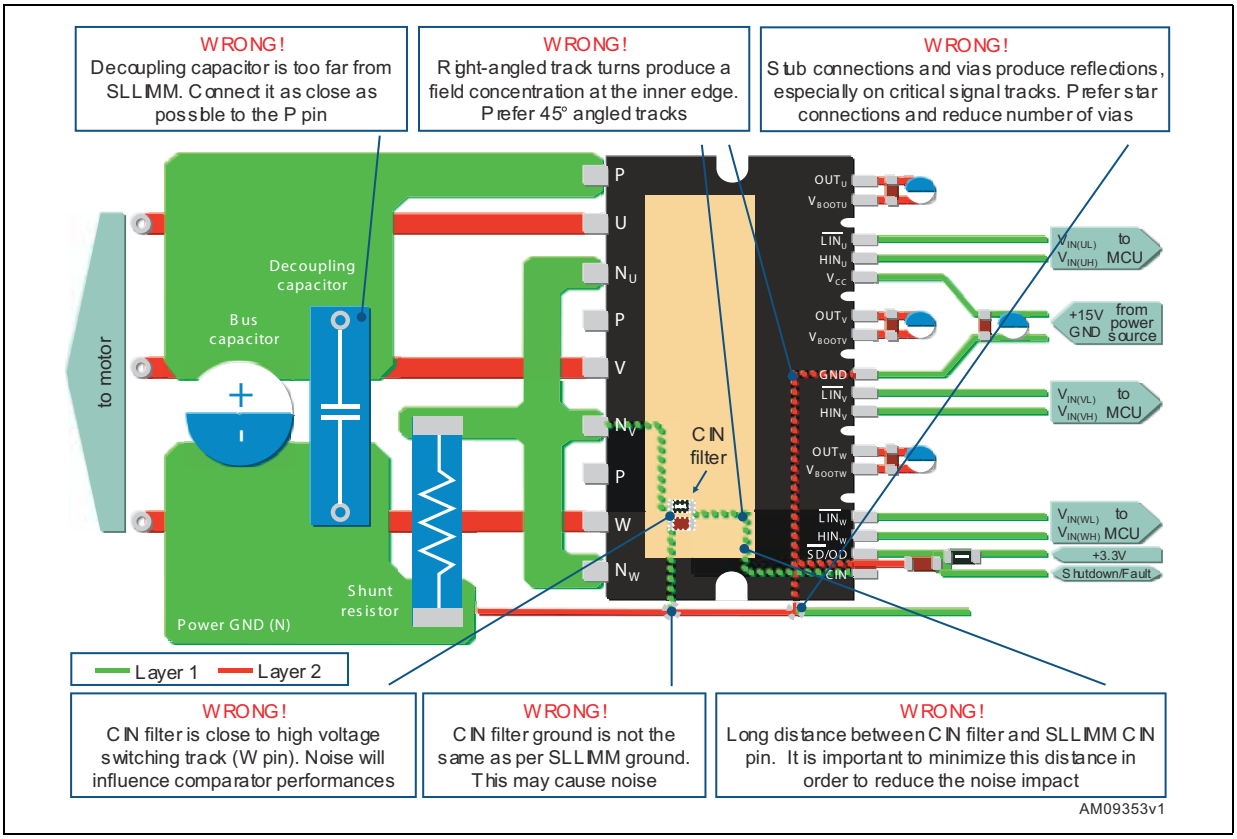
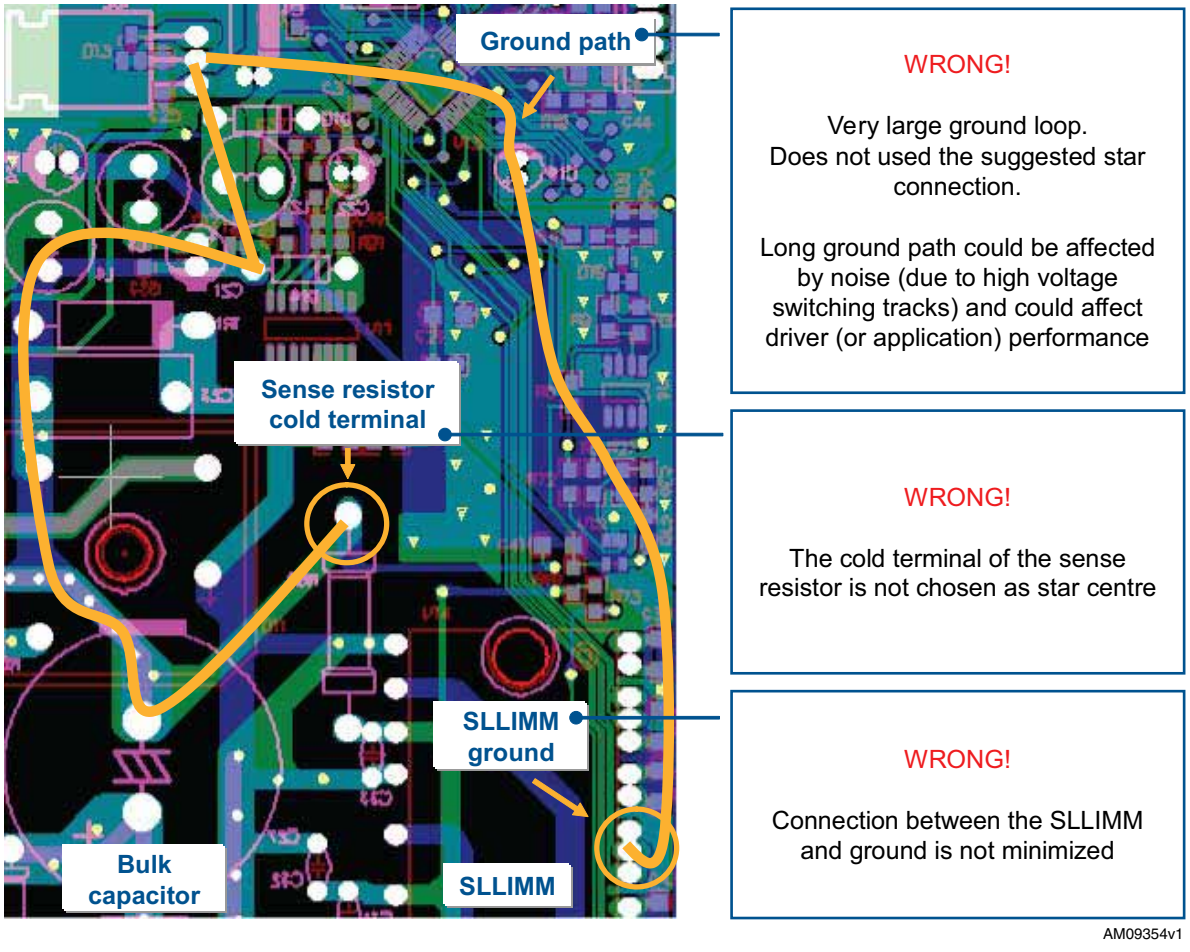


Figure 44. Example 2 of a possible wrong layout



5.2 Mounting instructions

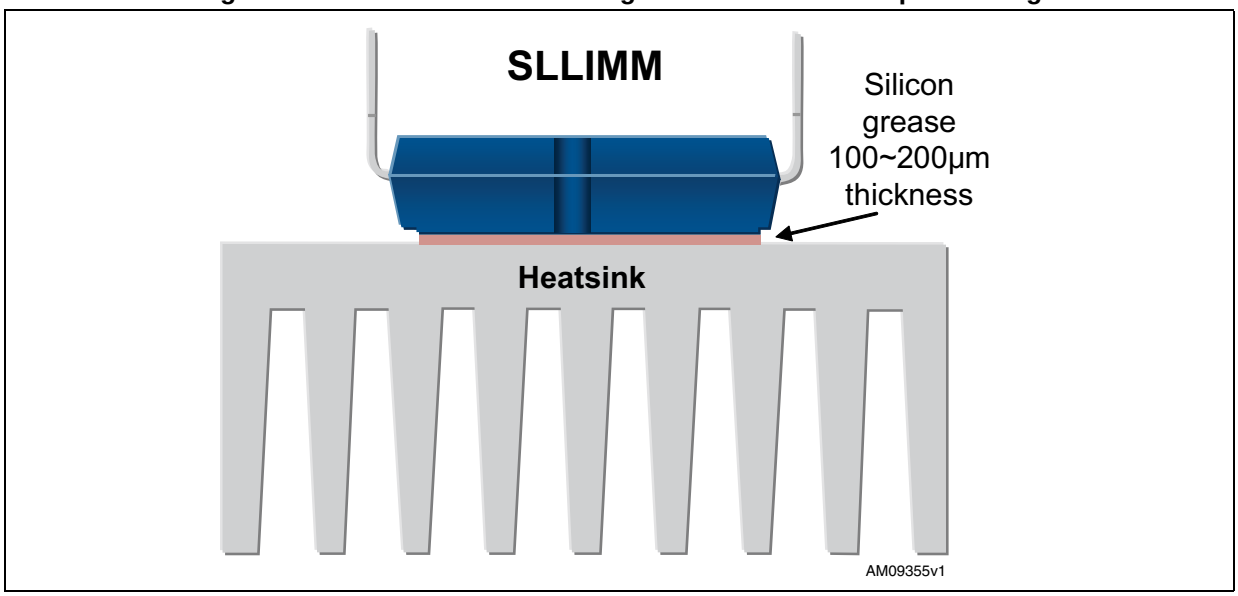
The purpose of the mounting instructions is to define some basic assembly rules in order to limit thermal and mechanical stresses or assure the best thermal conduction and electrical isolation of both SDIP-25L and SDIP-38L packages when mounting on a heatsink.
For further details please refer to the TN0107 technical note.

5.2.1 Heatsink mounting

The following precautions should be observed to maximize the effect of the heatsink and minimize stresses on the device. Smooth the surface by removing burrs and protrusions; it is essential to ensure an optimal contact between the SLLIMM and the heatsink.

Apply a uniform layer of silicon grease, from 100 µm up to 200 µm of thickness, between the device and the heatsink to reduce the contact thermal resistance, as shown in *Figure 45*. Be sure to apply the coating thinly and evenly, paying attention to not having any voids remaining on the contact surface between the SLLIMM and the heatsink. We recommend using high quality grease with stable performance within the operating temperature range of the SLLIMM.

Figure 45. Recommended silicon grease thickness and positioning



5.2.2 Mounting torque

While mounting the SLLIMM to a heatsink make sure not to apply excessive force during the assembly. *Table 14* provides the specified fastening torque. Inappropriate mounting can damage the device and over tightening the screws may cause DBC substrate or molding compound cracks. Avoid mechanical stress due to tightening on one side only. It is recommended to temporarily fasten both screws, then fasten them permanently to the specified torque value using a torque wrench. *Figure 47* shows the screw fastening order.

Table 14. Mounting torque and heatsink flatness

Parameter	Limits			Units
	Min.	Typ.	Max.	
Mounting torque (M3 screw)	0.4	0.7	1.0	Nm
Heatsink flatness	-50		150	µm
SDIP-25L package weight		13		g
SDIP-38L package weight		17		g

Figure 46. Measurement point of Cu heatsink flatness

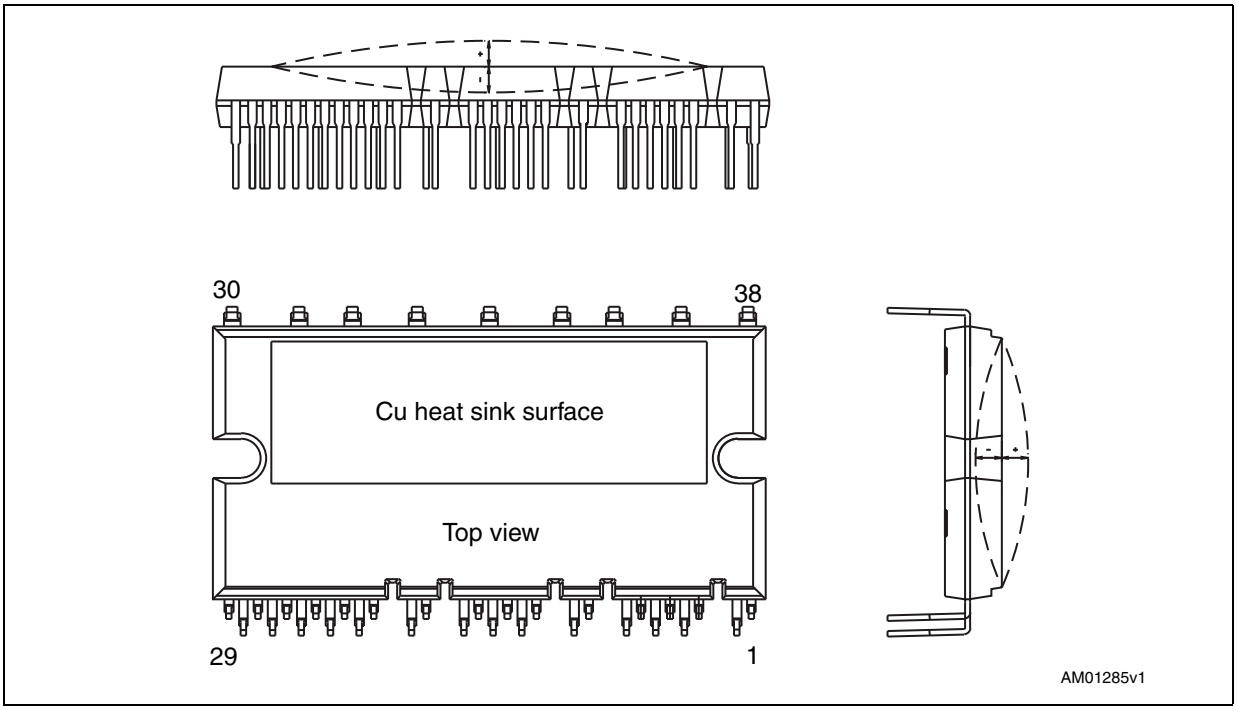
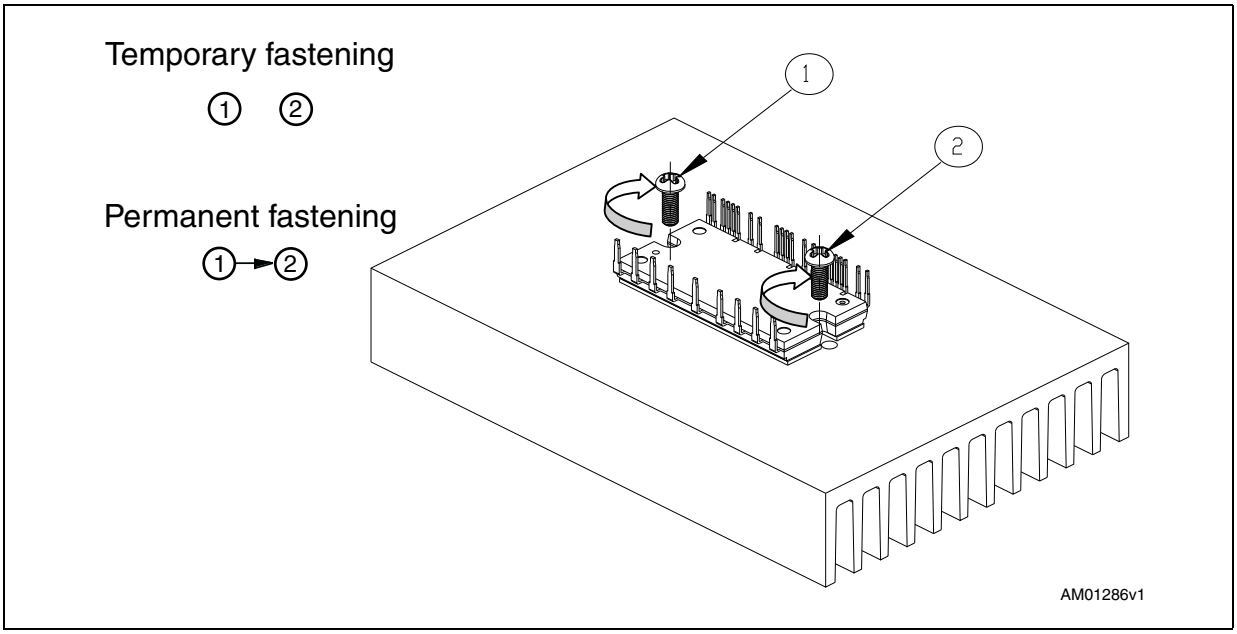


Figure 47. Recommended fastening order of mounting screws



5.2.3 General handling precaution and storage notices

The incidence of thermal and/or mechanical stress to the semiconductor devices due to improper handling may result in significant deterioration of their electrical characteristics and/or reliability.

The SLLIMM is an ESD sensitive device, it may be damaged in the case of ESD shocks. All equipment used to handle power modules must comply with ESD standards including transportation, storage, and assembly.

Transportation

Be careful when handling the SLLIMM and packaging material. Ensure that the module is not subjected to mechanical vibration or shock during transport. Do not toss or drop to ensure the SLLIMM is correctly functioning before boarding. Wet conditions are dangerous and moisture can also adversely affect the packaging. Hold the package avoiding touching the leads during mounting. Put package boxes upside down, leaning them or giving them uneven stress may cause the terminals to be deformed or the resin to be damaged. Throwing or dropping the packaging boxes may cause the modules to be damaged. Wetting the packaging boxes may cause the breakdown of modules when operating. Pay particular care when transporting in wet conditions.

Storage

- Do not force or load the external pressure to the modules while they are in storage
- Humidity should be kept within the range of 40% to 75%, the temperature should not go over 35 °C or below 5 °C
- Lead solder ability is degraded by lead oxidation or corrosion. So using storage areas where there is minimal temperature fluctuation is highly recommended
- The presence of harmful gases or dusty conditions is not acceptable for storage.
- Use antistatic containers

Electrical shock and thermal injury

- Do not touch either module or heatsink when SLLIMM is operating to avoid sustaining an electrical shock and/or a burn injury.

6 References

1. STGIPS10K60A datasheet
2. STGIPS14K60 datasheet
3. STGIPL14K60 datasheet
4. STGIPS20K60 datasheet
5. STGIPL20K60 datasheet
6. AN2738 application note
7. UM0969 user manual
8. UM0900 user manual
9. UM1036 user manual
10. Minimum-Loss Strategy for Three-Phase PWM Rectifier, IEEE, JUNE 1999
11. TN0107 technical note.

Note: SLLIMM™ and PowerMESH™ are trademarks of STMicroelectronics.

7 Revision history

Table 15. Document revision history

Date	Revision	Changes
21-Mar-2011	1	Initial release.
12-Jul-2011	2	Modified: R_{thJC} *Table 1 on page 9*, *Figure 32 on page 47* and Heatsink flatness max. value *Table 14 on page 67*.
17-Sep-2012	3	Updated: *Figure 4 on page 10*, *Figure 18 on page 30*, *Figure 41 on page 63*, *Figure 42 on page 64* and *Figure 43 on page 65*.
17-Mar-2015	4	Updated product features in *Section 1.1* Added footnote to *Table 1* Updated figures: *Figure 4*, *Figure 14*, *Figure 16*, *Figure 22*, *Figure 23*, *Figure 30*, *Figure 31* Removed footnote from *Table 5* Updated *Table 9*, *Table 10* In *Section 3.5*, updated Positive DC-link pin details Updated Equations *26* and *27* Updated *Table 13* Removed Section 5.2.4 Packaging specifications