SMART® Modular Technologies

SG2567RD312893UUD

February 20, 2009

Ordering Information		
Part Numbers	**Description**	**Device Vendor**
SG2567RD312893HBD	256Mx72 (2GB), DDR3, 240-pin Registered DIMM, Parity, ECC, 128Mx8 Based, PC3-10600, DDR3-1333-999, 30.00mm, Green Module (RoHS Compliant).	Hynix, Rev. B H5TQ1G83BFR-H9C
SG2567RD312893SDD	256Mx72 (2GB), DDR3, 240-pin Registered DIMM, Parity, ECC, 128Mx8 Based, PC3-10600, DDR3-1333-999, 30.00mm, Green Module (RoHS Compliant).	Samsung, Rev. D K4B1G0846D-HCH9
SG2567RD312893SED	256Mx72 (2GB), DDR3, 240-pin Registered DIMM, Parity, ECC, 128Mx8 Based, PC3-10600, DDR3-1333-999, 30.00mm, Green Module (RoHS Compliant).	Samsung, Rev. E K4B1G0846E-HCH9

(All specifications of this module are subject to change without notice.)

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Revision History

- **February 20, 2009**
  Datasheet released.

2GByte (256Mx72) DDR3 SDRAM Module - 128Mx8 Based 240-pin DIMM, Registered, Parity, ECC

Features

- Standard = JEDEC
- Configuration = ECC
- Number of Module Ranks = 2
- Number of Devices = 18
- $V_{DD} = V_{DDQ}$ = 1.5V
- V_{DDSPD} = 1.7V to 3.6V
- Cycle Time = 1.5ns
- $\overline{CAS}$ Latency = 6, 8, 9
- Additive Latency = 0, CL-1, and CL-2
- $\overline{CAS}$ Write Latency (CWL) = 5, 6, 7
- Burst Length = BC4, BL8, BC4 or BL8 (on the fly)
- Burst Length = Nibble Sequential & Interleave Mode
- Internal Banks per SDRAM = 8
- Refresh = 8K/64ms
- Device Package = FBGA
- Lead Finish = Gold
- Length x Height = 133.35mm x 30.00mm
- No. of sides = Double-sided
- Mating Connector (Examples)
  Vertical = AMP - 5-1932000-9
- ZQ calibration supported
- On chip DLL align DQ, DQS and $\overline{DQS}$ transition with CK transition
- DM write data-in at both the rising and falling edges of the data strobe
- All addresses and control inputs latched on the rising edges of the clock
- Dynamic On Die Termination supported
- Driver strength selected by EMRS
- Asynchronous RESET pin supported
- Write Levelization supported
- 8-bit pre-fetch

Addressing

Device Configuration	128Mx8
Number of Internal Banks	8
Bank Address	BA0 - BA2
Auto precharge	A10/AP
BC switch on the fly	A12/$\overline{BC}$
Row Address	A0 - A13
Column Address	A0 - A9

Pin Description Table

Symbol	Type	Polarity	Function
CK0~CK1, $\overline{CK0}$~$\overline{CK1}$	Input	Differential Crossing	CK and $\overline{CK}$ are differential clock inputs. All the DDR3 SDRAM address/control inputs are sampled on the crossing of the positive edge of CK and the negative edge of $\overline{CK}$. Output (read) data is referenced to the crossing of CK and $\overline{CK}$ (Both directions of crossing).
CKE0, CKE1	Input	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
$\overline{CS0}$~$\overline{CS1}$	Input	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When decoder is disabled, new commands are ignored but previous operations continue.This signal provides for external rank selection on systems with multiple ranks.
ODT0, ODT1	Input	Active High	When high, termination resistance is enabled for all DQ, DQS, $\overline{DQS}$ and DM pins, assuming this function is enabled on the DRAM.
BA0~BA2	Input	-	Selects which SDRAM bank of the eight is activated.

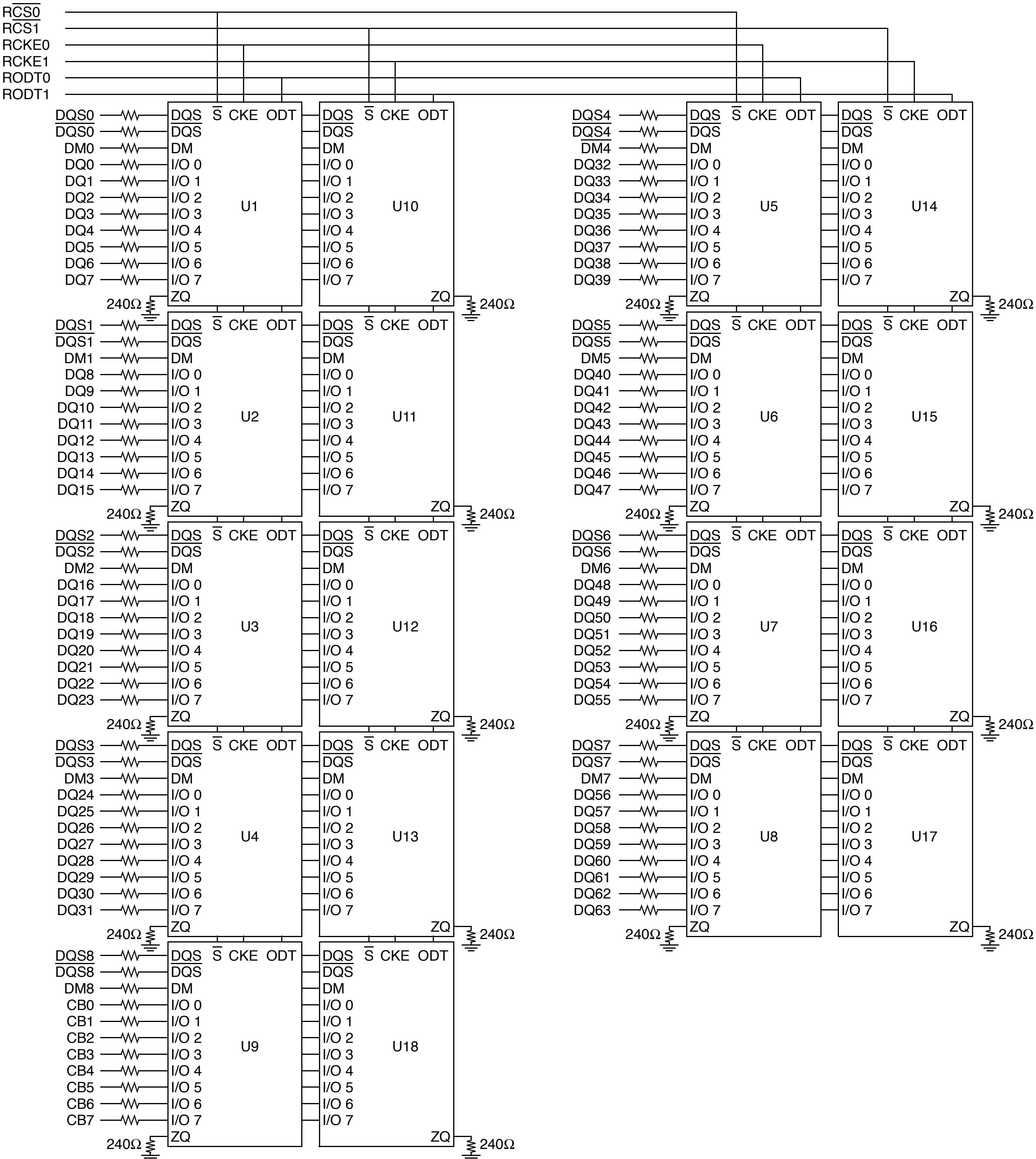
Pin Description Table (Contd.)

Symbol	Type	Polarity	Function
A0~A15	Input	-	During a Bank Activate command cycle, address inputs define the row address (RA0–RA13). During a Read or Write command cycle, address inputs define the column address (CA0–CA9). In addition to the column address, AP is used to invoke auto-precharge operation at the end of the burst read or write cycle. If AP is high, auto-precharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, auto-precharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to pre-charge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12($\overline{\text{BC}}$) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped). A14 & A15 are only connected to the register for the parity check.
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Input	Active Low	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
DQ0~DQ63 CB0~CB7	Input/ Output	-	Data and Check Bit Input/Output pins.
DQS0~DQS8 $\overline{\text{DQS0}}$~$\overline{\text{DQS8}}$	Input/ Output	Differential Crossing	Data strobe for input and output data.
DM0~DM8	Input	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled high coinci-dent with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
PAR_IN	Input	Active High	Parity bit for the Address and Control bus. (“1 “: Odd, “0 “: Even)
$\overline{\text{ERR\_OUT}}$	Output	Active Low	Parity error detected on the Address and Control bus. A resistor may be connected from $\overline{\text{ERR\_OUT}}$ bus line to V_{DD} on the system planar to act as a pull up.
SA0~SA2	Input	-	These signals are tied at the system to either V_{SS} or V_{DDSPD} to configure the serial SPD EEPROM address range.
SDA	Input/ Output	-	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resis-tor may be connected from the SDA bus line to V_{DDSPD} to act as a pullup on the system board.
SCL	Input	-	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus tied to V_{DDSPD} to act as a pullup on the system board.
$\overline{\text{EVENT}}$	Output	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device.The system should guarantee the electrical level requirement is met for the $\overline{\text{EVENT}}$ pin on TS/SPD part. No pull-up resister is provided on DIMM.
$\overline{\text{RESET}}$	Input	Active Low	Asynchronous Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}.
V_{DD}, V_{SS}	Supply	-	Power and ground for the DDR3 SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD}/V_{DDQ} planes on these modules. V_{SS} pins are tied to V_{SS} planes on these modules.
V_{DDQ}	Supply	-	Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. V_{DDQ} shares the same power plane as V_{DD} pins.
V_{REFDQ}	Supply		Reference voltage for I/O inputs.
V_{REFCA}	Supply	-	Reference voltage for address/command inputs.
V_{DDSPD}	Supply	-	Power supply for SPD EEPROM. This supply is separate from the V_{DD}/V_{DDQ} power plane.
V_{TT}	Supply	-	Termination voltage for address/command/control/clock nets.
NC	-	-	No Connect.

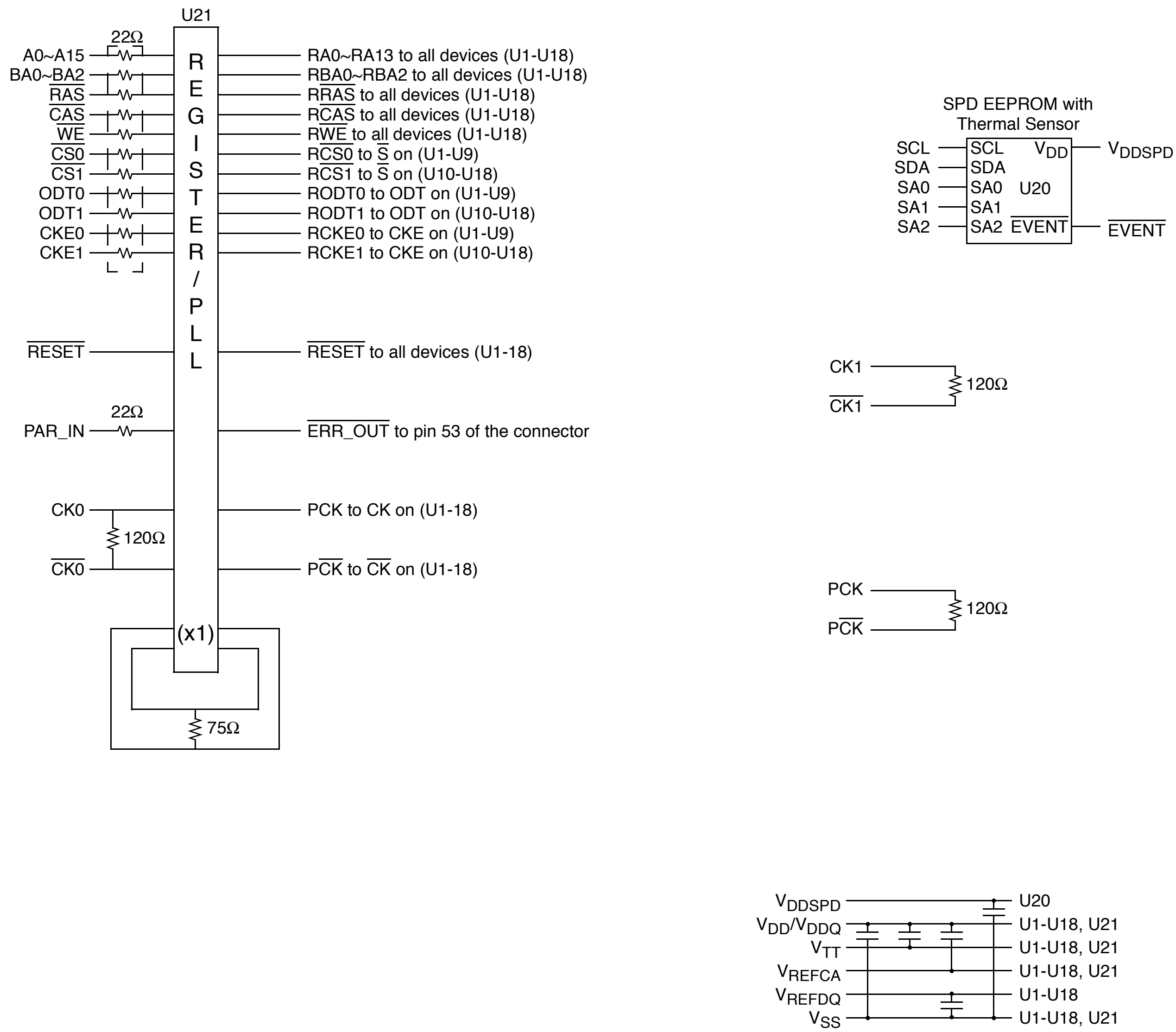
DDR3 240-pin DIMM Pin List

Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	V_{REFDQ}	31	DQ25	61	A2	91	DQ41	121	V_{SS}	151	V_{SS}	181	A1	211	V_{SS}
2	V_{SS}	32	V_{SS}	62	V_{DD}	92	V_{SS}	122	DQ4	152	DM3	182	V_{DD}	212	DM5
3	DQ0	33	$\overline{\text{DQS3}}$	63	CK1	93	$\overline{\text{DQS5}}$	123	DQ5	153	NC	183	V_{DD}	213	NC
4	DQ1	34	DQS3	64	$\overline{\text{CK1}}$	94	DQS5	124	V_{SS}	154	V_{SS}	184	CK0	214	V_{SS}
5	V_{SS}	35	V_{SS}	65	V_{DD}	95	V_{SS}	125	DM0	155	DQ30	185	$\overline{\text{CK0}}$	215	DQ46
6	$\overline{\text{DQS0}}$	36	DQ26	66	V_{DD}	96	DQ42	126	NC	156	DQ31	186	V_{DD}	216	DQ47
7	DQS0	37	DQ27	67	V_{REFCA}	97	DQ43	127	V_{SS}	157	V_{SS}	187	$\overline{\text{EVENT}}$	217	V_{SS}
8	V_{SS}	38	V_{SS}	68	PAR_IN	98	V_{SS}	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	V_{DD}	99	DQ48	129	DQ7	159	CB5	189	V_{DD}	219	DQ53
10	DQ3	40	CB1	70	A10/AP	100	DQ49	130	V_{SS}	160	V_{SS}	190	BA1	220	V_{SS}
11	V_{SS}	41	V_{SS}	71	BA0	101	V_{SS}	131	DQ12	161	DM8	191	V_{DD}	221	DM6
12	DQ8	42	$\overline{\text{DQS8}}$	72	V_{DD}	102	$\overline{\text{DQS6}}$	132	DQ13	162	NC	192	$\overline{\text{RAS}}$	222	NC
13	DQ9	43	DQS8	73	$\overline{\text{WE}}$	103	DQS6	133	V_{SS}	163	V_{SS}	193	$\overline{\text{CS0}}$	223	V_{SS}
14	V_{SS}	44	V_{SS}	74	$\overline{\text{CAS}}$	104	V_{SS}	134	DM1	164	CB6	194	V_{DD}	224	DQ54
15	$\overline{\text{DQS1}}$	45	CB2	75	V_{DD}	105	DQ50	135	NC	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	$\overline{\text{CS1}}$	106	DQ51	136	V_{SS}	166	V_{SS}	196	A13	226	V_{SS}
17	V_{SS}	47	V_{SS}	77	ODT1	107	V_{SS}	137	DQ14	167	NC	197	V_{DD}	227	DQ60
18	DQ10	48	NC	78	V_{DD}	108	DQ56	138	DQ15	168	$\overline{\text{RESET}}$	198	$\overline{\text{CS3}}$ (NC)	228	DQ61
19	DQ11	49	NC	79	$\overline{\text{CS2}}$ (NC)	109	DQ57	139	V_{SS}	169	CKE1	199	V_{SS}	229	V_{SS}
20	V_{SS}	50	CKE0	80	V_{SS}	110	V_{SS}	140	DQ20	170	V_{DD}	200	DQ36	230	DM7
21	DQ16	51	V_{DD}	81	DQ32	111	$\overline{\text{DQS7}}$	141	DQ21	171	A15	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	V_{SS}	172	A14	202	V_{SS}	232	V_{SS}
23	V_{SS}	53	$\overline{\text{ERR\_OUT}}$	83	V_{SS}	113	V_{SS}	143	DM2	173	V_{DD}	203	DM4	233	DQ62
24	$\overline{\text{DQS2}}$	54	V_{DD}	84	$\overline{\text{DQS4}}$	114	DQ58	144	NC	174	A12/$\overline{\text{BC}}$	204	NC	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	V_{SS}	175	A9	205	V_{SS}	235	V_{SS}
26	V_{SS}	56	A7	86	V_{SS}	116	V_{SS}	146	DQ22	176	V_{DD}	206	DQ38	236	V_{DDSPD}
27	DQ18	57	V_{DD}	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	V_{SS}	178	A6	208	V_{SS}	238	SDA
29	V_{SS}	59	A4	89	V_{SS}	119	SA2	149	DQ28	179	V_{DD}	209	DQ44	239	V_{SS}
30	DQ24	60	V_{DD}	90	DQ40	120	V_{TT}	150	DQ29	180	A3	210	DQ45	240	V_{TT}

Block Diagram



Note: Unless otherwise noted, data resistor values are 15Ω ± 5%.

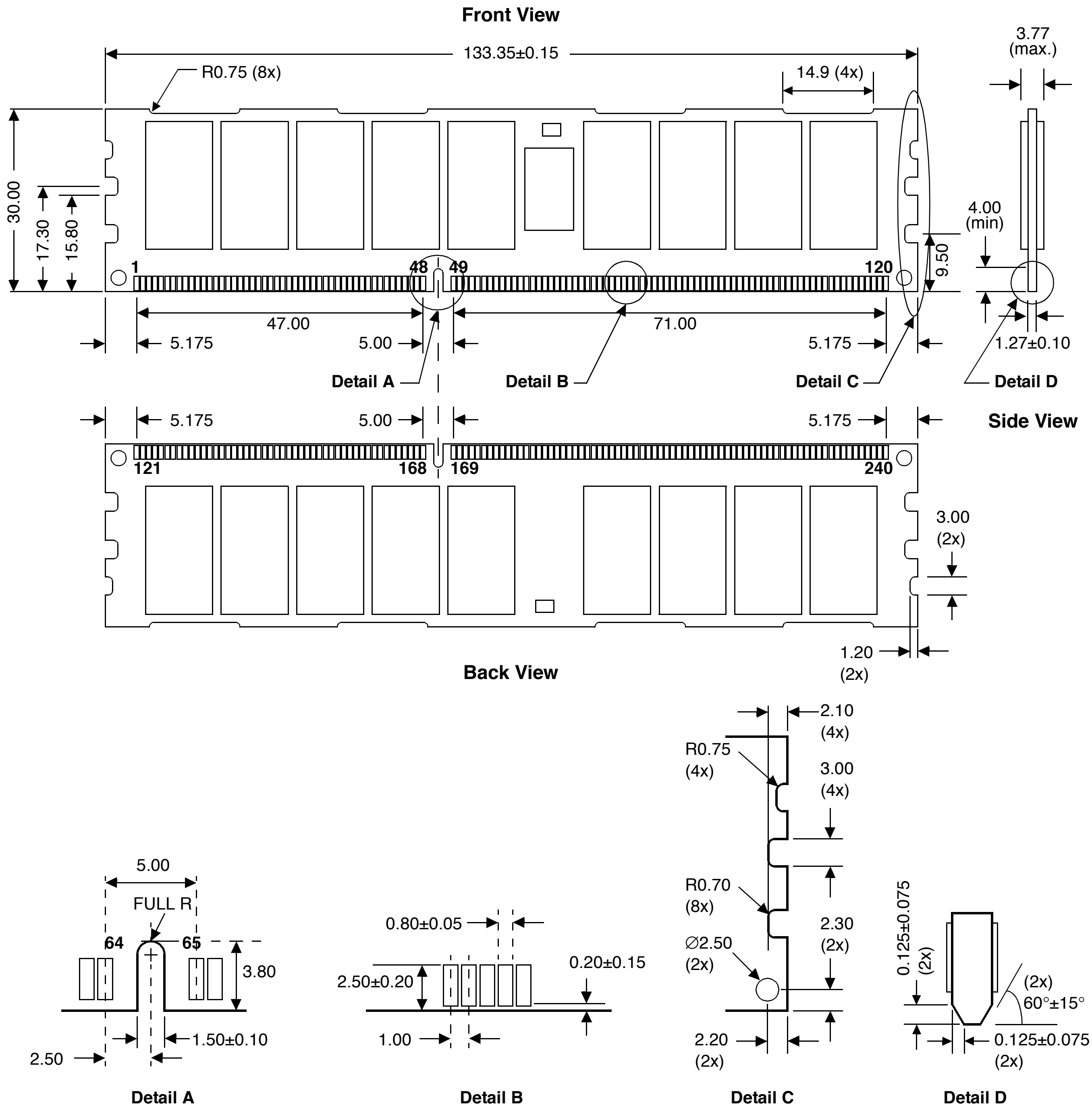


Notes:

1. Each address, command and control signal output line from the register is terminated at the end of the line through a 39Ω series resistor to V_{TT}.
2. Data bits may be swapped within a device. However, DQ/DQS/DM relationship must be maintained as shown on page 6.

Physical Dimensions

240-pin DIMM Module



(All dimensions are in millimeters with ±0.15mm tolerance unless specified otherwise.)

Serial Presence Detect Table (SG2567RD312893HBD/SDD/SED)

Byte No.	Byte Description	Value Supported	Hex Value
0	No. of Bytes Used, No. of Bytes in SPD Device, CRC Coverage	176, 256, 0~116	92h
1	SPD Revision	Revision 1.0	10h
2	Key Byte/DRAM Device Type	DDR3 SDRAM	0Bh
3	Key Byte/Module Type	RDIMM	01h
4	SDRAM Density and Banks	1Gb, 8 Banks	02h
5	SDRAM Addressing	14 Rows, 10 Columns	11h
6	Reserved	-	00h
7	Module Organization	2 Ranks, x8	09h
8	Module Memory Bus Width	x72	0Bh
9	Fine Timebase (FTB) Dividend/Divisor	2.5ps	52h
10	Medium Timebase Dividend	1	01h
11	Medium Timebase Divisor	8	08h
12	Minimum SDRAM Cycle Time (t_{CK}min)	1.5ns	0Ch
13	Reserved	-	00h
14	$\overline{CAS}$ Latencies Supported (CL4-CL11)	6, 8, 9	34h
15	$\overline{CAS}$ Latencies Supported (CL12-CL18)	-	00h
16	Minimum $\overline{CAS}$ Latency Time (t_{AA}min)	13.5ns	6Ch
17	Minimum Write Recovery Time (t_{WR}min)	15ns	78h
18	Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay Time (t_{RCD}min)	13.5ns	6Ch
19	Minimum Row Active to Row Active Delay Time (t_{RRD}-min)	6ns	30h
20	Minimum Row Precharge Delay Time (t_{RP}min)	13.5ns	6Ch
21	Upper Nibbles for t_{RAS} and t_{RC}	-	11h
22	Minimum Active to Precharge Delay Time (t_{RAS}min)	36ns	20h
23	Minimum Active to Active/Refresh Delay Time (t_{RC}-min)	49.5ns	8Ch
24	Minimum Refresh Recovery Delay Time (t_{RFC}min) (LSB)	110ns	70h
25	Minimum Refresh Recovery Delay Time (t_{RFC}min) (MSB)	110ns	03h

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Value Supported	Hex Value
26	Minimum Internal Write to Read Command Delay Time (t_{WTR}min)	7.5ns	3Ch
27	Minimum Internal Read to Precharge Command Delay Time (t_{RTP}min)	7.5ns	3Ch
28	Upper Nibble for t_{FAW}	30ns	00h
29	Minimum Four Active Window Delay Time (t_{FAW})	30ns	F0h
30	SDRAM Output Drivers Supported	DLL-off Mode, RZQ/7, RZQ/6	83h
31	SDRAM Thermal and Refresh Options	ASR, Ext. Temp. Range	05h
32	Module Thermal Sensor	EEPROM with Thermal Sensor	80h
33	SDRAM Device Type	Monolithic	00h
34~59	Reserved	-	00h
60	Module Nominal Height	30mm	0Fh
61	Module Maximum Thickness	Double-sided	11h
62	Reference Raw Card Used	R/C B, Rev. 0	01h
63	DIMM Module Attributes	1 Row, 1 Register	05h
64	RDIMM Thermal Heat Spreader	None	00h
65	Register Manufacturer ID Code (LSB)	Generic	00h
66	Register Manufacturer ID Code (MSB)	Generic	00h
67	Register Revision Number	-	FFh
68	Register Type	SSTE32882	00h
69	RC1 (MS Nibble) / RC0 (MS Nibble)	Raw Card B	01h
70	RC3 (MS Nibble) / RC2 (MS Nibble)	Raw Card B	00h
71	RC5 (MS Nibble) / RC4 (MS Nibble)	Raw Card B	00h
72	RC7 (MS Nibble) / RC6 (MS Nibble)	Raw Card B	00h
73	RC9 (MS Nibble) / RC8 (MS Nibble)	Raw Card B	00h
74	RC11 (MS Nibble) / RC10 (MS Nibble)	Raw Card B	00h
75	RC13 (MS Nibble) / RC12 (MS Nibble)	Raw Card B	00h
76	RC15 (MS Nibble) / RC14 (MS Nibble)	Raw Card B	00h
77~116	Reserved	-	00h

Serial Presence Detect Table (Contd.)

Byte No.	Byte Description	Value Supported	Hex Value
117	Module Manufacturer ID Code (LSB)	Continuation Code	01h
118	Module Manufacturer ID Code (MSB)	Smart ID code	94h
119	Module Manufacturing Location	See Note 1	01h
120	Module Manufacturing Date (Year)	Date	Date
121	Module Manufacturing Date (Week)	Date	Date
122~125	Module Serial Number	Serial Number	S. No
126	SPD Cyclical Redundancy Code		22h
127	SPD Cyclical Redundancy Code		C7h
128~145	Module Part Number	SG2567RD312893UUD	
146	Module Revision Code (SPD Revision)	Revision 0	00h
147	Module Revision Code	-	00h
148	DRAM Manufacturer ID Code (LSB)	Hynix Samsung	80h 80h
149	DRAM Manufacturer ID Code (MSB)	Hynix Samsung	ADh CEh
150~175	Manufacturer Specific Data	SMART Modular Technologies	
176~255	Open for Customer use	-	00h

Note:

1. Manufacturing Location:
   00h - Undefined,
   01h - Fremont, USA,
   02h - Aguada, Puerto Rico,
   03h - East Kilbride, Scotland,
   04h - Penang, Malaysia,
   05h - Bangalore, India,
   06h - Sao Paulo, Brazil,
   07h - Aguadilla, Puerto Rico,
   08h - Mayaguez, Puerto Rico,
   09h - Santo Domingo, Dominican Republic,
   0Ah - Dongguan, China,

Mode Register (MR0) Table Definition

The mode register stores the data for controlling the various operating modes of DDR3 SDRAM. It controls CAS latency, burst length, burst chop, burst sequence, test mode, DLL reset, t_{WR} and various vendor specific options to make DDR3 SDRAM useful for various applications. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, BA0, BA1 and BA2 while controlling the state of address pins A0~A15.

	BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Address Field	BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register 0	0[1]	0	0	0[1]	0[1]	0[1]	PPD	WR			DLL	TM	CAS Latency			RBT	CL	BL	

A8	DLL Reset
0	No
1	Yes

A7	Mode
0	Normal
1	Test

A3	Read Burst Type
0	Nibble Sequential
1	Interleave

A1	A0	Burst Length
0	0	8 (Fixed)
0	1	BC4 or 8 (on-the-fly)
1	0	BC4 (Fixed)
1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

A11	A10	A9	WR (cycles)
0	0	0	Reserved
0	0	1	5[2]
0	1	0	6[2]
0	1	1	7[2]
1	0	0	8[2]
1	0	1	10[2]
1	1	0	12[2]
1	1	1	Reserved

A6	A5	A4	A2	$\overline{CAS}$ Latency
0	0	0	0	Reserved
0	0	1	0	5 (Optional)
0	1	0	0	6
0	1	1	0	7 (Optional)
1	0	0	0	8 (Optional)
1	0	1	0	9 (Optional)
1	1	0	0	10 (Optional)
1	1	1	0	11 (Optional)

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Notes:

1. BA2 and A13~A15 are reserved for future use and must be programmed to 0 during MRS.
2. WR(write recovery for autoprecharge)min in clock cycles is calculated by dividing t_{WR}(in ns) by t_{CK}(in ns) and rounding up to the next integer: WRmin[cycles] = Round-up(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with t_{RP} to determine t_{DAL}.

Mode Register (MR1) Table Definition

The Mode Registers MR1 stores the data for enabling or disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write Leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA0 and low on BA1 and BA2, while controlling the state of address pins A0~A15.

	BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Address Field	BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register 1	0[1]	0	1	0[1]	0[1]	0[1]	Qoff	TDQS	0[1]	Rtt_Nom	0[1]	Level	Rtt_Nom	D.I.C	AL		Rtt_Nom	D.I.C	DLL

A11	TQDS enable
0	Disabled
1	Enabled

A7	Write Leveling enable
0	Disabled
1	Enabled

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

A0	DLL Enable
0	Enable
1	Disable

A12	Qoff[2]
0	Output buffer enabled
1	Output buffer disabled

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A9	A6	A2	Rtt_Nom[3]
0	0	0	ODT disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12[4]
1	0	1	RZQ/8[4]
1	1	0	Reserved
1	1	1	Reserved

Note: RZQ = 240Ω

A5	A1	Output Driver Impedance Control
0	0	Reserved for RZQ/6
0	1	RZQ/7
1	0	RZQ/TBD
1	1	RZQ/TBD

Note: RZQ = 240Ω

Notes:
1. BA2 and A8, A10, A13~A15 are reserved for future use and must be programmed to 0 during MRS.
2. Outputs disabled - DQs, DQSs, $\overline{DQSs}$.
3. In Write Leveling Mode (MR1[bit7] = 1) with MR1[bit12] = 1, all Rtt_Nom settings are allowed; in Write Leveling Mode (MR1[bit7] =1) with MR1[bit12] = 0, only Rtt_Nom settings of RZQ/2, RZQ/4 and RZQ/6 are allowed.
4. If Rtt_Nom is used during Writes, only the values RZQ/2, RZQ/4 and RZQ/6 are allowed.

Mode Register (MR2) Table Definition

The Mode Registers MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS Write Latency. The Mode Register 2 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and low on BA0 and BA2 while controlling the state of address pins A0~A15.

Address Field	BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register 2	0[1]	1	0	0[1]	0[1]	0[1]	0[1]	0[1]	Rtt_WR		0[1]	SRT	ASR	CWL			PASR		

A7	Self-Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended (optional) operating temperature range

A2	A1	A0	Partial Array Self-Refresh (Optional)
0	0	0	Full Array
0	0	1	Half Array (BA[2:0] = 000, 001, 010, & 011)
0	1	0	Quarter Array (BA[2:0] = 000 & 001)
0	1	1	1/8th Array (BA[2:0] = 000)
1	0	0	3/4 Array (BA[2:0] = 010,011,100,101,110, & 111)
1	0	1	Half Array (BA[2:0] = 100, 101, 110, & 111)
1	1	0	Quarter Array (BA[2:0] = 110, & 111)
1	1	1	1/8th Array (BA[2:0] = 111)

A6	Auto Self-Refresh (ASR)
0	Manual SR Ref. (SRT)
1	ASR enable (optional)

A10	A9	Rtt_WR[2]
0	0	Dynamic ODT off
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A5	A4	A3	$\overline{CAS}$ Write Latency
0	0	0	5 ($t_{CK} \geq 2.5ns$)
0	0	1	6 ($2.5ns > t_{CK} \geq 1.875ns$)
0	1	0	7 ($1.875ns > t_{CK} \geq 1.5ns$)
0	1	1	8 ($1.5ns > t_{CK} \geq 1.25ns$)
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Notes:
1. BA2, A8 and A11~A15 are reserved for future use and must be programmed to 0 during MRS.
2. If Rtt_WR value can be applied during writes even when Rtt_Nom is disabled. During Write Leveling, Dynamic ODT is not available.

Mode Register (MR3) Table Definition

The Mode Register MR3 controls Multi-purpose registers. The Mode Register 3 is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, high on BA1 and BA0, low on BA2 while controlling the state of address pins A0~A15.

	BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Address Field	BA2	BA1	BA0	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
Mode Register 3	0[1]	1	1	0[1]													MPR	MPR Loc	

MPR Address

A2	MPR
0	Normal Operation[3]
1	Dataflow from MPR

MPR Address

A1	A0	MPR Location
0	0	Predefined pattern[2]
0	1	RFU
1	0	RFU
1	1	RFU

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Notes:
1. BA2, A3~A15 are reserved for future use and must be programmed to 0 during MRS.
2. The predefined pattern will be used for read synchronization.
3. When MPR control is set for normal operation (MR3 A[2] = 0), then MR3 A[1:0] will be ignored.

Command Truth Table

The following Truth Tables provide a general reference of available commands. For a more detailed description please refer to the device data sheets.

(a) Notes 1- 4 apply to the entire Command Truth Table.

(b) Note 5 applies to all Read/Write command.

[BA= Bank address, RA= row Address, CA = Column Address, $\overline{\text{BC}}$ = Burst chop, X = Don't care, V = Valid]

Function	Abbreviation	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	BA0~ BA2	A13~ A15	A12/ $\overline{\text{BC}}$	A10/ AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self-Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7, 9, 12
Self-Refresh Exit	SRX	L	H	H	V	V	V	V	V	V	V	V	7, 8, 9, 12
				L	H	H	H						
Single Bank Precharge	PRE	H	H	L	L	H	L	BA	V	V	L	V	
Precharge All Banks	PREA	H	H	L	L	H	L	V	V	V	H	V	
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	L	L	BA	RFU	L	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	L	L	BA	RFU	H	L	CA	
Write with Auto-Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto-Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto-Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto-Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto-Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto-Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power-Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6, 12
				H	V	V	V						
Power-Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6, 12
				H	V	V	V						
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Command Truth Table Notes:

1. All DDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. $\overline{RESET}$ command is enabled when Low, which will be used only for asynchronous reset, so $\overline{RESET}$ must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS, BA selects an (Extended) Mode Register.
4. “V” means “H or L (but a defined logic level)” and “X” means either “defined or undefined (like floating) logic level”.
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by the MRS.
6. The Power-Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
8. Self-Refresh Exit is asynchronous.
9. V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self-Refresh operation.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command (NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read and write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

CKE Truth Table

(a) Notes 1-7 apply to the entire CKE Truth Table.
(b) CKE low is allowed only if tMRD and tMOD are satisfied.

Current State	CKE		Command (N)[3] $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$	Action (N)[3]	Notes
	Previous Cycle (N-1)	Current Cycle (N)			
Power-Down	L	L	X	Maintain Power-Down	14, 15
	L	H	Deselect or NOP	Power-Down Exit	11, 14
Self-Refresh	L	L	X	Maintain Self-Refresh	15, 16
	L	H	Deselect or NOP	Self-Refresh Exit	8, 12, 16
Bank Activate	H	L	Deselect or NOP	Active Power-Down Entry	11, 13, 14
Reading	H	L	Deselect or NOP	Power-Down Entry	11, 13, 14, 17
Writing	H	L	Deselect or NOP	Power-Down Entry	11, 13, 14, 17
Precharging	H	L	Deselect or NOP	Power-Down Entry	11, 13, 14, 17
Refreshing	H	L	Deselect or NOP	Precharge Power-Down Entry	11
All Banks Idle	H	L	Deselect or NOP	Precharge Power-Down Entry	11, 13, 14, 18
		L	Refresh	Self-Refresh	9, 13, 18
For more details with all signals, see Command Truth Table on the previous pages.					10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. CKE must be registered with the same value on t_{CKE}min consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the t_{CKE}min clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of t_{IS} + t_{CKE}min + t_{IH}.
7. Deselect and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit, Deselect or NOP commands must be issued on every clock edge occurring during the t_{XS} period. Read or ODT commands may be issued only after t_{XSDLL} is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are NOP and Deselect only.
12. Valid commands for Self-Refresh Exit are NOP and Deselect only.
13. Self-Refresh can not be entered during Read or Write operations.
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care” (including floating around V_{REF}) in Self-Refresh and Power-Down. It also applies to Address pins.
16. V_{REF} (Both V_{REFDQ} and V_{REFCA}) must be maintained during Self-Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. “Idle state” is defined as all banks are closed (t_{RP}, t_{DAL}, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (t_{MRD}, t_{MOD}, t_{RFC}, t_{ZQinit}, t_{ZQoper}, t_{ZQCS}, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (t_{XS}, t_{XP}, t_{XPDLL}, etc.).

Absolute Maximum Ratings

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} relative to V_{SS}	-0.4 ~ 1.975	V	1, 3
V_{DDQ}	Voltage on V_{DDQ} relative to V_{SS}	-0.4 ~ 1.975	V	1, 3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4 ~ 1.975	V	1
V_{DDSPD}	Voltage on V_{DDSPD} relative to V_{SS}	1.7 ~ 3.6	V	1
T_{STG}	Storage Temperature	-50 to +100	°C	1, 2

Notes:

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. V_{DD} and V_{DDQ} must be within 300 mV of each other at all times and V_{REF} must be not greater than 0.6*V_{DDQ}. When V_{DD} and V_{DDQ} are less than 500 mV; V_{REF} may be equal to or less than 300 mV.

Operating Temperature Range

Symbol	Parameter	Max	Units	Notes
T_{OPER}	Normal Operating Temperature Range (Case)	0 to 85	°C	1, 2
	Extended Operating Temperature Range (Optional)	85 to 95	°C	1, 3

Notes:

1. Operating Temperature T_{OPER} is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C and 85°C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval t_{REFI} to 3.9µs. It is also possible to specify a component with 1X refresh (t_{REFI} to 7.8µs) in the Extended Temperature Range. Please refer to the SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the SPD for option availability.

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min	Typ	Max		
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1, 2
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V	1
V_{DDSPD}	SPD Supply Voltage	3.0	3.3	3.6	V	
V_{TT}	SPD Supply Voltage	0.7125	0.75	0.7875	V	3
V_{SS}	Ground	0	0	0	V	

Notes:

1. Under all conditions, V_{DDQ} must be less than or equal to V_{DD}.
2. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.
3. $V_{TT} = V_{DDQ}/2$

AC and DC Logic Input Levels for Single-Ended Signals

Symbol	Parameter	DDR3-1333		Units	Notes
		Min	Max		
$V_{IH(DC)}$	DC input logic high	V_{REF} + 0.100	V_{DD}	V	1
$V_{IL(DC)}$	DC input logic low	V_{SS}	V_{REF} - 0.100	V	1
$V_{IH(AC)}$	AC input logic high	V_{REF} + 0.175	-	V	1
$V_{IL(AC)}$	AC input logic low	-	V_{REF} - 0.175	V	1

Notes:

1. For DQ and DM, $V_{REF} = V_{REFDQ}$. For input only pins except RESET#, $V_{REF} = V_{REFCA}$.
2. The ac peak noise on V_{REF} may not allow V_{REF} to deviate from $V_{REF(DC)}$ by more than ±1% V_{DD} (for reference: approx. ±15mV).
3. For reference: approx. $V_{DD}/2$ ± 15mV.

Differential swing requirements for clock (CK/$\overline{CK}$) and strobe (DQS/$\overline{DQS}$)

Symbol	Parameter	DDR3-1333		Units	Notes
		Min	Max		
V_{IHDIFF}	Differential input logic high	0.200	Note 3	V	1
V_{ILDIFF}	Differential input logic high	Note 3	-0.200	V	1
$V_{IHDIFF(AC)}$	AC input logic high	2 * ($V_{IH(AC)}$ - V_{REF})	Note 3	V	2
$V_{ILDIFF(AC)}$	AC input logic low	Note 3	2 * (V_{REF} - $V_{IL(AC)}$)	V	2

Notes:
1. Used to define a differential signal slew-rate.
2. For CK/$\overline{CK}$, use V_{IH}/$V_{IL(AC)}$ of ADD/CMD and V_{REFCA}; for DQS/$\overline{DQS}$, use V_{IH}/$V_{IL(AC)}$ of DQs and V_{REFDQ}; if a reduced AC-high or AC-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$ need to be within the respective limits ($V_{IH(DC)}$max, $V_{IL(DC)}$min) for single-ended signals as well as the limitations for overshoot and undershoot.

Single-ended Input Slew Rate Definition

Description	Measured		Defined by	Applicable for
	from	to		
Input slew rate for rising edge	V_{REF}	$V_{IL(AC)min}$	$\frac{V_{IH(AC)min} - V_{REF}}{\Delta TRS}$	Setup (t_{IS}, t_{DS})
Input slew rate for falling edge	V_{REF}	$V_{IL(AC)max}$	$\frac{V_{REF} - V_{IL(AC)max}}{\Delta TFS}$	
Input slew rate for rising edge	$V_{IL(DC)max}$	V_{REF}	$\frac{V_{REF} - V_{IL(DC)max}}{\Delta TFH}$	Hold (t_{IH}, t_{DH})
Input slew rate for falling edge	$V_{IL(DC)min}$	V_{REF}	$\frac{V_{IH(DC)min} - V_{REF}}{\Delta TRH}$	

Input/Output Capacitance

Speed Bin		DDR3-1333		Units	Notes
Parameter	**Symbol**	**min**	**max**		
Input/output capacitance, (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	C_{IO}	3.0	5	pF	1, 2
Input/output capacitance delta, (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$)	C_{DIO}	-1	0.6	pF	2, 7
Input/output capacitance delta, (DQS and $\overline{DQS}$)	C_{DDQS}	0	0.4	pF	2, 4
Input capacitance, (CK and $\overline{CK}$)	C_{CK}	2.0	3.0	pF	2
Input capacitance delta, (CK and $\overline{CK}$)	C_{DCK}	-	0.5	pF	2, 3
Input capacitance, (ADD, CMD, CTRL input-only pins)	C_I	1.5	2.5	pF	2, 5
Input capacitance delta, (ADD, CMD, CTRL input-only pins)	C_{DI}	-	0.5	pF	2, 6

Notes:

1. Although the DM, TDQS and $\overline{TDQS}$ pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization.
3. Absolute value of $C_{CK} - C_{\overline{CK}}$
4. Absolute value of $C_{IO}(DQS) - C_{IO}(\overline{DQS})$
5. CI applies to ODT, $\overline{CS}$, CKE, A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
6. $C_{DI} = C_I - 0.5 * (C_I(CK) + C_I(\overline{CK}))$
7. $C_{DIO} = C_{IO}(DQ,DM) - 0.5 * (C_{IO}(DQS) + C_{IO}(\overline{DQS}))$

IDD Timing Parameters

Speed Bin	DDR3-1333	Units
Parameter	9-9-9	
t_{CKmin}(IDD)	1.5	ns
CL(IDD)	9	
t_{RCDmin}(IDD)	13.5	ns
t_{RCmin}(IDD)	49.5	ns
t_{RASmin}(IDD)	36	ns
t_{RPmin}(IDD)	13.5	ns
t_{FAW}(IDD)	30	ns
t_{RRD}(IDD)	6	ns
t_{RFC}(IDD)	110	ns

Definitions for IDD Measurement Conditions

- LOW is defined as $V_{IN} \leq V_{ILAC(max)}$; HIGH is defined as $V_{IN} \geq V_{IHAC(max)}$.
- STABLE is defined as inputs are stable at a HIGH or LOW level.
- FLOATING is defined as inputs are $V_{REF} = V_{DDQ} / 2$.
- Read Data is defined as the output data switching every clock, and Write Data is defined as the input data switching every clock, which means that Read Data and Write Data are stable during one clock cycle.
- SWITCHING is defined by the following table:

SWITCHING for Address, Bank Address, Command Signals, Data (DQ) and Data Masking (DM)	
Address (Row, Column):	If not otherwise mentioned, the inputs are stable at HIGH or LOW during 4 clock cycles and then change to the opposite value (e.g. Ax Ax Ax Ax $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ $\overline{Ax}$ Ax Ax Ax Ax.....)
Bank Address:	If not otherwise mentioned, the bank addresses should be switched like the row/column addresses
Command ($\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$):	Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$} = {HIGH, LOW, LOW, LOW} Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$} = {HIGH, HIGH, HIGH, HIGH} Define Command Background Pattern = D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$ D D $\overline{D}$ $\overline{D}$... If other commands are necessary (e.g. ACT for IDD0 or Read for IDD4R), the Background Pattern Command is substituted by the respective $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ levels of the necessary command.
Data (DQ):	Data DQ is changing between HIGH and LOW every other data transfer (once per clock) for DQ signals, which means that data DQ is stable during one clock.
Data Masking (DM):	No Switching; DM must be driven LOW at all times.

IDD Measurement Conditions

Symbol	Description	Conditions
I_{DD0}	Operating Current 0 → One bank Activate → Precharge	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}$(IDD); $t_{RC} = t_{RCmin}$(IDD); $t_{RAS} = t_{RASmin}$(IDD); $\overline{CS}$ is HIGH between Activate and Precharge commands; Command Inputs are SWITCHING except during Activate and Precharge commands; Row Addresses are SWITCHING; Address Input A10 must be LOW at all times; Bank Address is fixed (bank 0); Data I/O are SWITCHING; Output Buffer (DQ/DQS) is Off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; Bank 0 active in a ACT-PRE loop; All other banks idle.
I_{DD1}	Operating Current 1 → One bank Activate → Read → Precharge	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}$(IDD); $t_{RC} = t_{RCmin}$(IDD); $t_{RAS} = t_{RASmin}$(IDD); $t_{RCD} = t_{RCDmin}$(IDD); CL = CL(IDD); $\overline{CS}$ is HIGH between Activate, Read and Precharge commands; Command Inputs are SWITCHING except during Activate, Read and Precharge commands; Row Addresses are SWITCHING; Address Input A10 must be LOW at all times; Bank Address is fixed (bank 0); Data I/O are in Read Data; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1) in order to achieve I_{OUT} = 0mA; Data I/O should be FLOATING when there is no READ DATA; Rtt_Nom and Rtt_WR are disabled; Burst length = 8 fixed (MR0 bits [A1,A0] = {0,0}); Bank 0 active in a ACT-RD-PRE loop; All other banks idle.
$I_{DD2P}(0)$	Precharge Power-Down Current Slow Exit - MR0 bit A12 = 0	CKE is LOW; External Clock is on; $t_{CK} = t_{CKmin}$(IDD); $\overline{CS}$ is STABLE; Bank Addresses, Row Addresses and Command Inputs are STABLE; Data inputs are FLOATING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks idle; Slow Exit (RD and ODT commands must satisfy $t_{XPDLL-AL}$) (MR0 bit A12 = 0).
$I_{DD2P}(1)$[1]	Precharge Power-Down Current Fast Exit - MR0 bit A12 = 1	CKE is LOW; External Clock is on; $t_{CK} = t_{CKmin}$(IDD); $\overline{CS}$ is STABLE; Bank Addresses, Row Addresses and Command Inputs are STABLE; Data inputs are FLOATING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks idle; Fast Exit (any valid command after t_{XP}[2]) (MR0 bit A12 = 1).
I_{DD2N}	Precharge Standby Current	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}$(IDD); $\overline{CS}$ is HIGH; Bank Addresses, Row Addresses and Command Inputs are SWITCHING; Data inputs are SWITCHING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks idle.
I_{DD2Q}	Precharge Quiet Standby Current	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}$(IDD); $\overline{CS}$ is HIGH; Bank Addresses, Row Addresses and Command Inputs are STABLE; Data Input are FLOATING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks idle.

IDD Measurement Conditions (Contd.)

Symbol	Description	Conditions
I_{DD3P}	Active Power Down Current[3] Always Fast Exit	CKE is LOW; External Clock is on; $t_{CK} = t_{CKmin}$(IDD); $\overline{CS}$ is STABLE; Address and Command Inputs are STABLE; Data I/O are FLOATING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks active; Active power Down Mode is always "Fast Exit" with DLL on.
I_{DD3N}	Active Standby Current	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}$(IDD); $\overline{CS}$ is HIGH; Address and Command Inputs are SWITCHING; Data I/O are SWITCHING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks active.
I_{DD4R}	Operating Current Burst Read	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}$(IDD); CL = CL(IDD); $\overline{CS}$ is HIGH between valid commands; Command Inputs are SWITCHING except during Read commands; Column Addresses are SWITCHING; Address Input A10 must be LOW at all times; Bank Addresses are cycling ($0 \rightarrow 1 \rightarrow 2 \rightarrow 3$); Data I/O use Seamless Read Data Burst (BL8); Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1) in order to achieve I_{OUT} = 0mA; Rtt_Nom and Rtt_WR are disabled; Burst length = 8 fixed (MR0 bits [A1,A0] = {0,0}); All banks active.
I_{DD4W}	Operating Current Burst Write	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}$(IDD); CL = CL(IDD); $\overline{CS}$ is HIGH between valid commands; Command Inputs are SWITCHING except during Write commands; Column Addresses are SWITCHING; Address Input A10 must be LOW at all times; Bank Addresses are cycling ($0 \rightarrow 1 \rightarrow 2 \rightarrow 3$); Data I/O use Seamless Write Data Burst (BL8); Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1) in order to achieve I_{OUT} = 0mA; Rtt_Nom and Rtt_WR are disabled; Burst length = 8 fixed (MR0 bits [A1,A0] = {0,0}); All banks active.
I_{DD5B}	Burst Refresh Current	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}$(IDD); $t_{RFC} = t_{RFC\text{-}min}$(IDD); $\overline{CS}$ is HIGH between valid commands; Address and Command inputs are SWITCHING; Data I/O are SWITCHING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; Refresh command every $t_{RFC} = t_{RFCmin}$.
I_{DD6}	Self-Refresh Current Normal Temperature Range T_{CASE} = 0 to 85°C	T_{CASE} = 85°C; Normal Temperature Range (MR2 bit A6 = 0); CKE is LOW; External Clock is off; CK/$\overline{CK}$ are LOW; $\overline{CS}$ is FLOATING; Command Inputs are FLOATING; Row and Column Addresses are FLOATING; Bank Addresses are FLOATING; Data I/O are FLOATING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks are active during Self-Refresh actions; All banks are idle between Self-Refresh actions.

IDD Measurement Conditions (Contd.)

Symbol	Description	Conditions
I_{DD6ET}	Self-Refresh Current Extended Temperature Range T_{CASE} = 85 to 95°C	T_{CASE} = 95°C; Extended Temperature Range (MR2 bit A6 = 1); CKE is LOW; External Clock is off; CK/$\overline{CK}$ are LOW; $\overline{CS}$ is FLOATING; Command Inputs are FLOATING; Row and Column Addresses are FLOATING; Bank Addresses are FLOATING; Data I/O are FLOATING; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1); Rtt_Nom and Rtt_WR are disabled; All banks are active during Self-Refresh actions; All banks are idle between Self-Refresh actions.
I_{DD7}	All Bank Interleave Read Current	CKE is HIGH; External Clock is on; $t_{CK} = t_{CKmin}$(IDD); $t_{RC} = t_{RCmin}$(IDD); $t_{RAS} = t_{RASmin}$(IDD); $t_{RCD} = t_{RCDmin}$(IDD); $t_{RRD} = t_{RRDmin}$(IDD); CL = CL(IDD); AL = t_{RCDmin} - 1 * t_{CK}; $\overline{CS}$ is HIGH between valid commands; For Command inputs, see device datasheet for test patterns; Row and Column Addresses are STABLE during DESELECTs; Bank Addresses are cycling (0 → 1 → 2 → 3); Data I/O use Read Data (BL8); DM is low at all times; Output Buffer (DQ, DQS) is off (MR1 bit A12 = 1) in order to achieve I_{OUT} = 0mA; Rtt_Nom and Rtt_WR are disabled; Burst length = 8 fixed (MR0 bits [A1,A0] = {0,0}); All banks active (rotational).

Notes:

1. The MR0 bit A12 defines DLL on/off behavior only for precharge power down. There are 2 different Precharge Power Down states possible: one with DLL on (fast exit, bit 12 = 1) and one with DLL off (slow exit, bit 12 = 0).
2. Because it is an exit after precharge power down, the valid commands are: Activate, Refresh, Mode-Register Set, Enter - Self Refresh.
3. DDR3 will offer only ONE active power down mode with DLL on (→ fast exit). MR0 bit A12 will not be used for active power down. Instead bit A12 will be used to switch between two different precharge power down modes.

IDD Specifications

Speed Bin	DDR3-1333	Units	Notes
Parameter	9-9-9		
I_{DD0}	2045	mA	
I_{DD1}	2225	mA	
I_{DD2P}(0)	866	mA	
I_{DD2P}(1)	1550	mA	
I_{DD2N}	1730	mA	
I_{DD2Q}	1730	mA	
I_{DD3P}	1685	mA	
I_{DD3N}	1820	mA	
I_{DD4R}	3080	mA	
I_{DD4W}	3305	mA	
I_{DD5B}	3215	mA	
I_{DD6}	180	mA	
I_{DD6ET}	TBD	mA	
I_{DD7}	4520	mA	

Refresh Parameters

Parameter		Symbol	1Gb	Units
REF command to ACT or REF command time		t_{RFC}	110	ns
Average periodic refresh interval	0 °C ≤ T_{CASE} ≤ 85 °C	t_{REFI}	7.8	µs
	85 °C ≤ T_{CASE} ≤ 95 °C		3.9	µs

Device Standard Speed Bins

Speed Bin			DDR3-1333		Units	Notes
CL - nRCD - nRP			9-9-9			
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.5	20	ns	
ACT to internal read or write delay time		t_{RCD}	13.5	-	ns	
Pre command period		t_{RP}	13.5	-	ns	
ACT to ACT or REF command period		t_{RC}	49.5	-	ns	
ACT to PRE command period		t_{RAS}	36	9 * t_{REFI}	ns	
CL = 6	CWL = 5	$t_{CK(avg)}$	2.5	3.3	ns	1, 2, 3, 5
	CWL = 6, 7		Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(avg)}$	Reserved		ns	4
	CWL = 6		1.875	< 2.5	ns	1, 2, 3, 5
	CWL = 7		Reserved		ns	4
CL = 9	CWL = 5, 6	$t_{CK(avg)}$	Reserved		ns	4
	CWL = 7		1.5	< 1.875	ns	1, 2, 3
Supported CL Settings			6, 8, 9		n_{CK}	
Supported CWL Settings			5, 6, 7		n_{CK}	

Speed Bin Tables Notes

1. The CL setting and CWL setting result in $t_{CK(AVG)}$min and $t_{CK(AVG)}$max requirements. When making a selection of $t_{CK(AVG)}$, both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. $t_{CK(AVG)}$min limits: Since $\overline{CAS}$ Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard $t_{CK(AVG)}$ value (2.5, 1.875, or 1.5) when calculating CL [nCK] = t_{AA} [ns] / $t_{CK(AVG)}$ [ns], rounding up to the next 'Supported CL'.
3. $t_{CK(AVG)}$max limits: Calculate $t_{CK(AVG)} = t_{AA}$max / CL SELECTED and round the resulting $t_{CK(AVG)}$ down to the next valid speed bin (i.e. 3.3ns, 2.5ns, or 1.875 ns). This result is $t_{CK(AVG)}$max corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.

Device Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-1333		Units	Notes
		Min	Max		
Clock Timing					
Minimum clock cycle time (DLL off mode)	$t_{CK(DLL\_OFF)}$	8	-	t_{CK}	6
Average clock period	$t_{CK(avg)}$	Refer to Speed Bin on page 28		ps	
Average high pulse width	$t_{CH(avg)}$	0.47	0.53	$t_{CK(avg)}$	
Average low pulse width	$t_{CL(avg)}$	0.47	0.53	$t_{CK(avg)}$	
Absolute clock period	$t_{CK(abs)}$	$t_{CK(avg)min}$ + $t_{JIT(per)min}$	$t_{CK(avg)max}$ + $t_{JIT(per)max}$	ps	
Absolute clock high pulse width	$t_{CH(abs)}$	0.43	-	$t_{CK(avg)}$	25
Absolute clock low pulse width	$t_{CL(abs)}$	0.43	-	$t_{CK(avg)}$	26
Clock period jitter	$t_{JIT(per)}$	-80	80	ps	
Clock period jitter during DLL locking period	$t_{JIT(per, lck)}$	-70	70	ps	
Cycle to cycle period jitter	$t_{JIT(CC)}$	160		ps	
Cycle to cycle period jitter during DLL locking period	$t_{JIT(CC, lck)}$	140		ps	
Duty cycle jitter	$t_{JIT(duty)}$	-	-	ps	
Cumulative error across 2 cycles	$t_{ERR(2per)}$	-118	118	ps	
Cumulative error across 3 cycles	$t_{ERR(3per)}$	-140	140	ps	
Cumulative error across 4 cycles	$t_{ERR(4per)}$	-155	155	ps	
Cumulative error across 5 cycles	$t_{ERR(5per)}$	-168	168	ps	
Cumulative error across 6 cycles	$t_{ERR(6per)}$	-177	177	ps	
Cumulative error across 7 cycles	$t_{ERR(7per)}$	-186	186	ps	
Cumulative error across 8 cycles	$t_{ERR(8per)}$	-193	193	ps	
Cumulative error across 9 cycles	$t_{ERR(9per)}$	-200	200	ps	
Cumulative error across 10 cycles	$t_{ERR(10per)}$	-205	205	ps	
Cumulative error across 11 cycles	$t_{ERR(11per)}$	-210	210	ps	
Cumulative error across 12 cycles	$t_{ERR(12per)}$	-215	215	ps	
Cumulative error across n = 13-50 cycles	$t_{ERR(nper)}$	$t_{ERR(nper)min} = (1 + 0.68\ln(n)) * t_{JIT(per)min}$ $t_{ERR(nper)max} = (1 + 0.68\ln(n)) * t_{JIT(per)max}$		ps	24

Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-1333		Units	Notes
		Min	Max		
Data Timing					
DQS, $\overline{DQS}$ to DQ skew, per group, per access	t_{DQSQ}	-	125	ps	13
DQ output hold time from DQS, $\overline{DQS}$	t_{QH}	0.38	-	$t_{CK(avg)}$	13, b
DQ low-impedance from CK, $\overline{CK}$	$t_{LZ(DQ)}$	-500	250	ps	13, 14, a
DQ high-impedance from CK, $\overline{CK}$	$t_{HZ(DQ)}$	-	250	ps	13, 14, a
Data setup time to DQS, $\overline{DQS}$ referenced to $V_{IH(AC)}$ / $V_{IL(AC)}$ levels	$t_{DS(base)}$	TBD	-	ps	17, d
Data hold time from DQS, $\overline{DQS}$ referenced to $V_{IH(DC)}$ / $V_{IL(DC)}$ levels	$t_{DH(base)}$	TBD	-	ps	17, d
Data Strobe Timing					
DQS, $\overline{DQS}$ differential READ preamble	t_{RPRE}	0.9	Note 19	$t_{CK(avg)}$	13, 19, b
DQS, $\overline{DQS}$ differential READ postamble	t_{RPST}	0.3	Note 11	$t_{CK(avg)}$	11, 13, b
DQS, $\overline{DQS}$ differential output high time	t_{QSH}	0.4	-	$t_{CK(avg)}$	13, b
DQS, $\overline{DQS}$ differential output low time	t_{QSL}	0.4	-	$t_{CK(avg)}$	13, b
DQS, $\overline{DQS}$ differential WRITE preamble	t_{WPRE}	0.9	-	$t_{CK(avg)}$	
DQS, $\overline{DQS}$ differential WRITE postamble	t_{WPST}	0.3	-	$t_{CK(avg)}$	
DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$	t_{DQSCK}	-255	255	ps	13, a
DQS and $\overline{DQS}$ low-impedance time (Referenced from RL - 1)	$t_{LZ(DQS)}$	-500	250	ps	13, 14, a
DQS and $\overline{DQS}$ low-impedance time (Referenced from RL + BL / 2)	$t_{HZ(DQS)}$	-	250	ps	13, 14, a
DQS, $\overline{DQS}$ differential input low pulse width	t_{DQSL}	0.4	0.6	$t_{CK(avg)}$	
DQS, $\overline{DQS}$ differential input high pulse width	t_{DQSH}	0.4	0.6	$t_{CK(avg)}$	
DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge	t_{DQSS}	-0.25	0.25	$t_{CK(avg)}$	c
DQS, $\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge	t_{DSS}	0.2	-	$t_{CK(avg)}$	c
DQS, $\overline{DQS}$ falling edge hold time from CK, $\overline{CK}$ rising edge	t_{DSH}	0.2	-	$t_{CK(avg)}$	c

Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-1333		Units	Notes
		Min	Max		
Command and Address Timing					
DLL locking time	t_{DLLK}	512	-	nCK	
Internal READ command to PRECHARGE command delay	t_{RTP}	max (4nCK, 7.5ns)	-		e
Delay from start of internal write transaction to internal READ command	t_{WTR}	max (4nCK, 7.5ns)	-		18, e
WRITE recovery time	t_{WR}	15	-	ns	e
Mode Register Set command cycle time	t_{MRD}	4	-	nCK	
Mode Register Set command update delay	t_{MOD}	max (12nCK, 15ns)	-		
ACT to internal read or write delay time	t_{RCD}	Refer to Speed Bin on page 28			e
PRECHARGE command period	t_{RP}	Refer to Speed Bin on page 28			e
ACT to ACT or REF command period	t_{RC}	Refer to Speed Bin on page 28			e
$\overline{CAS}$ to $\overline{CAS}$ command delay	t_{CCD}	4	-	nCK	
Auto-precharge write recovery + precharge time	$t_{DAL(min)}$	WR + roundup (t_{RP} / $t_{CK(avg)}$)		nCK	
Multi-purpose register recovery time	t_{MPRR}	1	-	nCK	22
ACTIVE to PRECHARGE command period	t_{RAS}	Refer to Speed Bin on page 28			e
ACTIVE to ACTIVE command period for 1KB page size	t_{RRD}	max (4nCK, 6ns)	-		e
Four activate window for 1KB page size	t_{FAW}	30	-	ns	e
Command and Address setup time to CK, $\overline{CK}$ referenced to $V_{IH(AC)}$ / $V_{IL(AC)}$ levels	$t_{IS(base)}$	65	-	ps	16, b
Command and Address hold time to CK, $\overline{CK}$ referenced to $V_{IH(DC)}$ / $V_{IL(DC)}$ levels	$t_{IH(base)}$	140	-	ps	16, b
Command and Address setup time to CK, $\overline{CK}$ referenced to $V_{IH(AC)}$ / $V_{IL(AC)}$ levels	$t_{IS(base)}$ AC150	65 + 125	-	ps	16, 27, b
Calibration Timing					
Power-up and RESET calibration time	t_{ZQinit}	512	-	nCK	
Normal operation Full calibration time	t_{ZQoper}	256	-	nCK	
Normal operation Short calibration time	t_{ZQCS}	64	-	nCK	23

Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-1333		Units	Notes
		Min	Max		
Reset Timing					
Exit Reset from CKE HICH to a valid command	t_{XPR}	max (5nCK, t_{RFC}(min) + 10ns)	-		
Self Refresh Timing					
Exit Self Refresh from to commands not requiring a locked DLL	t_{XS}	max (5nCK, t_{RFC}(min) + 10ns)	-		
Exit Self Refresh from to commands requiring a locked DLL	t_{XSDLL}	t_{DLLK}(min)	-	nCK	
Minimum CKE low width for Self Refresh entry to exit timing	t_{CKESR}	t_{CKE}(min) + 1nCK	-		
Valid clock requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	t_{CKSRE}	max (5nCK, 10ns)	-		
Valid clock requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	t_{CKSRX}	max (5nCK, 10ns)	-		
Power Down Timing					
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	t_{XP}	max (3nCK, 7.5ns)	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	t_{XPDLL}	max (10nCK, 24ns)	-		2
Command pass disable delay	t_{CPDED}	1	-	nCK	
Power Down Entry to Exit Timing	t_{PD}	t_{CKE}(min)	9 * t_{REFI}		15
Timing of ACT command to Power Down entry	$t_{ACTPDEN}$	1	-	nCK	20
Timing of PRE or PREA command to Power Down entry	t_{PRPDEN}	1	-	nCK	20
Timing of RD/RDA command to Power Down entry	t_{RDPDEN}	RL + 4 + 1	-	nCK	
CKE minimum pulse width	t_{CKE}	max (3nCK, 5.625ns)	-	nCK	

Device Timing Parameters by Speed Bin (Contd.)

Parameter	Symbol	DDR3-1333		Units	Notes
		Min	Max		
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	t_{WRPDEN}	WL + 4 + (t_{WR} / $t_{CK(avg)}$)	-	nCK	9
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	$t_{WRAPDEN}$	WL + 4 + WR + 1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	t_{WRPDEN}	WL + 2 + (t_{WR} / $t_{CK(avg)}$)	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	$t_{WRAPDEN}$	WL +2 + WR + 1	-	nCK	10
Timing of REF command to Power Down entry	$t_{REFPDEN}$	1	-	nCK	20, 21
Timing of MRS command to Power Down entry	$t_{MRSPDEN}$	t_{MOD}(min)	-		
ODT Timing					
ODT high time without Write command or with Write command and BC4	ODTH4	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	t_{AONPD}	1	9	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	t_{AOFPD}	1	9	ns	
RTT turn-on	t_{AON}	-250	250	ps	7, a
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	t_{AOF}	0.3	0.7	$t_{CK(avg)}$	8, a
RTT dynamic change skew	t_{ADC}	0.3	0.7	$t_{CK(avg)}$	a
Write Leveling Timing					
First DQS/$\overline{DQS}$ rising edge after write leveling mode is programmed	t_{WLMRD}	40	-	nCK	3
DQS/$\overline{DQS}$ delay after write leveling mode is programmed	$t_{WLDQSEN}$	25	-	nCK	3
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	t_{WLS}	195	-	ps	
Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing	t_{WLH}	195	-	ps	
Write leveling output delay	t_{WLO}	0	9	ns	
Write leveling output error	t_{WLOE}	0	2	ns	

Device Timing Parameters Notes

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in the Mode Register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, t_{REFI}.
7. Minimum RTT turn-on time (*t*AONmin) is the point in time when the device leaves high impedance and ODT resistance begins to turn on. Maximum RTT turn on time (*t*AONmax) is the point in time when the ODT resistance is fully on. Both are measured from ODTLon.
8. Minimum RTT turn-off time (*t*AOFmin) is the point in time when the device starts to turn off the ODT resistance. Maximum RTT turn off time (*t*AOFmax) is the point in time when the on-die termination has reached high impedance. Both are measured from ODTLoff.
9. t_{WR} is defined in ns, for calculation of t_{WRPDEN} it is necessary to round up t_{WR} / t_{CK} to the next integer.
10. WR is in clock cycles as programmed in MR0.
11. The maximum postamble is bound by t_{HZDQS}(max)
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD.
13. Value is only valid for RON34
14. Single ended signal parameter.
15. t_{REFI} depends on T_{OPER}.
16. $t_{IS(base)}$ and $t_{IH(base)}$ values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{CK}$ differential slew rate. Note for DQ and DM signals, $V_{REF(DC)} = V_{REFDQ(DC)}$. For input only pins except $\overline{RESET}$, $V_{REF(DC)} = V_{REFCA(DC)}$.
17. $t_{DS(base)}$ and $t_{DH(base)}$ values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{DQS}$ differential slew rate. Note for DQ and DM signals, $V_{REF(DC)} = V_{REFDQ(DC)}$. For input only pins except $\overline{RESET}$, $V_{REF(DC)} = V_{REFCA(DC)}$.
18. Start of internal write transaction is defined as follows:
    For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
19. The maximum preamble is bound by t_{LZDQS}(min).
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once $t_{REFPDEN}$(min) is satisfied, there are cases where additional time such as t_{XPDLL}(min) is also required.
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters.
    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{ZQCorrection}{(TSens \times Tdriftrate) + (VSens \times TVdriftrate)}$$

    where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.
    For example, if TSens = 1.5% / °C, VSens = 0.15% / mV, Tdriftrate = 1 °C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1) + (0.15 + 15)} = 0.133 \approx 128ms$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. $t_{CH(abs)}$ is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. $t_{CL(abs)}$ is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The $t_{IS(base)}$ AC150 specifications are adjusted from the $t_{IS(base)}$ specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].

Jitter Notes

a When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{ERR(mper)}$act of the input clock, where $2 \leq m \leq 12$. (Output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR3-800 SDRAM has $t_{ERR(mper)}$act,min = - 172 ps and $t_{ERR(mper)}$act,max = + 193 ps, then t_{DQSCK}min(derated) = t_{DQSCK}min - $t_{ERR(mper)}$act,max = - 400 ps - 193 ps = - 593 ps and t_{DQSCK}max(derated) = t_{DQSCK},max - $t_{ERR(mper)}$act,min = 400 ps + 172 ps = + 572 ps. Similarly, $t_{LZ(DQ)}$ for DDR3-800 derates to $t_{LZ(DQ)}$min(derated) = - 800 ps - 193 ps = - 993 ps and $t_{LZ(DQ)}$max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!)
Note that $t_{ERR(mper)}$act,min is the minimum measured value of $t_{ERR(nper)}$ where $2 \leq n \leq 12$, and $t_{ERR(mper)}$act,max is the maximum measured value of $t_{ERR(nper)}$ where $2 \leq n \leq 12$.

b When the device is operated with input clock jitter, this parameter needs to be derated by the actual $t_{JIT(per)}$,act of the input clock. (Output deratings are relative to the SDRAM input clock.)

For example, if the measured jitter into a DDR3-800 SDRAM has $t_{CK(avg)}$act = 2500 ps, $t_{JIT(per)}$act,min = - 72 ps and $t_{JIT(per)}$act,max = + 93 ps, then t_{RPRE}min(derated) = t_{RPRE}min + $t_{JIT(per)}$act,min = 0.9 x $t_{CK(avg)}$act + $t_{JIT(per)}$act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, t_{QH}min(derated) = t_{QH}min + $t_{JIT(per)}$act,min = 0.38 x $t_{CK(avg)}$act + $t_{JIT(per)}$act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

c These parameters are measured from a data strobe signal (DQS, $\overline{DQS}$) crossing to its respective clock signal (CK, $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

d These parameters are measured from a data signal (DM, DQ0, DQ1, etc.) transition edge to its respective data strobe signal (DQS, $\overline{DQS}$) crossing.

e For these parameters, the DDR3 SDRAM device supports t_{nPARAM} [nCK] = RU{t_{PARAM} [ns] / $t_{CK(avg)}$ [ns]}, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support t_{nRP} = RU{t_{RP} / $t_{CK(avg)}$}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which t_{RP} = 15ns, the device will support t_{nRP} = RU{t_{RP} / $t_{CK(avg)}$} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15 ns due to input clock jitter.

Part Number Decode

S	G	256	7	RD3	128	9	3	U	U	D
1	2	3	4	5	6	7	8	9	10	11

1 **SMART Modular Technologies**

2 **Module Process Technology**
G: Green Module (RoHS Compliant)

3 **Module Address Depth**
256: 256M

4 **Module Data Bus Width**
7: x72

5 **Module Configuration**
RD3: DDR3 Registered DIMM

6 **Device Configuration**
128: 128Mx8

7 **CAS Latency**
9: CL 9.0

8 **Module Speed**
3: DDR3-1333

9 **Device Vendor**
H: Hynix
S: Samsung

10 **Device Revision**
B: Revision B
D: Revision D
E: Revision E

11 **Register**
D: IDT register

Note: “U” in the part number should be replaced by user specified option.

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