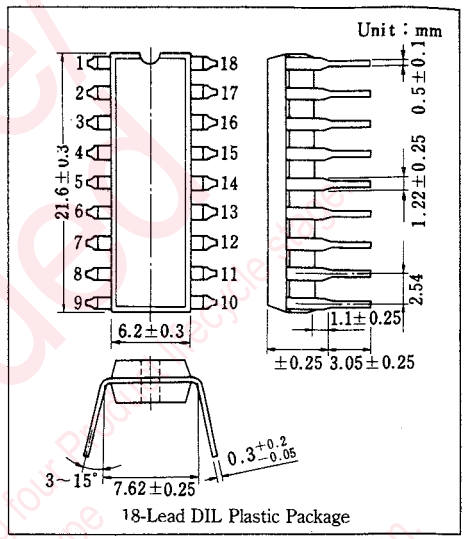
AN6346N

VTR Cylinder Interface Circuit

■ Outline

The AN6346N is an integrated circuit designed for VTR cylinder interface.

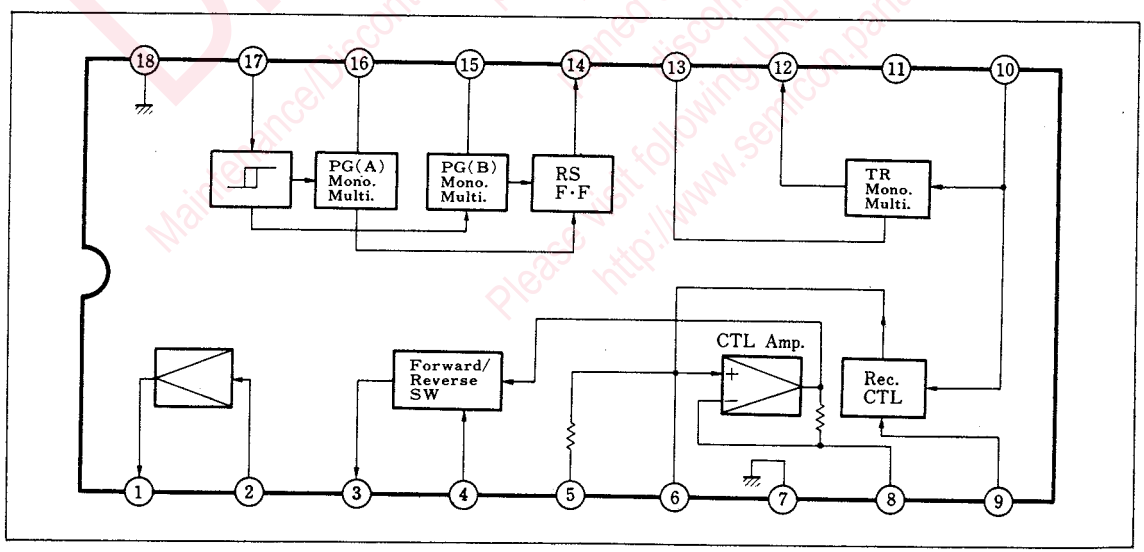


18-Lead DIL Plastic Package

■ Features

- The functions consist of:
  - PG monostable multivibrator
  - Tracking monostable multivibrator
  - CTL amplifier
- Supply voltage: 5V

■ Block Diagram



■ Pin

Pin No.	Pin Name		Pin No.	Pin Name
1	P.B. CTL Output		10	1/2 V_{ss} Input
2	P.B. CTL Clamp Input		11	V_{cc}
3	P.B. CTL Amp. Output		12	Tracking Mono. Multi. Output
4	Forward/Reverse Select		13	Tracking Mono. Multi. Control
5	1/2 V_{cc}		14	Head Switch Output
6	CTL Signal	Input(P.B.)	15	PG (B) Mono. Multi.
		Output(Rec.)	16	PG (A) Mono. Multi.
7	GND		17	Cylinder PG Input
8	CTL Amp. Feedback		18	GND
9	Rec./P.B. Select		—	———

■ Absolute Maximum Ratings (Ta=25℃)

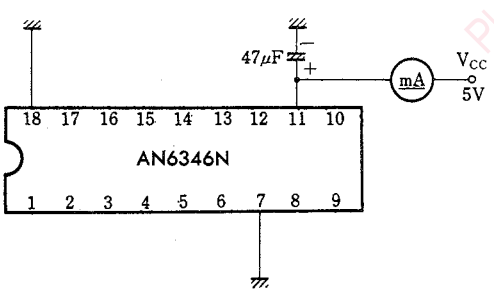
Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	6	V
Power dissipation (Ta=70℃)	P_D	100	mW
Operating ambient temperature	T_{opr}	−20～+70	℃
Storage temperature	T_{stg}	−40～+150	℃

■ Electrical Characteristics (V_{CC}= 5 V, Ta=25℃ ± 2 ℃)

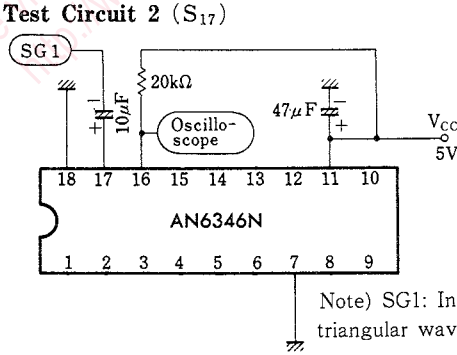
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit current	I_{11}	1	Without load	7.0		14	mA
PG amp. input sensitivity	S_{17}	2		±65			mV
PG A mono. multi. delay amount	T_{16}	3	C=0.056 μF, R=20 kΩ	690		860	μs
PG B mono. multi. delay amount	T_{15}	3	C=0.056 μF, R=20 kΩ	690		860	μs
H/SW high-level output	V_{OH14}	4	Without load	4.6			V
H/SW low-level input	V_{OL14}	4	Without load			0.4	V
1/2 V_{ss} input sensitivity	S_{10}	5				1.5	V
Rec. start select sensitivity	S_9	6		3.0			V
For/Rev. select sensitivity	S_4	7		3.0			V
Rec. CTL high-level output	V_{OH6}	8	Without load	4.0			V
Rec. CTL low-levelvel output	V_{OL6}	8	Without load			0.4	V
P.B. CTL amp. gain (For.)	G_{F3}	9	Without load	60		72	dB
P.B. CTL amp. gain (Rev.)	G_{R3}	9		59		72	dB
Tracking mono. multi. delay amount	T_{13}	10	C=0.27 μF, R=100 kΩ	18		22	ms
P.B. CTL wave shaping input sensitivity	S_2	11		300			mV

Note) Operating supply voltage range $V_{CC(opr)}$ 4.5～5.5V

Test Circuit 1 (I_{11})

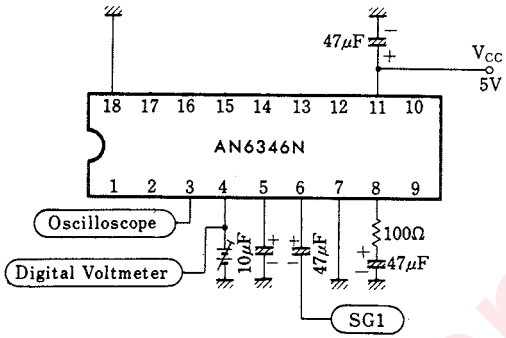


Test Circuit 2 (S_{17})



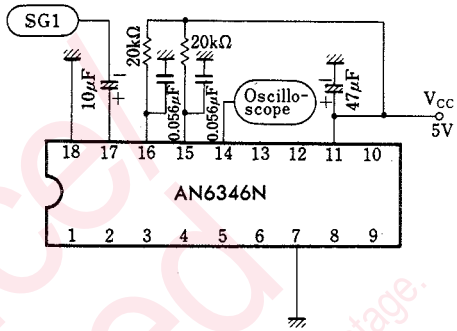
Note) SG1: Input signal triangular wave, f=100Hz

Test Circuit 3 (T_{16}, T_{15})



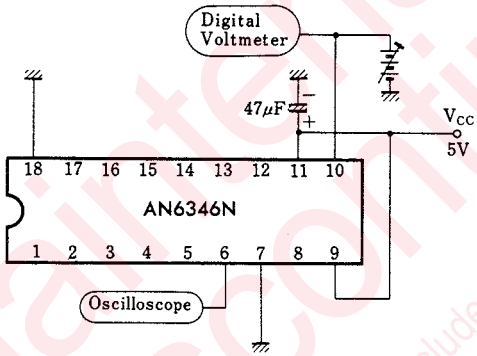
Note) SG1: Input signal sine wave f=1kHz, 0.2mVp−p

Test Circuit 4 (V_{OH14}, V_{OL14})



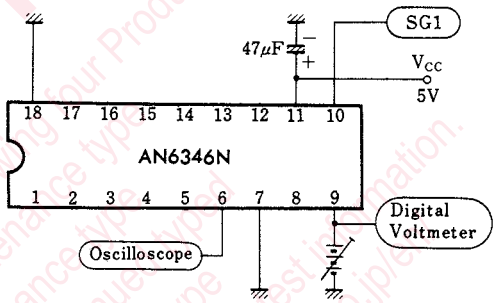
Note) SG1: Input signal triangular wave, f=100Hz,1Vp−p

Test Circuit 5 (S_{10})



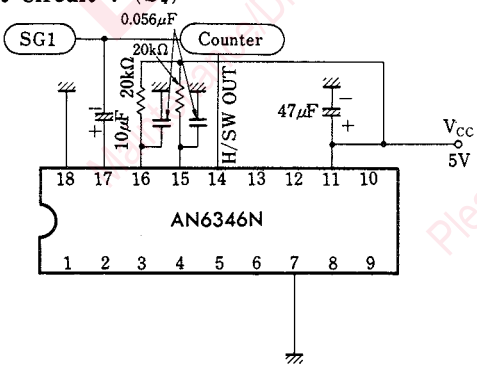
Note) Measure the Pin⑩ voltage at which Pin⑥ output changes after IC internal R−S FF setting-(applying pulses to the Pin⑩ in the circuit above).

Test Circuit 6 (S_9)



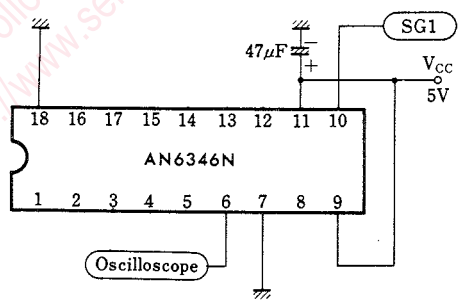
Note) SG1: Input signal rectangular wave, f=30Hz, 5Vo−p. Measure the Pin⑨ voltage at which no output is made to the Pin⑥.

Test Circuit 7 (S_4)



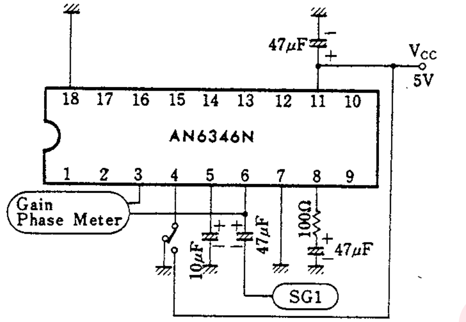
Note) SG1: Input signal rectangular wave, f=100Hz, 1Vp-p. T_{15} is a time from a fall of SG1 input signal to a rise of H/SW.OUT. T_{16} is a time from a rise of SG1 input signal to a fall of H/SW OUT.

Test Circuit 8 (V_{OH6}, V_{OL6})



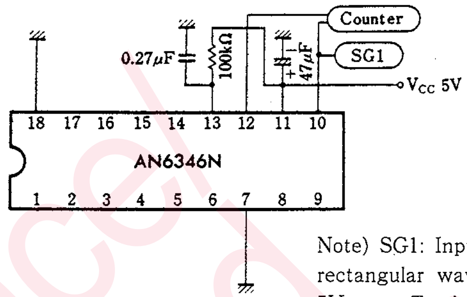
Note) SG1: Input signal rectangular wave, f=30Hz, 5Vo−p

Test Circuit 9 (G_{F3}, G_{R3})



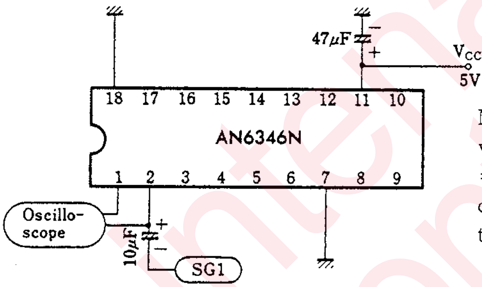
Note) SG1: Input signal sine wave, f=1kHz, 0.2mVp−p. G_{F3} for Pin④ GND, G_{R3} for Pin④ Vcc

Test Circuit 10 (T_{13})



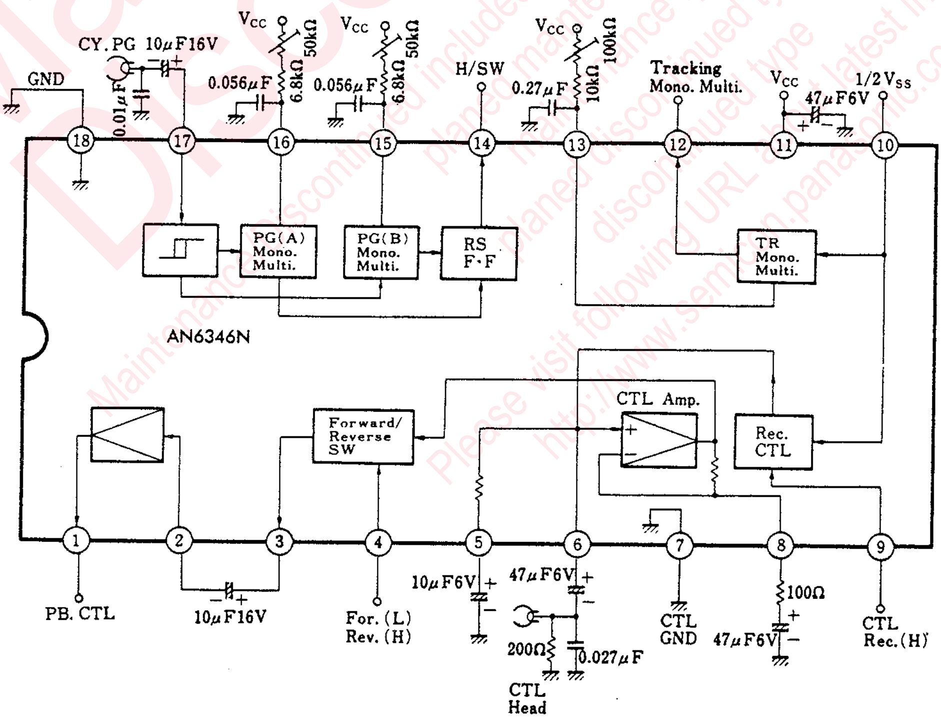
Note) SG1: Input signal rectangular wave, f=30Hz, 5Vo−p. T_{13} is a time from a rise of SG1 to a fall of Pin⑫ output.

Test Circuit 11 (S_2)



Note) SG1: Input signal rectangular wave, f=30Hz. $V_H - V_L$ of SG1 $= S_2$ when an SG1 signal level is changed and a signal is issued to the Pin①

■ Application Circuit


Vcc
50kΩ
Vcc
50kΩ
Vcc
100kΩ
CY.PG 10μF16V
GND
0.01μF
0.056μF
6.8kΩ
0.056μF
6.8kΩ
H/SW
0.27μF
10kΩ
Tracking
Mono. Multi.
Vcc
1/2Vss
47μF6V
18
17
16
15
14
13
12
11
10
PG(A)
Mono.
Multi.
PG(B)
Mono.
Multi.
RS
F·F
TR
Mono.
Multi.
AN6346N
CTL Amp.
Forward/
Reverse
SW
Rec.
CTL
1
2
3
4
5
6
7
8
9
PB. CTL
10μF16V
For. (L)
Rev. (H)
10μF6V
47μF6V
200Ω
0.027μF
CTL
Head
CTL
GND
100Ω
47μF6V
CTL
Rec. (H)

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