PRELIMINARY

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

DESCRIPTION

The SC1405C dual high speed MOSFET Driver provides a complete solution to driving MOSFETS in synchronous converters. The SC1405C features internal overlap protection to ensure that low-side FET does not turn on until the high-side FET has turned off. Each gate output drives a 3000pF load in 15ns rise/fall time and has ultra fast propagation delay to the gate of the power FET's. The delay between the low-side gate going low to the high-side gate switching high is externally programmable via a capacitor for optimal reduction of switching losses at the desired operating frequency. The low-side FET may be disabled at light loads by keeping MODE low to trigger asynchronous operation, thus saving it's gate drive current and inductor ripple current. The SC1405C provides overvoltage protection independent of the PWM feedback loop with a unique "adaptive OVP" comparator which rejects noise but responds quickly to a real OVP situation. Under-voltage lock-out circuitry guarantees both driver outputs are low when the 5V power supply is less than or equal to 4.4V (typ) at supply ramp up (4.35V at supply ramp down). A CMOS output indicates the status of the 5V supply. A logic low on the enable input places the IC in stand-by mode reducing supply current to less than 10µA. SC1405C is offered in a TSSOP package.

FEATURES

- Fast rise and fall times (15ns with 3000pf load)
- 14ns max. propagation delay (BG going low)
- Adaptive/programmable shoot-through protection
- Wide input voltage range (4.5-25V)
- Programmable delay between MOSFET's
- Power saving asynchronous mode control
- Adaptive overvoltage protection
- Internal thermal shutdown
- Under-Voltage lock-out
- Less than 10µA stand-by current (EN=low)
- Power ready output signal
- High frequency (to 1.2MHz) operation allows use of small inductors and low cost capacitors

APPLICATIONS

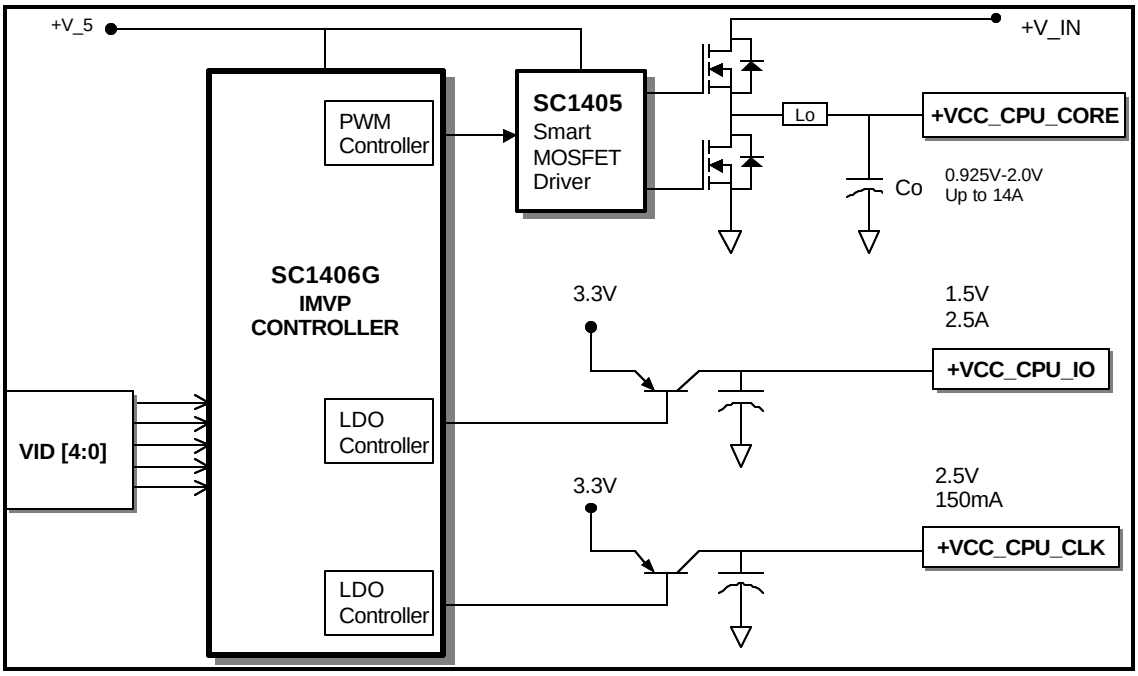
- High density, fast response power supplies
- Motor Drives/Class-D amps
- Portable computers

ORDERING INFORMATION

DEVICE(1)	PACKAGE	TEMP. RANGE (T_J)
SC1405CTS	TSSOP-14	0 - 125°C

Note:
(1) Add suffix 'TR' for tape and reel.

CONCEPTUAL APPLICATION CIRCUIT



652 MITCHELL ROAD NEWBURY PARK CA 91320

PRELIMINARY

ABSOLUTE MAXIMUM RATINGS

PARAMETER	MAXIMUM	UNITS
V_{CC} Supply Voltage	-0.3 to 7	V
BST to PGND	-0.3 to 30	V
BST to DRN (Steady-state)	-0.3 to 7	V
BST to DRN (Transient, < 100nS)	-0.3 to 8	V
DRN to PGND	-2 to 25	V
OVP to PGND	-0.3 to 10	V
EN, CO, DSPS, MODE, PRDY, DELAY, to AGND	-0.3 to 7.3	V
AGND to PGND	-1 to 1	V

THERMAL RATINGS

PARAMETER	SYMBOL	CONDITIONS	MAXIMUM	UNITS
Continuous Power Dissipation	Pd	Tamb = 25°C, T_J = 125°C	0.66	W
Thermal Resistance Junction to Case	θ_{JC}	40	40	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	150	150	°C/W
Operating Junction Temperature Range	T_J	0 to +125	0 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	-65 to +150	°C
Lead Temperature (Soldering) 10 sec	T_{LEAD}	300	300	°C

ELECTRICAL CHARACTERISTICS (DC OPERATING SPECIFICATIONS)

Unless specified: -0 < θ_J < 125°C; V_{CC} = 5V; 4V ≤ V_{BST} ≤ 26V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	VCC		4.15	5	6.0	V
Quiescent Current	Iq	EN = 0V			10	µA
Quiescent Current, operating	Iq	V_{CC} = 5V,CO=0V		1		mA
PRDY						
High Level Output Voltage		V_{CC} = 4.6V, Iload = 10mA	4.5	4.55		V
Low Level Output Voltage		V_{CC} < UVLO threshold, Iload = 10µA		0.1	0.2	V
DSPS_DR						
High Level Output Voltage		V_{CC} = 4.6V, Cload = 100pF	4.15			V
Low Level Output Voltage		V_{CC} = 4.6V, Cload = 100pF			0.05	V
UNDER-VOLTAGE LOCKOUT						
Start Threshold			4.2	4.4	4.6	V
Hysteresis	Vhys			0.05		V
Logic Active Threshold		EN is low			1.5	V

NOTE: (1) Specification refers to application circuit in Figure 1.

PRELIMINARY

ELECTRICAL CHARACTERISTICS (DC OPERATING SPECIFICATIONS) Cont.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OVERVOLTAGE PROTECTION						
Trip Threshold			1.145	1.2	1.255	V
Hysteresis				0.8		V
Trip Delay, 50mV Overdrive		t = 0 to 125ºC	300	470	800	ns
Trip Delay, 100mV Overdrive		t = 0 to 125ºC	125	225	400	ns
S_MOD						
High Level Input Voltage			2.0			V
Low Level Input Voltage					0.8	V
ENABLE						
High Level Input Voltage			2.0			V
Low Level Input Voltage					0.8	V
CO						
High Level Input Voltage			2.0			V
Low Level Input Voltage					0.8	V
THERMAL SHUTDOWN						
Over Temperature Trip Point				165		°C
Hysteresis				10		°C
HIGH-SIDE DRIVER						
Peak Output Current				2		A
Output Resistance		duty cycle < 2%, tpw < 100µs, T_J = 125°C, V_{BST} - V_{DRN} = 4.5V, V_{TG} = 4.0V source+V_{DRN} or V_{TG} = 0.5V (sink)+V_{DRN}		1 .7		Ω Ω
LOW-SIDE DRIVER						
Peak Output Current				2		A
Output Resistance		duty cycle < 2%, tpw < 100µs, T_J = 125°C VCC = 4.6V, V_{BG} = 4V source, or VBG = 0.5V (sink)		1.2 1.0		Ω Ω

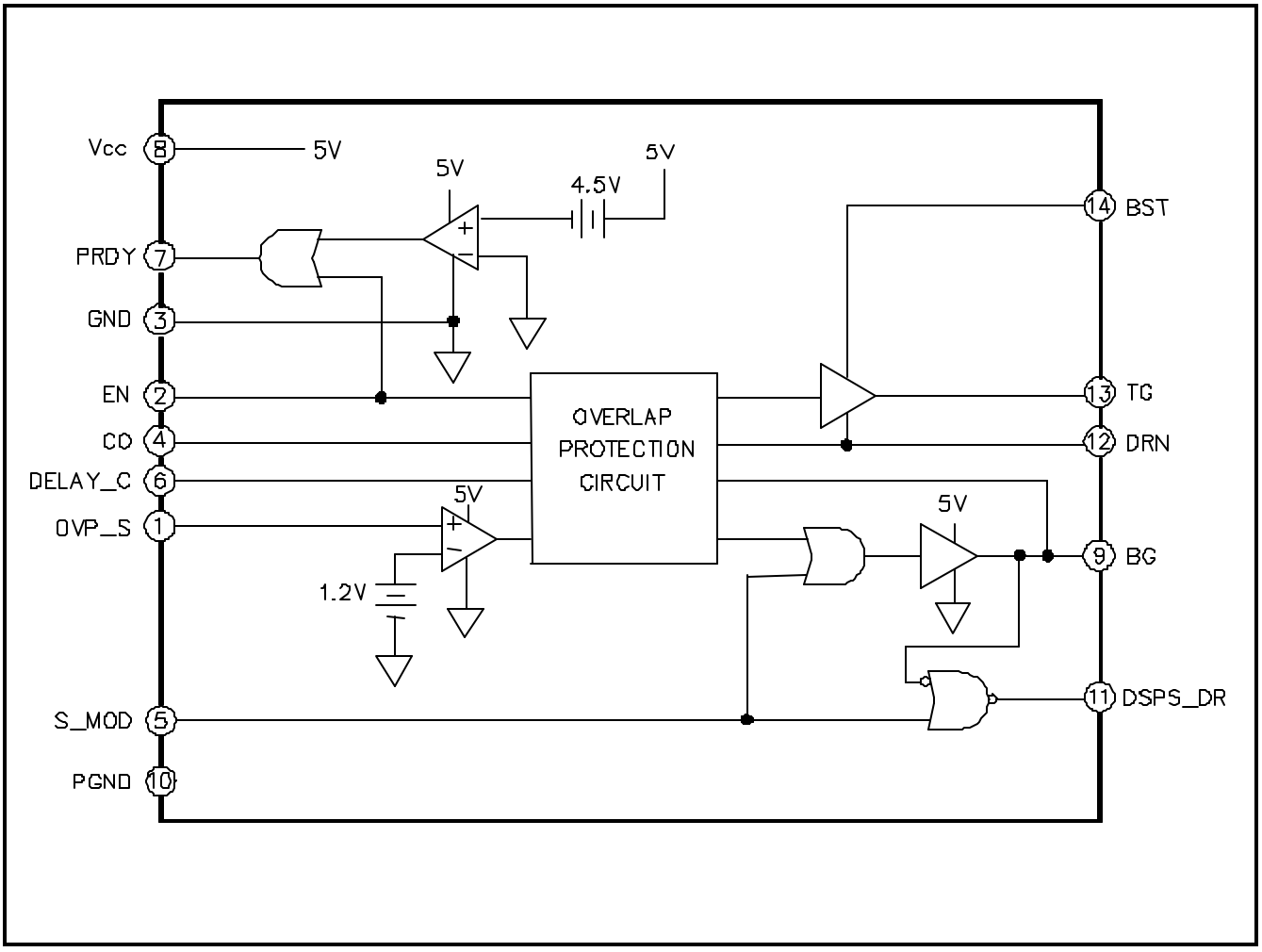
PRELIMINARY

ELECTRICAL CHARACTERISTICS (DC OPERATING SPECIFICATIONS) Cont.

PARAMETER	SYMBO	CONDITIONS	MIN	TYP	MAX	UNITS
AC OPERATING SPECIFICATIONS						
HIGH-SIDE DRIVER (see Fig. 2)						
Rise time	tr_{TG},	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V,		14	23	ns
Fall time	tf_{TG}	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V,		12	19	ns
Propagation delay time, TG going high	$tpdh_{TG}$	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V, C-delay=0		20	32	ns
Propagation delay time, TG going low	$tpdl_{TG}$	Cl = 3nF, V_{BST} - V_{DRN} = 4.6V,		15	24	ns
LOW-SIDE DRIVER (see Fig. 2)						
Rise time	tr_{BG}	Cl = 3nF, V_{V_5} = 4.6V,		15	24	ns
Fall time	tr_{BG}	Cl = 3nF, V_{V_5} = 4.6V,		13	21	ns
Propagation delay time	$tpdh_{BGHI}$	Cl = 3nF, V_{V_5} = 4.6V,		12	19	ns
Progagation delay time	$tpdl_{BG}$	Cl = 3nF, V_{V_5} = 4.6V,		7	12	ns
UNDER-VOLTAGE LOCKOUT						
VCC ramping up propogation delay	$tpdh_{UVLO}$	EN is High			10	us
VCC ramping down delay	$tpdl_{UVLO}$	EN is High			10	us
PROPOGATION DELAY						
EN is transitioning from low to high		VCC $\geq$ UVLO threshold, Delay measured from EN $\geq$ 2.0V to PRDY			10	µs
EN is transitioning from high to low		VCC $\geq$ UVLO threshold. Delay measured from EN $\leq$ 0.8V tp PRDY			500	µs
DSPS_DR						
Rise/fall time		Cl = 100pf, VCC = 4.6V,			20	ns
Propagation delay,		S_MOD goes high and			10	ns
Propagation delay		S_MOD goes high and BG goes low			10	ns
OVERVOLTAGE PROTECTION						
Propagation delay OVP_S going high		VCC = 4.6V, T_J = 125°C, OVP_S $\geq$ 1.2V to BG > 90% of VCC			1	µs

PRELIMINARY

BLOCK DIAGRAM



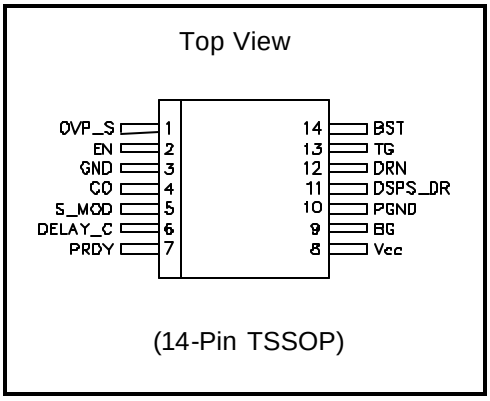
PRELIMINARY

PIN DESCRIPTION

Pin #	Pin Name	Pin Function
1	OVP	Overvoltage protection sense. External scaling resistors required to set
2	EN	When high, this pin enables the internal circuitry of the device. When low, TG, BG and PRDY are forced low and the supply current (VCC) is
3	GND	Logic GND.
4	CO	TTL-level input signal to the MOSFET drivers.
5	MODE	When low, this signal forces BG to be low. When high, BG is the inverse of CO.
6	DELAY	Sets the additional propagation delay for BG going low to TG going
7	PRDY	This pin indicates the status of 5V. When 5V is less than 4.4V(typ) this output is driven low. When 5V is greater than or equals to 4.4V(typ) this output is driven to 5V level. This output has a 10mA drive capability and
8	V_{CC}	+5V supply. A .22-1µF ceramic capacitor should be connected from 5V
9	BG	Output drive for the synchronous (low-side) MOSFET.
10	PGND	Power ground. Connect to the synchronous FET power ground.
11	DSPOUT	Dynamic Set Point Switch Drive. TTL level output signal. When S_MOD
12	DRN	This pin connects to the junction of the switching and synchronous MOSFET's. This pin can be subjected to a -2V minimum relative to
13	TG	Output gate drive for the switching (high-side) MOSFET.
14	BST	Bootstrap pin. A capacitor is connected between BST and DRN pins to develop the floating bootstrap voltage for the high-side MOSFET. The

NOTE: (1) All logic level inputs and outputs are open collector TTL compatible.

PIN CONFIGURATION



PRELIMINARY

APPLICATION CIRCUIT

Typical Distributed Power Supply

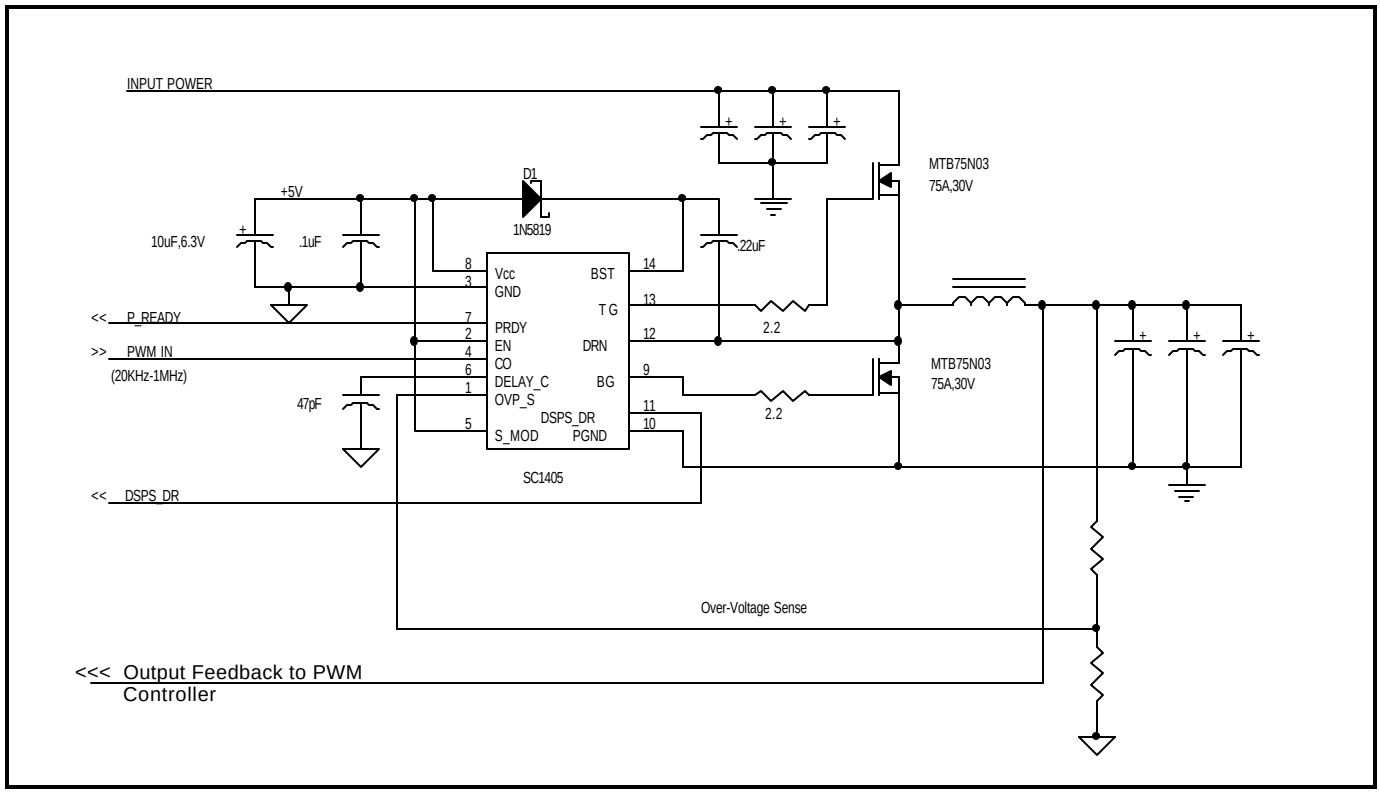


Figure 1.

TIMING DIAGRAM

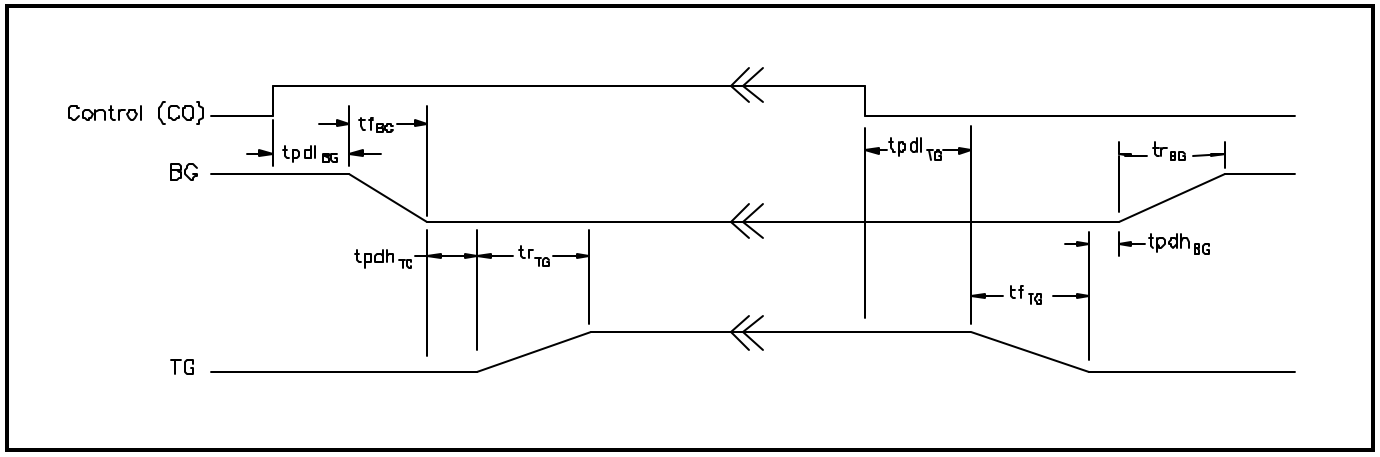


Figure 2.

PRELIMINARY

Figure 3 - APPLICATION EVALUATION BOARD SCHEMATIC

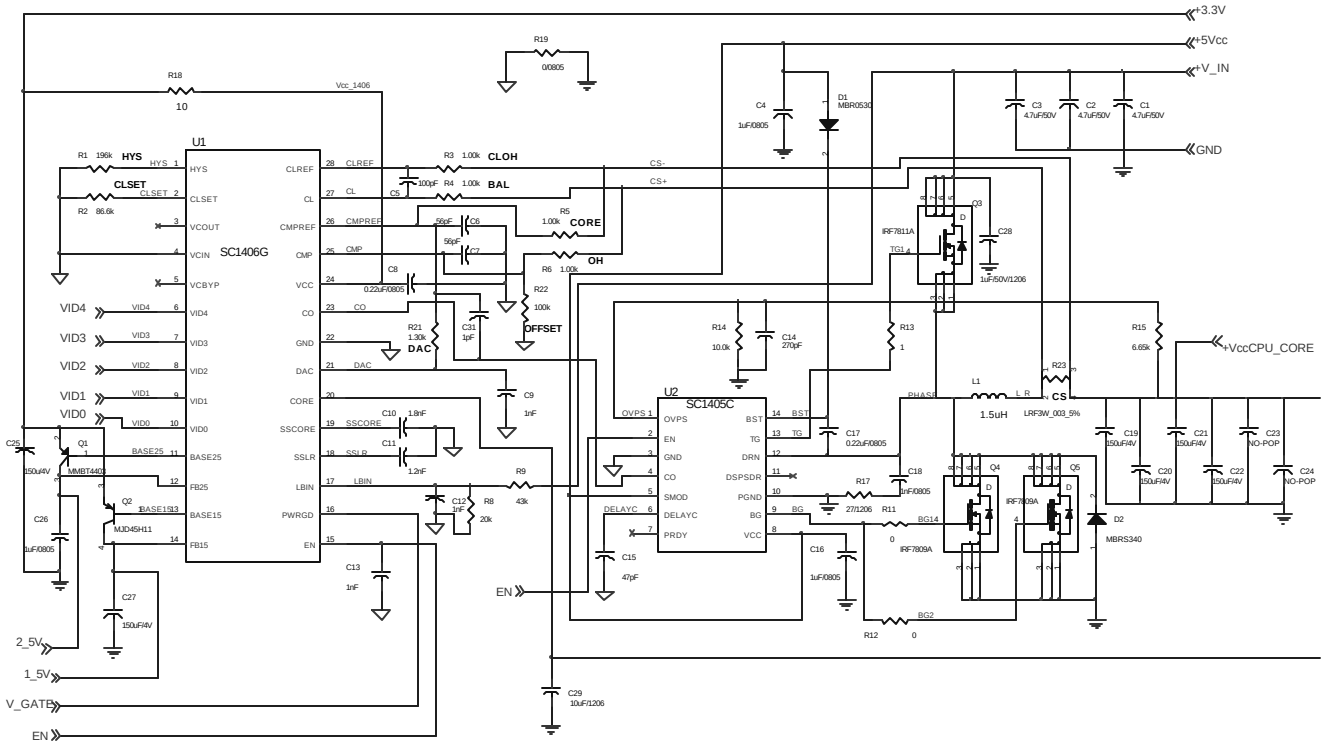


Figure 3

PRELIMINARY

APPLICATION INFORMATION:

SC1405C is the newest high speed driver in the SC1405 family. It drives low R_{DS_ON} power MOSFETs with rapid rise/fall times and propagation delays. As PWM converter frequency increases to reduce power stage volume and cost, fast rise and fall times are necessary to minimize switching losses of the high-side FET and reduce dead-time of the low-side FET. While low R_{DS_ON} MOSFETs have lower conduction (I^2R) losses, their die area is larger and the input capacitance of the FET is higher. Faster drivers are required to reduce the resulting switching losses. Often a 50% decrease in R_{DS_ON} more than doubles the required input gate charge supplied by the driver. The R_{DS_ON} power savings can be offset by the switching and dead-time losses with a sub-optimum driver. While discrete solutions can achieve reasonable drive capability, implementing shoot-through, programmable delay and other housekeeping functions necessary for high reliability is cumbersome and costly. The SC1405 family of parts presents a total solution for the high-speed, high power density applications. The wide input supply range of 4.5V-25V allows use in battery powered applications, new high voltage, distributed power servers as well as Class-D amplifiers.

THEORY OF OPERATION

The control input (CO) to the SC1405C is typically supplied by a PWM controller that regulates the power supply output. (See Application Evaluation Schematic, Figure 3). The timing diagram demonstrates the sequence of events by which the top and bottom drive signals are applied. The shoot-through protection is implemented by holding the bottom FET off until the voltage at the phase node (intersection of top FET source, the output inductor and the bottom FET drain) has dropped below 1V. This assures that the top FET has turned off and that a direct current path does not exist between the input supply and ground, a condition which both the top and bottom FETs are on momentarily. The top FET is also prevented from turning on until the bottom FET is off. This time is internally set to 20ns (typical) and may be increased by adding a capacitor to the DELAY pin. The additional delay is approximately 1ns/pf. The external capacitor is recommended when multiple low R_{DS_ON} MOSFETs are used in parallel and the fall time is greater than 20ns.

Please note that excessive values of delay capacitor reduces efficiency since the parallel Schottky or the bottom FET body diode conducts during dead-time.

LAYOUT GUIDELINES

As with any high speed, high current circuit, proper layout is critical in achieving optimum performance of the SC1405C. The evaluation board schematic (Refer to figure 3) shows a mobile CPU synchronous design with all surface mountable components.

While the placement and wiring of components connecting to DELAY, EN, MODE, DSPS and PRDY are not critical, tight placement and short, wide traces must be used in layout of TG, BG, DRN, OVP, and especially the PGND pin. The top gate driver supply voltage is provided by bootstrapping the +5V supply and adding it the phase node voltage (DRN). Since the bootstrap capacitor supplies the charge to the top gate driver, it must be less than .5" away from the SC1405. Ceramic X7R capacitors are a good choice for supply bypassing near the chip. The Vcc capacitor must also be less than .5" away from the SC1405. The ground node of this capacitor, the SC1405 PGND pin and the source of the low-side FET must be very close to each other, preferably with common PCB copper land and multiple vias to the ground plane (if used). The parallel Schottky must be physically next to the low-side FET drain and source. Any trace or lead inductance in these connections deflects current from the Schottky and allows it to flow through the FET's body diode, thus reducing efficiency.

PREVENTING INADVERTENT BOTTOM FET TURN-ON

Especially at high input voltages, (12V and greater) rapid turn-on of the high-side FET creates a positive going spike on the low-side FET's gate through the Miller capacitance, Crss of the low-side FET. The voltage appearing on the gate due to this spike is:

Vspike=Vin*Crss/(Crass+Ciss)

In this equation, Ciss is the input gate capacitance of the low-side FET, and assumes the impedance of the drive path is high compared to the instantaneous impedance of the capacitors, since dV/dT and thus the effective frequency is very high. If the BG pin of the SC1405C is very close to the low-side FET, Vspike is reduced, depending on trace inductance and the variables in the above equation.

While not shown in Figure 3, a capacitor may be

added from the gate of the low-side FET to its source, preferably less than .1" away. This capacitor increases Ciss in the above equation to reduce the effective spike voltage, Vspike. Pay attention to the Crss/Ciss ratio when selecting the low-side FET. A low ratio reduces the Miller feedback and thus reduces Vspike. Also, MOSFETs with higher threshold voltages conduct at a higher voltage and will not turn on during the spike. A zero ohm BG gate resistor help keep the gate voltage low. Ultimately, slowing down the top FET by adding gate resistance will reduce dV/dt which will in turn make the effective impedance of the capacitors higher, thus allowing the BG driver to hold the bottom gate voltage low.

RINGING ON THE PHASE NODE

The high-side MOSFET source must be close to the bottom MOSFET drain to reduce parasitic leakage inductances which drive the phase node negative, and produces the ringing on the phase node. This frequency is determined by:

F_{ring} =1/(2 $\prod$* Sqrt(L_{st}*Coss)), where:

L_{st} is the effective stray inductance of the high-side FET plus the trace inductance of the connection between the FET, plus the inductance of the low-side FET, plus to the interconnection inductance through the nearest high frequency decoupling capacitor.

Coss = Drain to source capacitance of bottom FET. If there is a Schottky used, the capacitance of the Schottky is added to the value.

Although this ringing does not pose significant power losses due to a fairly high Q, it may cause the phase node to go too far negative, thus causing improper operation, double pulsing or at worst driver damage. This ringing is also an EMI nuisance due to its high resonant frequency. Adding a capacitor, typically 1000-2000pf, in parallel with Coss can often eliminate the EMI issue. If double pulsing is caused due to excessive ringing, placing 4.7-10 ohm resistor between the phase node and the DRN pin of the SC1405 is recommended to cure the problem.

Proper layout minimizes ringing, and so the need for external components. Use of SO-8 or other surface mount MOSFETs reduces lead inductance and their parasitic effects.

ASYNCHRONOUS OPERATION

The SC1405C can be configured to operate in asynchronous mode by pulling MODE to logic LOW, thus disabling the low-side FET drive. This can save power at light loads since the low-side FET's gate capacitance does not have to charged at the switching frequency. Another efficiency benefit to operating in asynchronous mode is preventing reverse current flow. When operating in synchronous mode, the inductor current can go negative and flow in reverse direction when the bottom FET is on and the DC load is less than 1/2 inductor ripple current. At that point, the inductor core and wire losses, depending on the magnitude of the ripple current, can be significant. Operating in asynchronous mode at light loads effectively only charges the inductor by as much as needed to supply the load current, since the inductor never completely discharges at light loads. DC regulation can be an issue depending on the type of controller used and minimum load required to maintain regulation. If there are no Schottkys used in parallel with bottom FET, the FET's body diode will conduct in asynchronous mode. The high voltage drop of this diode must be considered when determining the criteria for this mode of operation.

DSPS

DSPS is a logical duplicate of the bottom FET's gate drive, if MODE is held LOW.

OVP / OVER TEMPERATURE SHUTDOWN

Output over-voltage protection (OVP) may be implemented on the SC1405 independent of the PWM controller . A voltage divider from the output is compared with the internal bandgap voltage of 1.2V (typical). Upon exceeding this voltage, the overvoltage comparator disables the top FET, while turning on the bottom FET to discharge the output capacitors through the output inductor.

The SC1405C has a unique adaptive OVP circuit. Short noise pulses, less than ~100ns are rejected completely; longer pulses will trigger OVP if only of sufficient magnitude. A long term transient will trigger OVP with a smaller magnitude.

Provide a single switching period RC time constant and at least 250mV headroom on the OVP pin to prevent false OVP events.

The SC1405 will shutdown if its Tj exceeds 165°C.

PRELIMINARY

Performance diagrams, Application Evaluation Board. (Fig.4)

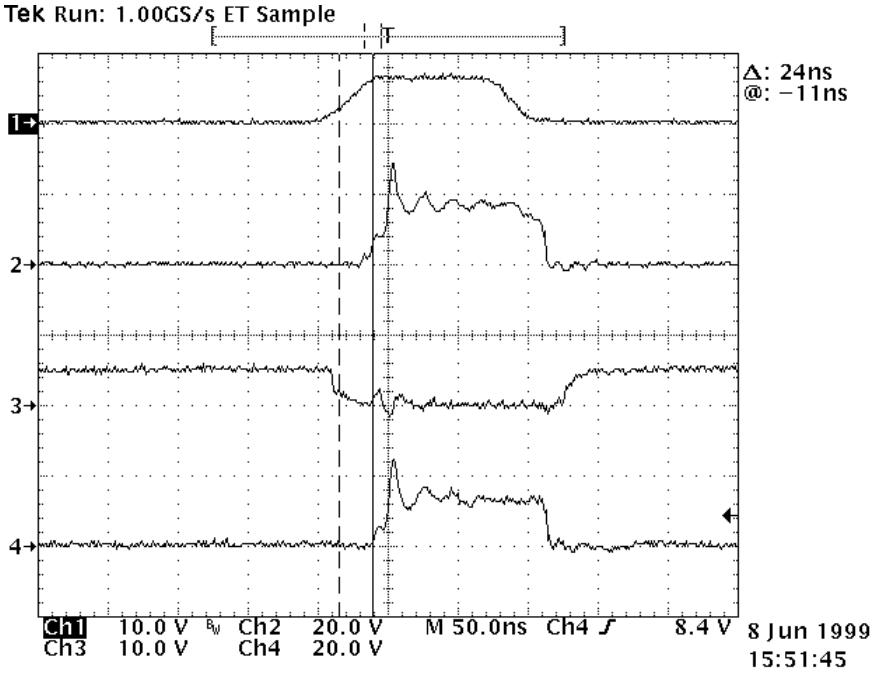


Figure 4-Timing diagram:
Ch1:CO input Ch2:TG drive Ch3:BG non-overlap drive Ch4:phase node Iout=20A (10A/phase)
Refer to Eval. Schematic (fig.3)

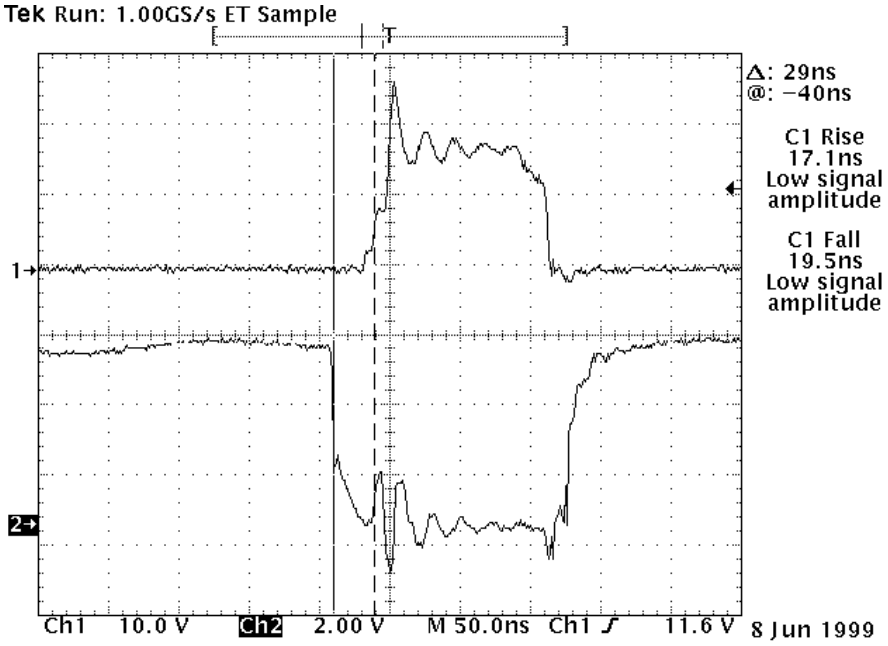


Figure 5-Timing diagram:
Rise/Fall times
Ch1:TG drive Ch2:BG drive Cursor:$Tpdh_{TG}$ Iout=20A (10A/phase) Refer to Eval. Schematic (fig. 3)

Vin = 12V,Vout = 1.6V Top FET=IR7811 FDB7030(BL) Qgd = 23nc

PRELIMINARY

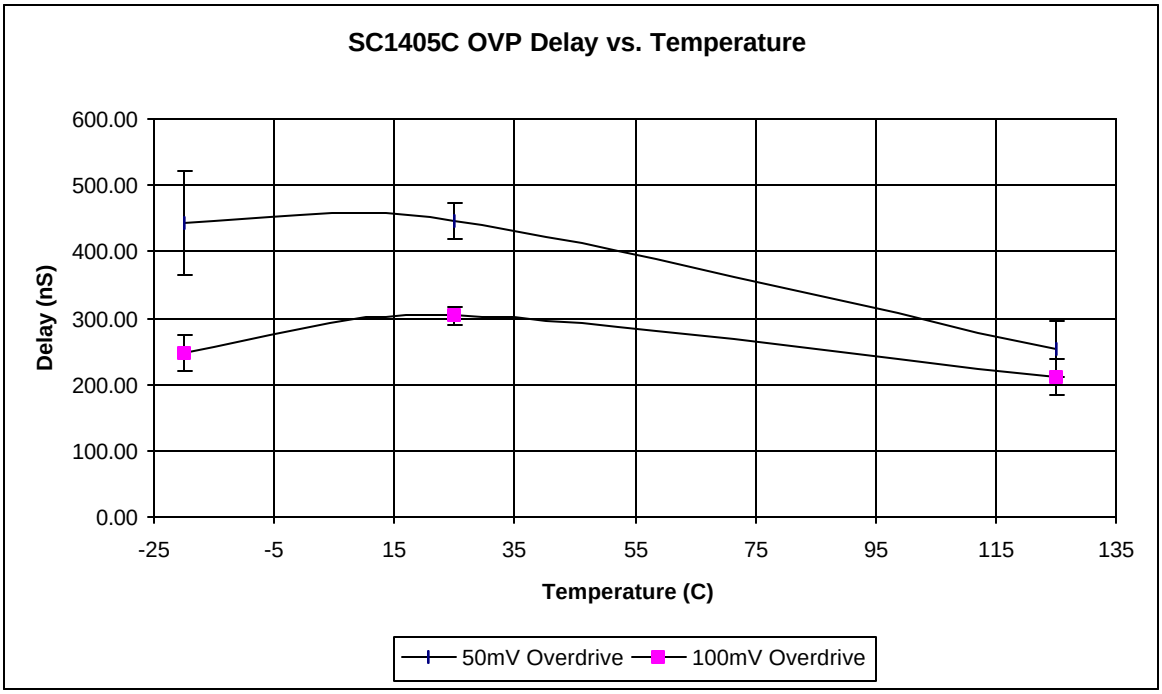


Figure 6-Delay vs. Temp

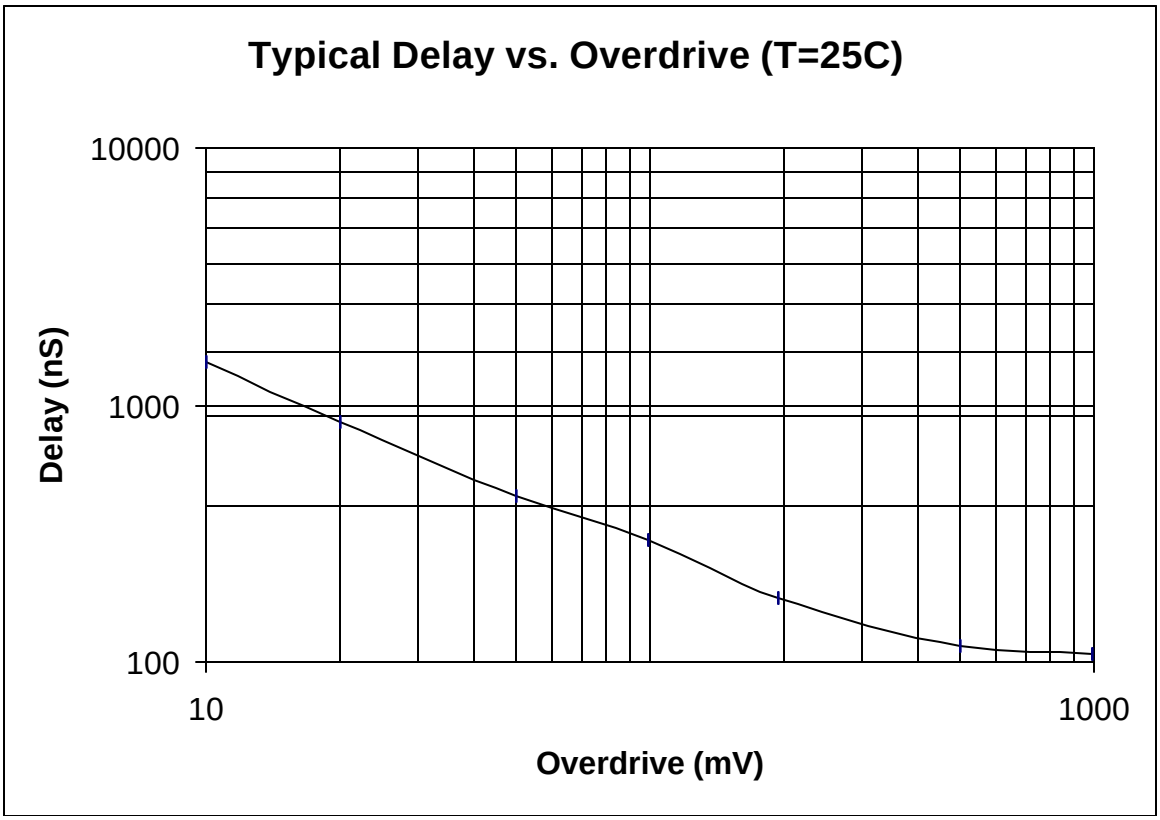
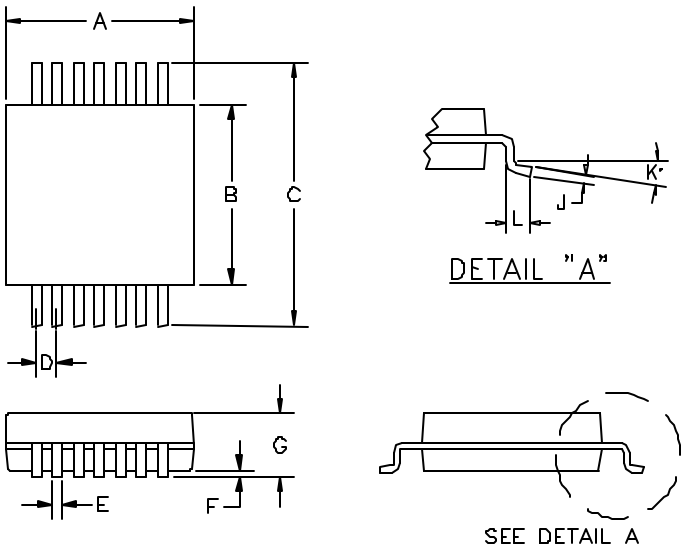


Figure 7-Delay vs. Overdrive

PRELIMINARY

OUTLINE DRAWING TSSOP-14



DIMENSIONS [1]					
DIM	INCHES		MM		NOTE
	MIN	MAX	MIN	MAX	
A	.193	.201	4.90	5.10	[2]
B	.169	.177	4.30	4.50	[2]
C	.252 BSC		6.40 BSC		—
D	.026 BSC		.65 BSC		—
E	.007	.012	.19	.30	—
F	.002	.006	.05	.15	—
G		.047		1.20	—
J	.004	.008	.09	.20	—
K	0°	8°	0°	8°	—
L	.018	.030	.45	.75	—

JEDEC MO-153AB1

[2] DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSIONS
[1] CONTROLLING DIMENSIONS: MILLIMETERS

ECN00-924