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Memory Products	

# 82S185A

## 8K-bit TTL bipolar PROM

### DESCRIPTION

The 82S185A is field programmable, which means that custom patterns are immediately available by following the Signetics Generic I fusing procedure. The devices are supplied with all outputs at logical Low. Outputs are programmed to a logic High level at any specified address by fusing the Ni-Cr link matrix.

This device includes on-chip decoding and one Chip Enable input for memory expansion. It features 3-State outputs for optimization of word expansion in bused organizations.

Ordering information can be found on the following page.

The 82S185A device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Signetics Military Data Handbook.

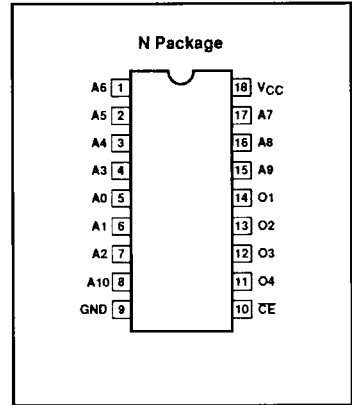
### FEATURES

- Low power dissipation: 70μW/bit typ
- Address access time: 50ns max
- Input loading: -100μA max
- On-chip address decoding
- No separate fusing pins
- Unprogrammed outputs are Low level
- Fully TTL compatible
- One Chip Enable input
- Outputs: 3-State

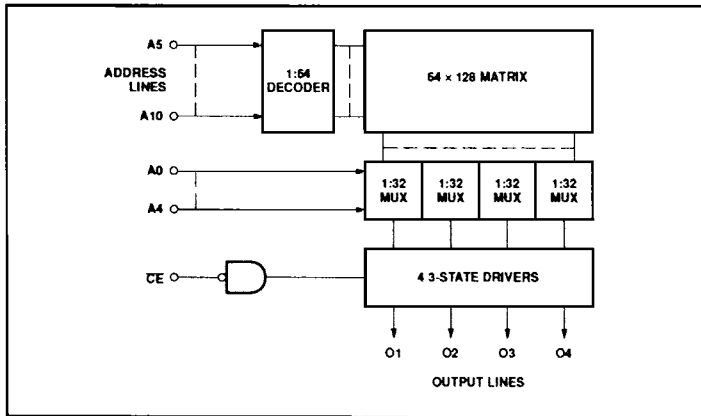
### APPLICATIONS

- Microprogramming
- Control store
- Random logic
- Code conversion

### PIN CONFIGURATION



### BLOCK DIAGRAM



## 8K-bit TTL bipolar PROM (2048 × 4)

82S185A

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE
18-Pin Plastic Dual-In-Line 300mil-wide	N82S185A N

## ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	+7.0	$V_{DC}$
$V_{IN}$	Input voltage	+5.5	$V_{DC}$
$V_O$	Output voltage Off-State	+5.5	$V_{DC}$
$T_{amb}$	Operating temperature range	0 to +75	°C
$T_{stg}$	Storage temperature range	-65 to +150	°C

## DC ELECTRICAL CHARACTERISTICS

0°C ≤  $T_{amb}$  ≤ +75°C, 4.75V ≤  $V_{CC}$  ≤ 5.25V

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1,2</sup>	LIMITS			UNIT
			Min	Typ <sup>3</sup>	Max	
<b>Input voltage</b>						
$V_{IL}$	Low	$V_{CC} = 4.75V$	2.0		0.8	V
$V_{IH}$	High	$V_{CC} = 5.25V$			V	
$V_{IC}$	Clamp	$I_{IN} = -12mA$			-1.2	V
<b>Output voltage</b>						
$V_{OL}$	Low	$\overline{CE} = \text{Low}$ $I_{OUT} = 16mA$	2.4		0.45	V
$V_{OH}$	High	$I_{OUT} = -2mA$				V
<b>Input current</b>						
$I_{IL}$	Low	$V_{IN} = 0.45V$			-100	μA
$I_{IH}$	High	$V_{IN} = 5.5V$				40
<b>Output current</b>						
$I_{OZ}$	Hi-Z state	$\overline{CE} = \text{High}, V_{OUT} = 0.5V$	-15		-40	μA
$I_{OS}$	Short circuit <sup>4</sup>	$\overline{CE} = \text{High}, V_{OUT} = 5.5V$			40	μA
		$\overline{CE} = \text{Low}, V_{OUT} = 0V, \text{High stored}$			-70	mA
<b>Supply current<sup>5</sup></b>						
$I_{CC}$		$V_{CC} = 5.25V$		110	155	mA
<b>Capacitance</b>						
$C_{IN}$	Input	$\overline{CE} = \text{High}, V_{CC} = 5.0V$ $V_{IN} = 2.0V$			5	pF
$C_{OUT}$	Output	$V_{OUT} = 2.0V$			8	pF

## NOTES:

- Positive current is defined as into the terminal referenced.
- All voltages with respect to network ground.
- All typical values are at  $V_{CC} = 5V, T_{amb} = +25°C$ .
- Duration of short circuit should not exceed 1 second.
- Measured with all inputs grounded and all outputs open.

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## AC ELECTRICAL CHARACTERISTICS

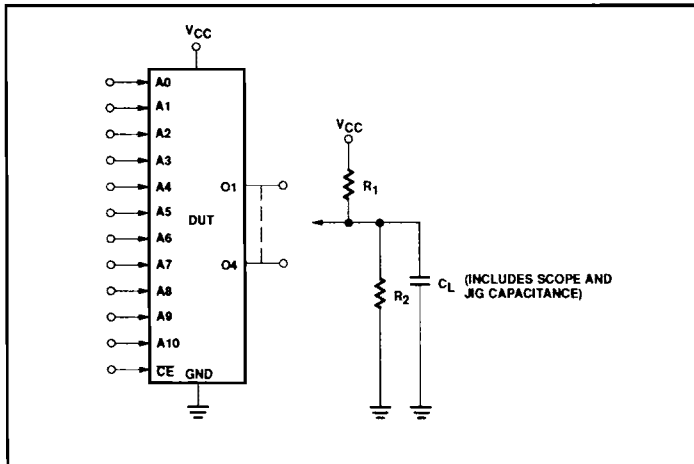
$R_1 = 270\Omega$ ,  $R_2 = 600\Omega$ ,  $C_L = 30\text{pF}$ ,  $0^\circ\text{C} \leq T_{\text{amb}} \leq +75^\circ\text{C}$ ,  $4.75\text{V} \leq V_{\text{CC}} \leq 5.25\text{V}$

SYMBOL	PARAMETER	TO	FROM	LIMITS			UNIT
				Min	Typ <sup>1</sup>	Max	
<b>Access time<sup>2</sup></b>							
$t_{AA}$		Output	Address		40	50	ns
$t_{CE}$		Output	Chip Enable		20	30	ns
<b>Disable time<sup>3</sup></b>							
$t_{CD}$		Output	Chip Disable		20	30	ns

**NOTES:**

1. Typical values are at  $V_{\text{CC}} = 5\text{V}$ ,  $T_{\text{amb}} = +25^\circ\text{C}$ .
2. Tested at an address cycle time of  $1\mu\text{s}$ .
3. Measured at a delta of 0.5V from Logic Level with  $R_1 = 750\Omega$ ,  $R_2 = 750\Omega$ ,  $C_L = 5\text{pF}$ .

## TEST LOAD CIRCUIT



## VOLTAGE WAVEFORMS

