

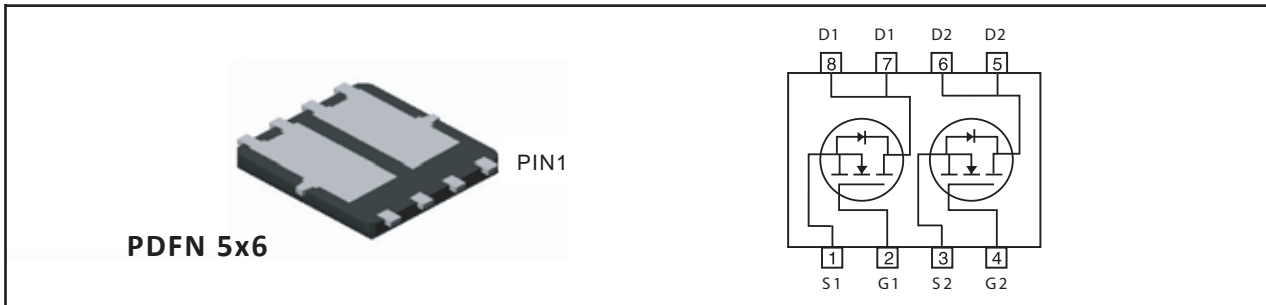


## Dual N-Channel Enhancement Mode Field Effect Transistor

PRODUCT SUMMARY		
V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Max
30V	7.5A	22 @ V <sub>GS</sub> =10V
		32 @ V <sub>GS</sub> =4.5V

### FEATURES

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- Surface Mount Package.



### ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	30	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous	T <sub>A</sub> =25°C	7.5 <sup>a</sup>
		T <sub>A</sub> =70°C	6 <sup>a</sup>
		T <sub>C</sub> =25°C	21.5 <sup>e</sup>
		T <sub>C</sub> =100°C	13.6 <sup>e</sup>
I <sub>DM</sub>	-Pulsed <sup>b</sup>	31	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>	49	mJ
P <sub>D</sub>	Maximum Power Dissipation	T <sub>A</sub> =25°C	2.5 <sup>a</sup>
		T <sub>A</sub> =70°C	1.6 <sup>a</sup>
		T <sub>C</sub> =25°C	20.8
		T <sub>C</sub> =100°C	8.3
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 150	°C

### THERMAL CHARACTERISTICS

R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	6	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient <sup>a</sup>	50	°C/W

# SP3903

Ver 1.4

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	30			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =24V , V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V , V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	1.4	1.7	2.3	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V , I <sub>D</sub> =3.75A		16	22	m ohm
		V <sub>GS</sub> =4.5V , I <sub>D</sub> =3.1A		23	32	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =5V , I <sub>D</sub> =3.75A		13		S
<b>DYNAMIC CHARACTERISTICS <sup>c</sup></b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =15V, V <sub>GS</sub> =0V f=1.0MHz		360		pF
C <sub>OSS</sub>	Output Capacitance			90		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			70		pF
<b>SWITCHING CHARACTERISTICS <sup>c</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =15V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>GEN</sub> =6 ohm		10		ns
t <sub>r</sub>	Rise Time			12.6		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			17		ns
t <sub>f</sub>	Fall Time			8.3		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =15V, I <sub>D</sub> =3.75A, V <sub>GS</sub> =10V		7		nC
		V <sub>DS</sub> =15V, I <sub>D</sub> =3.75A, V <sub>GS</sub> =4.5V		4		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =15V, I <sub>D</sub> =3.75A, V <sub>GS</sub> =4.5V		1		nC
Q <sub>gd</sub>	Gate-Drain Charge			2.3		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =2A		0.8	1.2	V

### Notes

- Surface Mounted on FR4 Board, t < 10sec.
- Pulse Test: Pulse Width < 300us, Duty Cycle < 2%.
- Guaranteed by design, not subject to production testing.
- Starting T<sub>J</sub>=25°C, L=0.5mH, V<sub>DD</sub> = 20V. (See Figure13)
- Drain current limited by maximum junction temperature.

Jul, 18, 2013

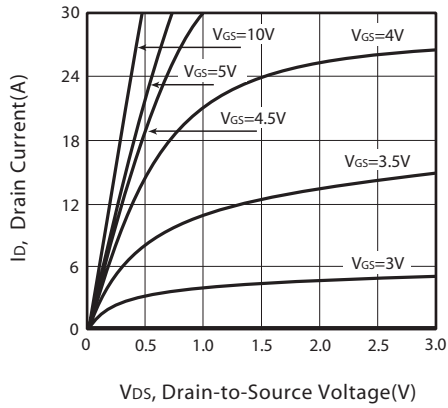


Figure 1. Output Characteristics

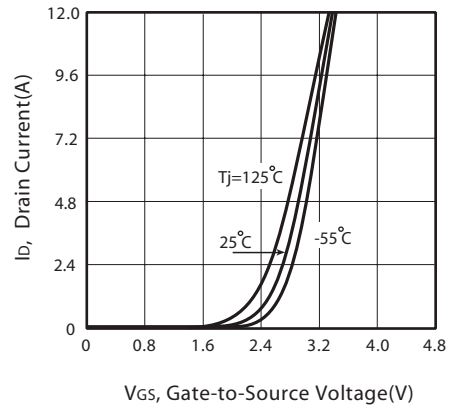


Figure 2. Transfer Characteristics

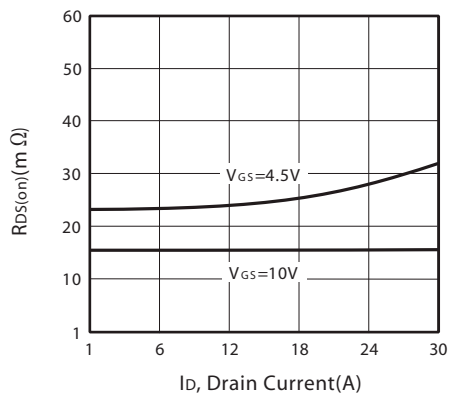


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

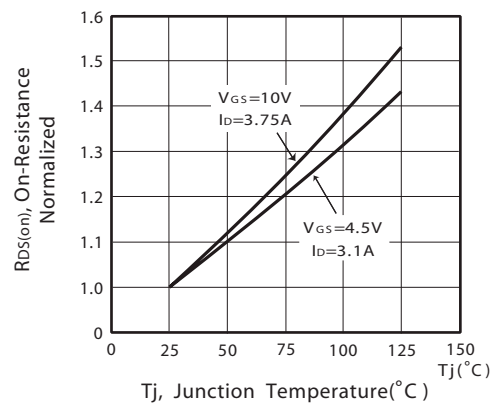


Figure 4. On-Resistance Variation with Drain Current and Temperature

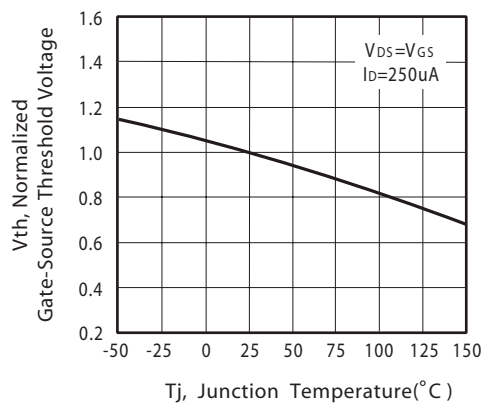


Figure 5. Gate Threshold Variation with Temperature

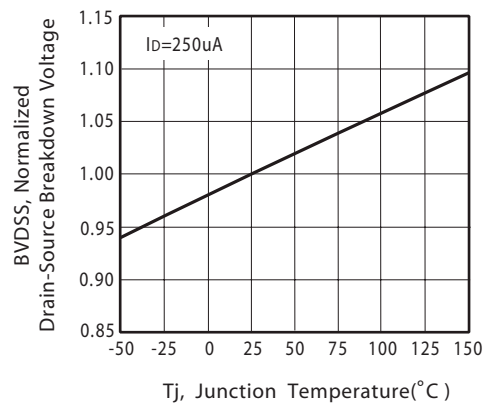


Figure 6. Breakdown Voltage Variation with Temperature

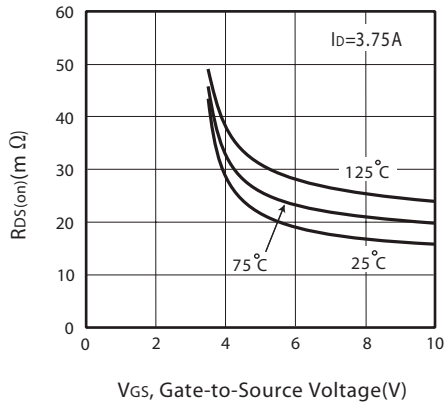


Figure 7. On-Resistance vs. Gate-Source Voltage

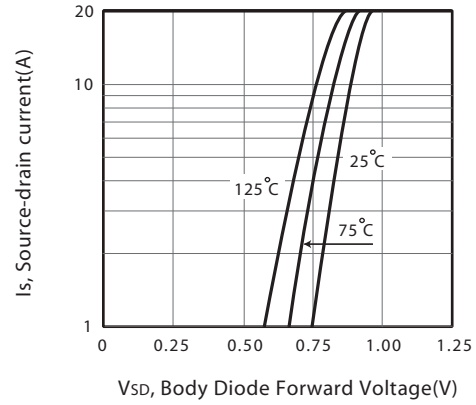


Figure 8. Body Diode Forward Voltage Variation with Source Current

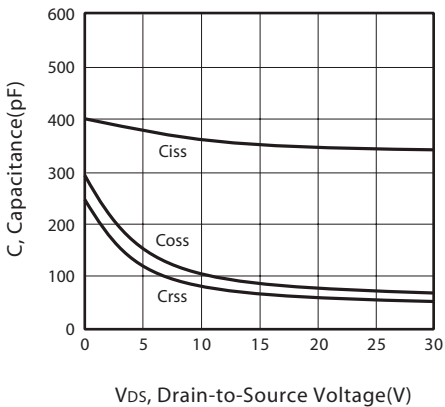


Figure 9. Capacitance

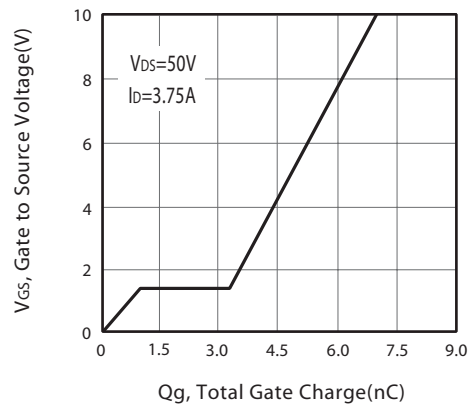


Figure 10. Gate Charge

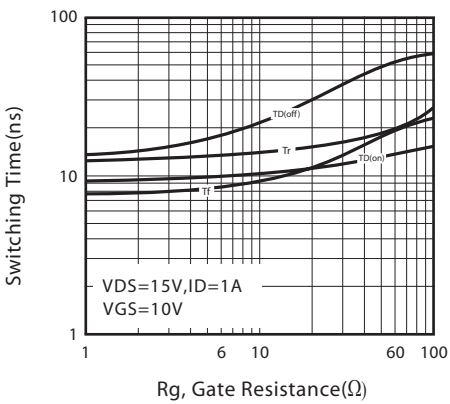


Figure 11. switching characteristics

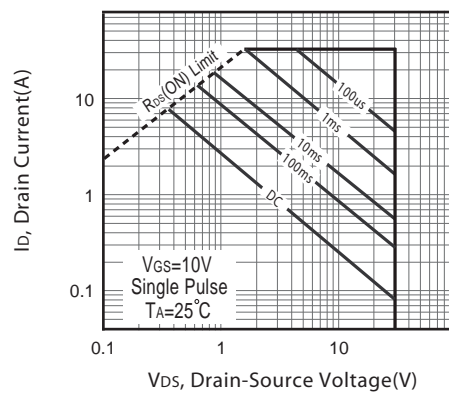
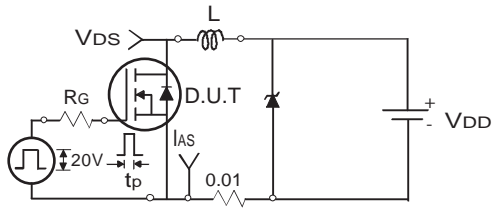
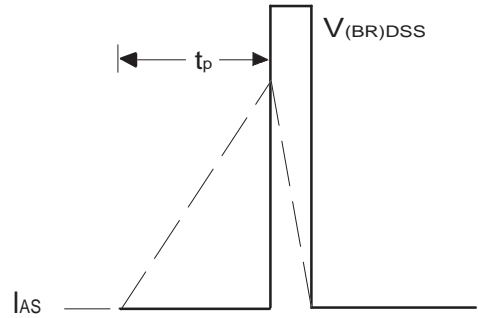


Figure 12. Maximum Safe Operating Area



Uncamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

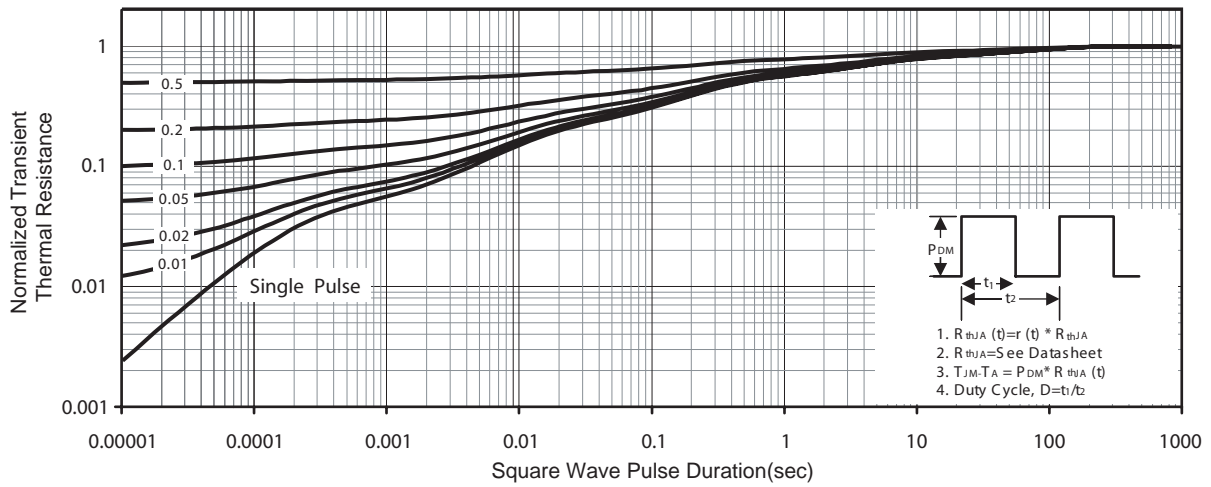
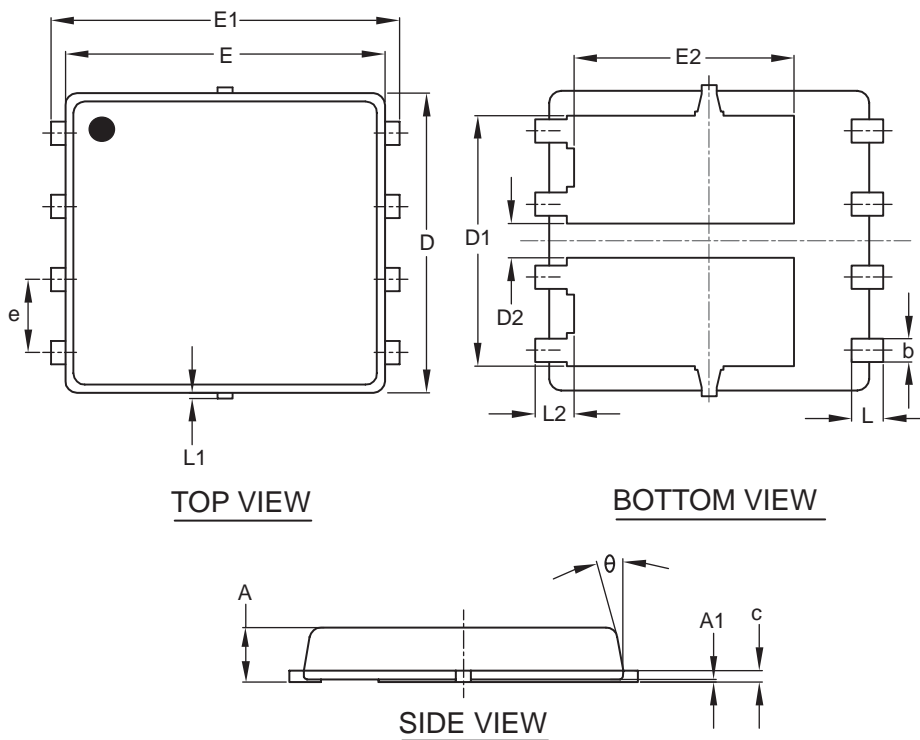


Figure 14. Normalized Thermal Transient Impedance Curve

## PACKAGE OUTLINE DIMENSIONS

### PDFN 5x6-8L



SYMBOLS	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	—	0.05
b	0.30	0.40	0.50
c	0.15	0.20	0.25
D	5.20 BSC		
D1	4.35 BSC		
D2	0.50	0.60	0.75
E	5.55 BSC		
E1	6.05 BSC		
E2	3.82 BSC		
e	1.27 BSC		
L	0.45	0.55	0.65
L1	0.00	—	0.15
L2	0.68 REF		
$\theta$	0°	—	10°

## TOP MARKING DEFINITION

