1 Megabit x 4 Dynamic RAM
5V, Fast Page

The EDI441024C is a high performance, low power CMOS Dynamic RAM organized as 1 Megabit x 4.

During READ and WRITE cycles each bit is addressed through 20 address bits which are entered 10 at a time (AØ-A9). RAS\ is used to latch the first 10 bits and CAS\, the second 10 bits. A READ or WRITE cycle is selected with the W\ input. A logic HIGH on W\ dictates READ mode, while a logic LOW on W\ dictates WRITE mode.

During a WRITE cycle Data-in is latched by the falling edge of W\ or CAS\, whichever occurs last. If W\ goes low prior to CAS\ going LOW, the output pins remain open (HIGH-Z) until the next CAS\ cycle, regardleses of the status of G\. If W\ goes LOW after data reaches the output pins, Data-out pins are activated and retain the selected cell data as long as CAS\ and G\ remain LOW, until W\ goes Low. This late W\ pulse results in a DELAYED WRITE or READ-WRITE cycle.

The four data inputs and four data outputs are routed through four pins using common I/O and pin direction is controlled by W\ and G\. FAST PAGE MODE operations allow faster data operations, READ, WRITE or READ-MODIFY-WRITE, within a row address.

All inputs and outputs are TTL compatible and operate from a single 5 volt supply.

* Note: W\ LOW prior to CAS\ LOW, EW detection circuit output is a HIGH (EARLY WRITE). CAS\ LOW prior to W\ LOW, EW detection circuit output is a LOW (LATE WRITE).

Features

1 Meg x 4 bit CMOS Dynamic
Random Access Memory

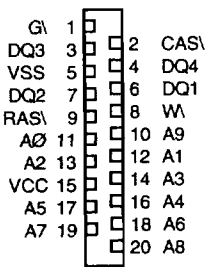
- Access Times: 70, 80 and 100ns
- 16ms Refresh Rate
- Low Operating Power Dissipation
- Low Standby Power
- Common I/O
- All Inputs/Outputs TTL Compatible

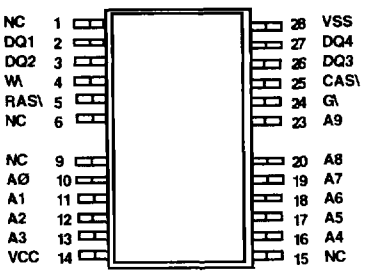
Package Style

- 20 pin Ceramic ZIP, No.18
- 24/28 Thinpack ™ Flatpack, No.317
- 24/28 pin Flatpack, No. 347

Single +5V (±10%) Supply Operation

Pin Configurations



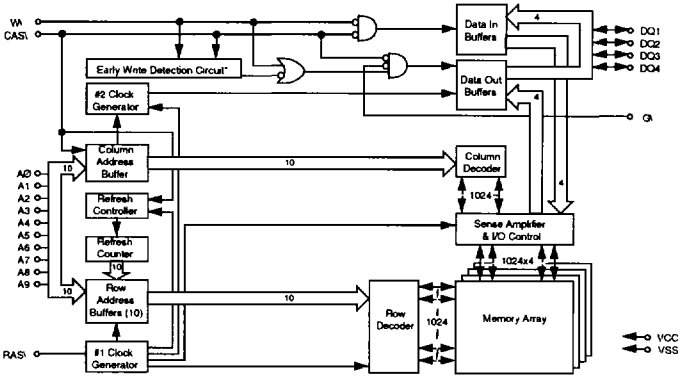


Pin Names

AØ-A9	Address Inputs
CAS\	Column Address Strobe
RAS\	Row Address Strobe
W\	Write Control Input
G\	Output Enable
DQ1-DQ4	Data Inputs/Outputs
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

3

Block Diagram



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-1.0V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0 to+70°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature (Ceramic)	-65°C to +150°C
Power Dissipation	1 Watt
Output Current	50 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

(Note 1)

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.4	--	5.5	V
Input Low Voltage	VIL	-1.0	--	0.8	V

Notes: 1. All voltage values are with respect to VSS.

Electrical Characteristics

(VCC = 5.0V ±10%) Note 2.

Parameter	Sym	Conditions	Min	Typ	Max	Units
Average Supply Current from VCC	ICC1	RAS\, CAS\ Cycling			100	mA
Operating (Notes 3, 4)		TRC = TWC = Min, Output Open				
Supply Current from VCC	ICC2	RAS\ = CAS\ = VIH, Outputs Open			3	mA
Standby		RAS\ = CAS\ ≥ VCC-0.2, Outputs Open			2	mA
Average Supply Current from VCC	ICC3	RAS\ Cycling, CAS\ = VIH			100	mA
Refreshing (Note 3)		TRC = Min, Outputs Open				
Average Supply Current from VCC	ICC4	RAS\ = VIL, CAS\ = Cycling			70	mA
Fast Page Mode (Notes 3, 4)		TPC = Min, Outputs Open				
Average Supply Current from VCC	ICC6	CAS\ before RAS\ Refresh Cycling			100	mA
CAS\ before RAS\ Refresh Mode (Note 3)		TRC = Min Outputs Open				
Input Current	II	0V ≤ VIN ≤ 5.5V	-2		2	µA
		All Other Input Pins = 0V				
Off-State Output Current	IOZ	Outputs Floating 0V≤ V OUT ≤ 5.5V	-10		10	µA
Output High Voltage	VOH	IOH = -5mA	2.4	—	VCC	V
Output Low Voltage	VOL	IOL= 4.2mA	0	—	0.4	V

Notes: 2. Current flowing into an IC is positive, out is negative.
3. ICC1(av), ICC3(av), ICC4(av), and ICC6 are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4. ICC1(av), and ICC4(av) are dependent on output loading. Specified values are obtained with the output open.

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Test Conditions	Min	Typ	Max	Unit
Address Input Capacitance	CA	VI = VSS			6	pF
Input Capacitance (D)	CD	f = 1MHz			6	pF
Input Capacitance (CAS\,W\, RAS\)	CC, CW, CR	Vi = 25mVrms			7	pF
Output Capacitance (Q)	CQ	VO = VSS, f = 1MHz, Vi = 25mVrms			8	pF

Input Conditions for Each Mode

The EDI441024C provides, in addition to normal Read, Write, and Read-modify-Write operations, a number of other functions, e.g. Fast Page Mode, RAS\-only Refresh, and Delayed Write. The input conditions for each are shown below.

ACT = Active
NAC= Non-active
DNC= Don't care
VLD = Valid
APD = Applied
OPN = Open

Operation	Inputs RAS\	CAS\	W\	G\	Row Address	Column Address	Input/Output D	Q
Read*	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD
Early Write*	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN
Read-Modify-Write*	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD
RAS\ -only Refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN
Hidden Refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD
CAS\ before RAS\ Refresh	ACT	ACT	ACT	DNC	DNC	DNC	DNC	OPN
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN

*Fast Page Mode Identical

Switching Characteristics

(VCC = 5.0V±10) NOTE 5.

Parameter	Sym	70ns Min	70ns Max	80ns Min	80ns Max	100ns Min	100ns Max	Units	Notes
Access Time from CAS\	TCAC		20		20		25	ns	6,7
Access Time from RAS\	TRAC		70		80		100	ns	6
Column Address Access Time	TCAA		35		40		50	ns	6,9
Access Time from CAS\ Precharge	TCPA		40		45		50	ns	6
Access Time from G\	TOEA		20		20		25	ns	6
Output Low Impedance Time from CAS\ low	TCLZ	0		0		0		ns	
Output Disable Time after CAS\ High	TOFF	3	20	3	20	3	20	ns	11
Output Disable Time after G\ High	TDISOE	0	20	0	20	0	20	ns	11

Notes: 5. An initial pause of 100µs is required after power-up, followed by any RAS\ only refresh or CAS\ before RAS\ refresh cycles with W\ HIGH before proper device operation is achieved. Note that RAS\ may be cycled during the initial pause. Any RAS\ only refresh or CAS\ before RAS\ refresh cycles with W\ HIGH are required after prolonged periods of RAS\ inactivity before proper device operation.

6 Measured with a load circuit equivalent to 2TTL loads and 100pF.

7. Assume that TRCD(max) ≤ TRAD and TRAD(max) ≥ TRAD.

8. Assume that TRCD ≤ TRCD(max) and TRAD ≤ TRAD(max).

9. Assume that TRCD - TRAD ≤ TCAA(max) and TRCD ≥ TRCD(max).

10. Assume that TCP ≤ TCP(max) and TASC ≥ TASC(max).

11. TOFF(max) defines the time at which the output achieves the high impedance state (IOUT ≤ I±10µAI) and is not reference to VOH(min) or VOL(max).

Timing Requirements
Read, Write, Read-Modify-Write, Refresh, and Fast Page Mode Cycles

(VCC = 5.0V±10%) Notes 12,13

		70ns		80ns		100ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Refresh Cycle	TREF		16		16		16	ms	
RAS\ Precharge Time	TRP	50		60		80		ns	
RAS\ to CAS\ Delay Time	TRCD	20	50	20	60	25	75	ns	14
Delay CAS\ High to RAS\ Low	TCRP	10		10		10		ns	15
CAS\ Precharge Time (Non Page Mode)	TCPN	10		10		10		ns	16
Column Address Delay from RAS\ Low	TRAD	15	35	15	40	20	50	ns	17
Row Address Set Up Time	TASR	0		0		0		ns	
Column Address Set Up Time	TASC	0		0		0		ns	18
Row Address Hold Time	TRAH	10		10		15		ns	
Column Address Hold Time	TCAH	15		15		20		ns	
Transition Time	TT	3	50	3	50	3	50	ns	19

Notes: 12. The timing requirements are assumed TT = 5ns.
13. VIH(min) and VIL (max) are reference levels for measuring timing of input signals.
14. TRCD(max) is specified as a reference point only. If TRCD is less than TRCD(max), access time is TRAC. If TRCD is greater than TRCD(max), access time is defined as TCAC and TCAA as shown in notes 7, 9.
15. TCRP requirement is applicable for all RAS\-CAS\ cycles.
16. TCPN(min) is specified as TCPN(min) =TRCD(min) +TCRP(min) except for TCP of fast page mode cycle.
17. TRAD(max) is specified as a reference point only. If TRAD ≥ TRAD(max), access time is assumed byTCAA for read cycle.
18. TASC(max) is specified as a reference point only of address acess time.
19. TT is measured between VIH(min) and VIL(max).

Read and Refresh Cycles

(VCC = 5.0V±10%) Notes 5, 12,13

		70ns		80ns		100ns			
Parameter	Sym	Min	Max	Min	Max	Min	Max	Unit	Notes
Read Cycle Time	TRC	130		150		190		ns	
RAS\ Low Pulse Width	TRAS	70	100,000	80	100,000	100	100,000	ns	
CAS\ Low Pulse Width	TCAS	20	100,000	20	100,000	25	100,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	70		80		100		ns	
RAS\ Hold Time after CAS\ Low	TRSH	20		20		25		ns	
Read Set Up Time before CAS\ Low	TRCS	0		0		0		ns	
Read Hold Time after CAS\ High	TRCH	0		0		0		ns	20
Read Hold Time after RAS\ High	TRRH	0		0		0		ns	20
Column Address to RAS\ Setup	TRAL	35		40		50		ns	
Precharge to CAS\ Active	TRPC	0		0		0		ns	
Delay Time, Data to G\ Low	TDOEL	0		0		0		ns	
Delay Time, G\ High to Data	TOEHD	20		20		25		ns	
CAS\ Hold Time after G\ Low	THOECH	20		20		25		ns	
RAS\ Hold Time after G\ Low	THOERH	20		20		25		ns	

Notes:20 Either TRCH or TRRH must be satisfied for a read cycle.

4 Megabit DRAM Refresh and Power Up Restrictions

Users of 4 meg DRAMS should be aware of the JEDEC defined test function implementation and its implications. The test function is enabled by entering a CAS\ before RAS\ refresh cycle with W\ held low. The test function will remain enabled for all subsequent memory cycles until a CAS\ before RAS\ refresh with W\ high disables the function. With the test function enabled it is not possible to read any data as the device output is tied to a comparator output, not the data out path. Writes performed with the test function enabled will write data to multiple locations simultaneously. There is no status flag to determine if the test function is active so it is the user's responsibility to insure the device is in the desired operating state.

Since the test function can be enabled during a CAS\ before RAS\ refresh with the W\ low, care must be taken that W\ is high for time TWRP before and is held high for time TWRH after each low going RAS\ transition for normal operation when CAS\ before RAS\ refresh is used.

To prevent the possibility of power up initiating the test function, the 4 meg Dram wake up cycles are now limited to a 100µs pause followed by at least eight CAS\ before RAS\ refresh cycles with W\ high or at least eight RAS\ only refresh cycles. No other RAS\ cycles are allowed for device wake up.

Restriction Summary

1. W\ must be high before initiating a CAS\ before RAS\ refresh to prevent the test function from becoming active.
2. Wake up cycles are limited to a 100µs pause after power up, followed by at least eight RAS\ only or eight CAS\ before RAS\ cycles with W\ high.

Write Cycle, Early and Delayed Write

(VCC = 5.0V±10%) Notes 5, 12, 13

		70ns		80ns		100ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Write Cycle Time	TWC	130		150		190		ns	
RAS\ Low Pulse Width	TRAS	70	100,000	80	100,000	100	100,000	ns	
CAS\ Low Pulse Width	TCAS	20	100,000	20	100,000	25	100,000	ns	
CAS\ Hold Time after RAS\ Low	TCSH	70		80		100		ns	
RAS\ Hold Time after CAS\ Low	TRSH	20		20		25		ns	
Write Setup Time before CAS\ Low	TWCS	0		0		0		ns	22
Write Hold Time after CAS\ Low	TWCH	15		15		20		ns	
CAS\ Hold Time after Write Low	TCWL	20		20		25		ns	
RAS\ Hold Time after Write Low	TRWL	20		20		25		ns	
Write Pulse Width	TWP	15		15		20		ns	
Data Set up Time	TDS	0		0		0		ns	22
Data Hold Time after CAS\ Low	TDH	15		15		20		ns	22
Delay Time, G\ High to Data	TOEHD	20		20		25		ns	
G\ Hold Time after Write Low	THWOE	20		20		25		ns	

Read-Write and Read-Modify-Write Cycles

(VCC = 5.0V±10%) Notes 5, 12, 13

		70ns		80ns		100ns			
Parameter	**Sym**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Read-Modify-Write CycleTime	TRWC	180		205		220		ns	21
RAS\ Low Pulse Width	TRASRW	70	100,000	80	100,000	100	100,000	ns	
CAS\ Low Pulse Width	TCASRW	20	100,000	20	100,000	25	100,000	ns	
CAS\ Hold Time after RAS\ Low	TCSHRW	70		80		100		ns	
RAS\ Hold Time after CAS\ Low	TRSHRW	20		20		25		ns	
Read Setup time before CAS\ Low	TRCS	0		0		0		ns	
CAS\ Low to W\ Low Delay	TCWD	50		50		55		ns	22
RAS\ Low to W\ Low Delay	TRWD	100		110		130		ns	22
CAS\ Hold after W\ Low	TCWL	20		20		25		ns	
RAS\ Hold after W\ Low	TRWL	20		20		25		ns	
Write Pulse Width	TWP	15		15		20		ns	
Data Set up Time	TDS	0		0		0		ns	
Data Hold Time after W\ Low	TDH	15		15		20		ns	
Address to W\ Low Delay	TAWD	65		70		80		ns	22
Delay Time, Data to G\ Low	TDOEL	0		0		0		ns	
Delay Time, G\ High to Data	TOEHD	20		20		25		ns	
G\ Hold Time after Write Low	THWOE	20		20		25		ns	

Notes: 21. TRWC is specified as TRWC(min) = TRCD(max) + TCWD (min) +TRWL(min) + TRP(min) +4TT.

22. TWCS, TRWD, TCWD, and TAWD do not define the limits of operation, but are included as electrical characteristics only.
When TWCS ≥ TWCS(min), an early write cycle is performed, and the data output keeps the high-impedance state. When TRWD≥ TRWD(min), TCWD ≥ TCWD(min) and TAWD ≥ TAWD(min), a read write cycle is performed, and the data of the selected address will be read out on the data output. If neither of the above conditions is satisfied, the condition of Q (at the access time and until CAS\ goes back to VIH) is indeterminate.

Fast Page Mode Cycle Read. Early Write, Read-Write. Read-Modify-Write Cycles

(VCC = 5.0V±10%) Notes 5, 12 13

		70ns		80ns		100ns		
Parameter	Sym	Min	Max	Min	Max	Min	Max	Unit
Fast Page Mode Cycle Time	TPC	40		45		55		ns
Fast Page Mode for R/W, R/M/W Cycle Time	TPRWC	100		105		115		ns
RAS\ Low Pulse Width for Read, Write Cycle	TRASP	70	100,000	80	100,000	100	100,000	ns
CAS\ Low Pulse Width for Read Cycle	TCAS	20	100,000	20	100,000	25	100,000	ns
CAS\ Pulse Width (Page Mode)	TCP	10		10		10		ns
RAS\ Hold Time after CAS\ Low	TRSH	20		20		25		ns

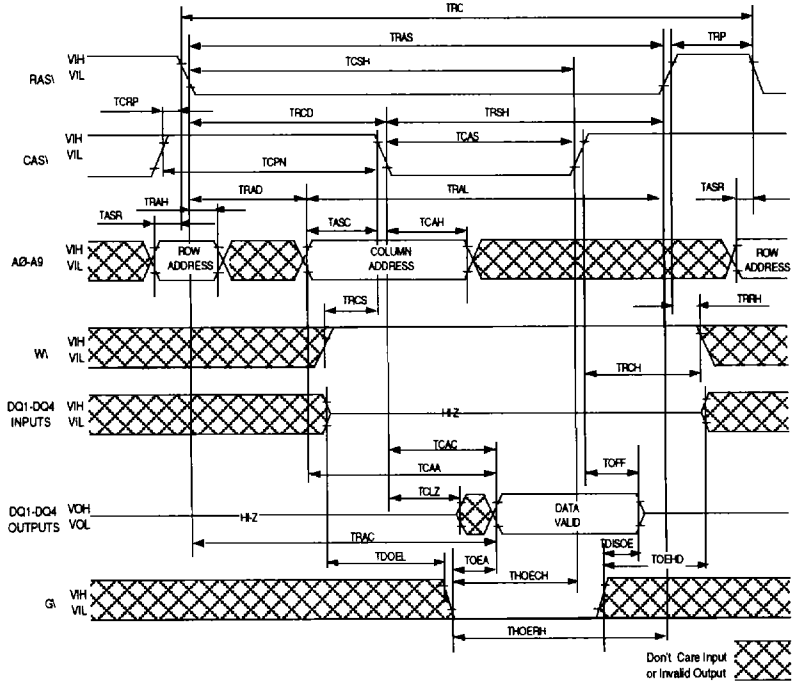
CAS\ before RAS\ Refresh Cycle

(VCC = 5.0V±10%) Notes 5, 12, 13 ,23

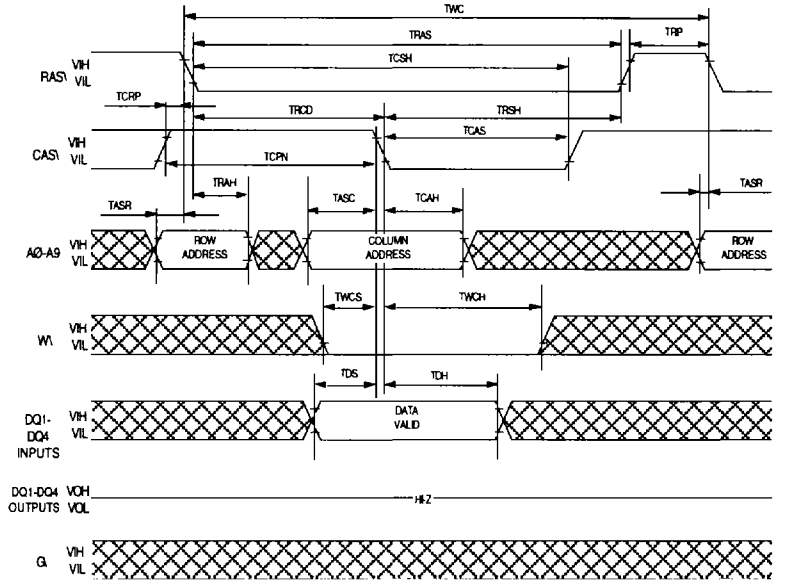
		70ns		80ns		100ns		
Parameter	Sym	Min	Max	Min	Max	Min	Max	Unit
CAS\ Setup for CAS\ before RAS\ Refresh	TCSR	10		10		10		ns
CAS\ Hold for CAS\ before RAS\ Refresh	TCHR	10		10		10		ns
Precharge to CAS\ Active	TRPC	0		0		0		ns
Write Set Up	TWRP	10		10		10		ns
Write Hold	TWRH	10		10		10		ns

Note: 23. Eight or more CAS\ before RAS\ cycles are necessary for proper operation of CAS\ before RAS\ refresh mode.

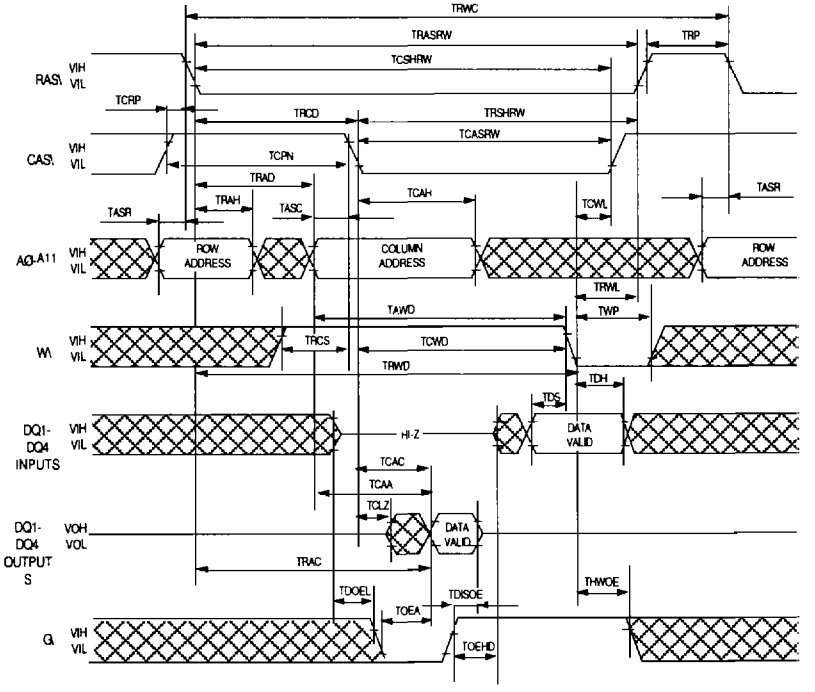
Read Cycle



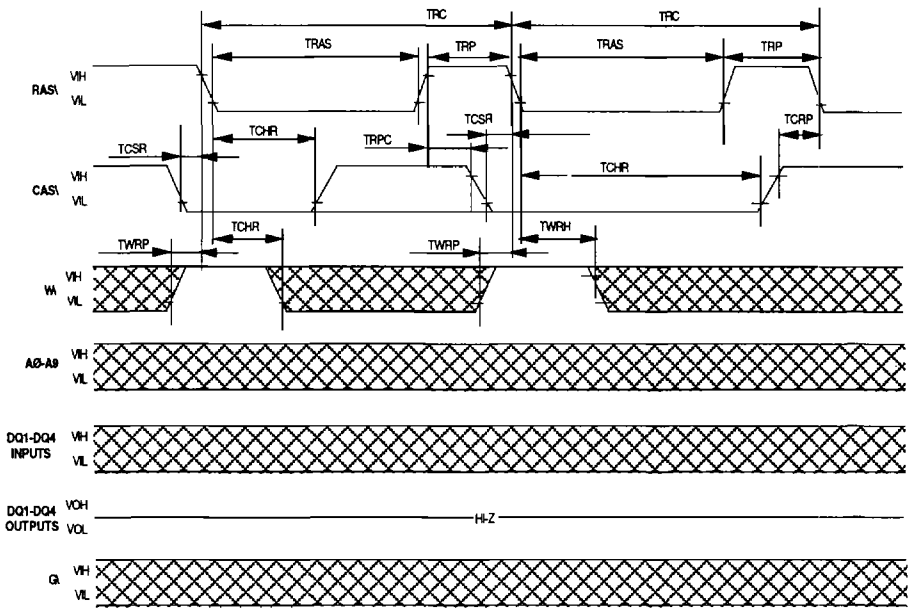
Write Cycle. Early Write



Read-Write, Read-Modify-Write and Delayed Write Cycle

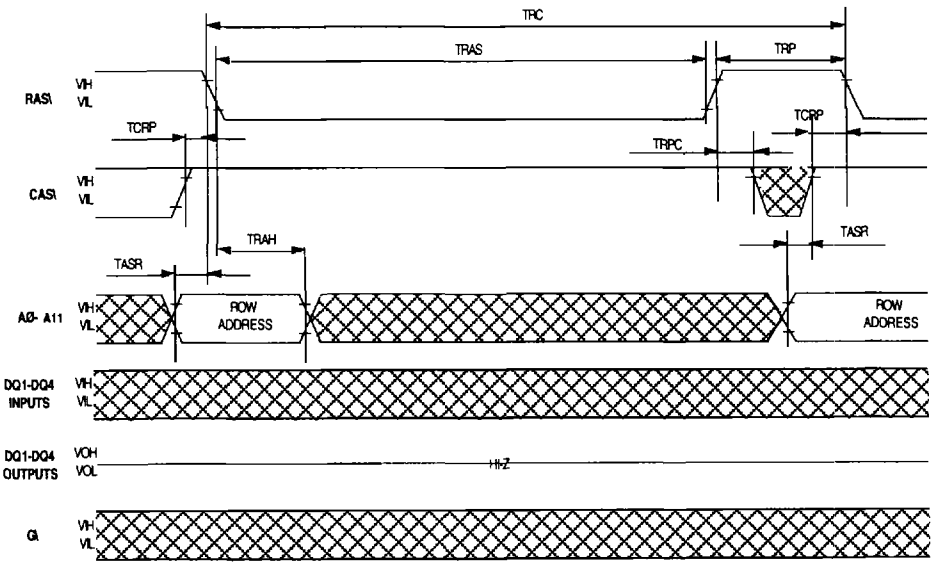


CAS\ before RAS\ Refresh



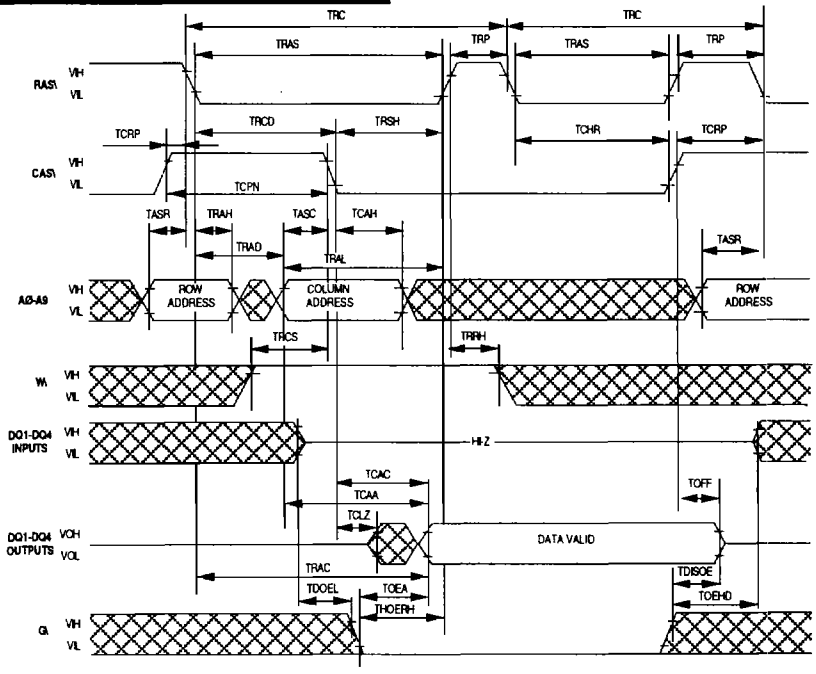
RAS\-only Refresh Cycle

Note 24

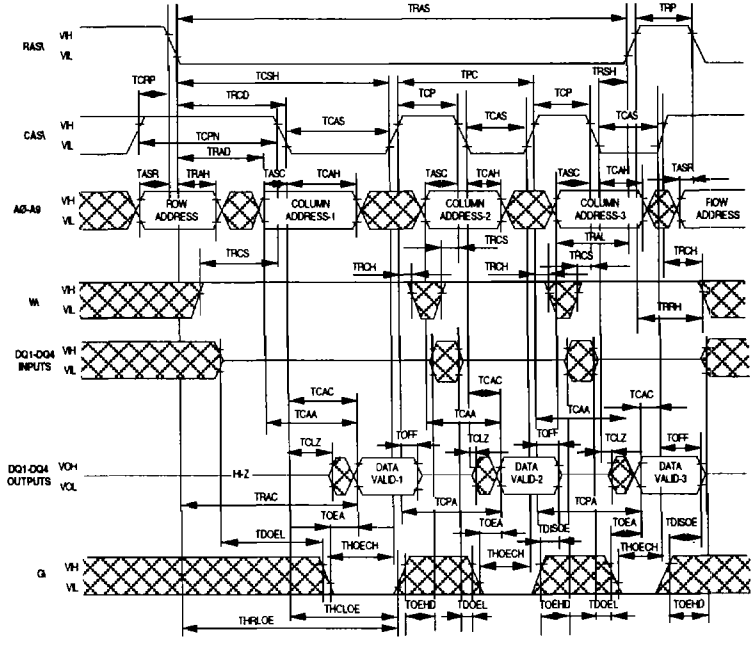


Note 24: W\ Don't Care

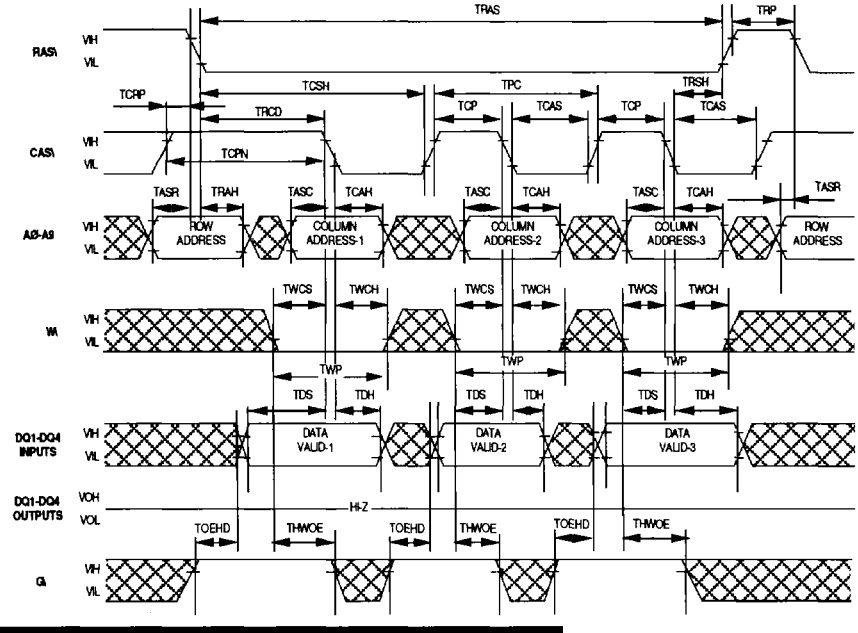
Hidden Refresh Cycle



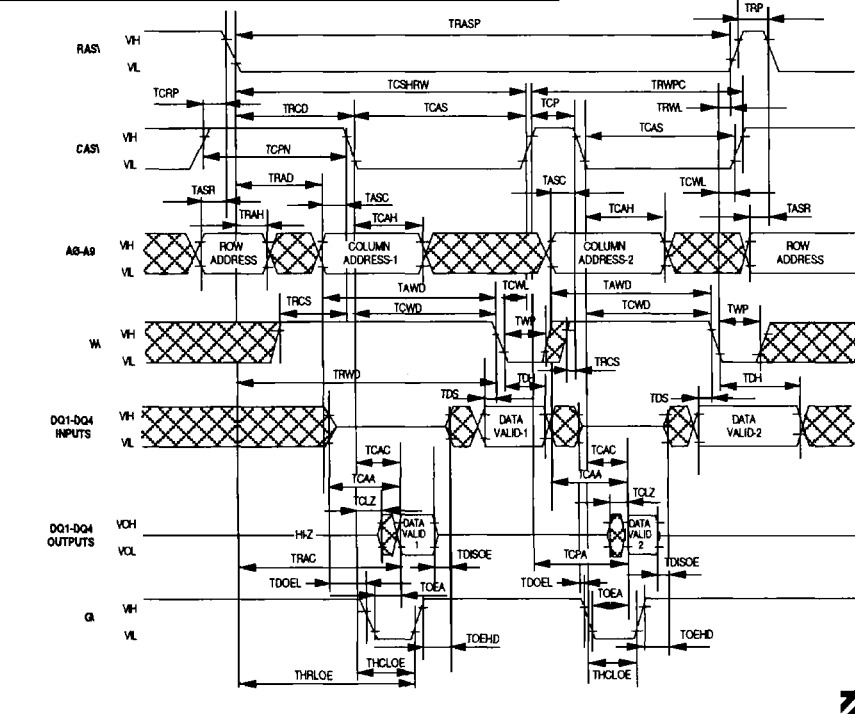
Fast-Page-Mode, Read Cycle



Fast-Page-Mode, Early Write Cycle



Fast-Page-Mode, Read-Write, Read-Modify-Write Cycle



Ordering Information

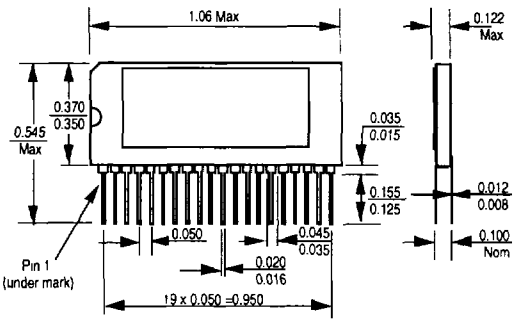
Part No.	Speed (ns)	Package No.
EDI441024C70LZB	70	18
EDI441024C80LZB	80	18
EDI441024C100LZB	100	18

Notes: For Commercial, Industrial or Mil-Temp-Only grade products use C,I or M respectively to replace B in the suffix of the part number, eg. EDI441024C70LZB becomes EDI441024C70LZI (Industrial Temp Range).

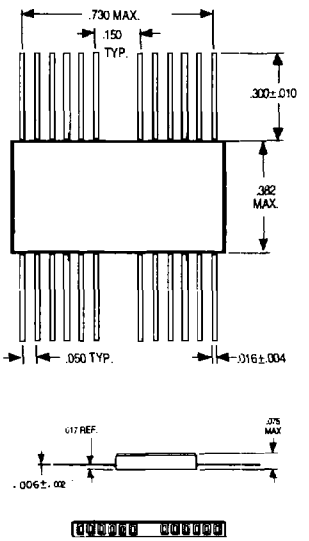
Part No.	Speed (ns)	Package No.
EDI441024C70BB	70	317
EDI441024C80BB	80	317
EDI441024C100BB	100	317
EDI441024C70FB	70	347
EDI441024C80FB	80	347
EDI441024C100FB	100	347

Package Description

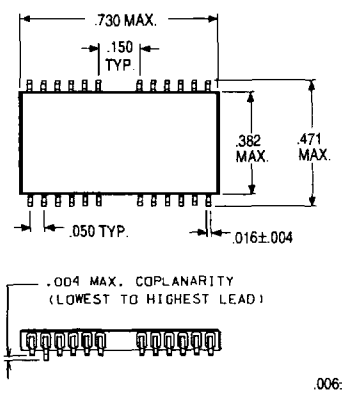
Package No. 18
20 Pin Ceramic Zip



Package No. 347
24/28 Pin Ceramic Flatpack
Weight = 1.2 gm
Theta Jc = 15°C/W
Theta Ja = 38°C/W



Package No. 317
24/28 Pin Ceramic Thinpack™ Flatpack
Weight = 1.2 gm
Theta Jc = 15°C/W
Theta Ja = 38°C/W



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