AsahiKASEI
ASAHI KASEI EMD

AKD4141-A
Evaluation board Rev.2 for AK4141

GENERAL DESCRIPTION

The AKD4141 is an evaluation board for the AK4141, digital stereo decoder with stereo sample rate converter, digital switches and sound processing functions.
The AKD4141 has the analog/digital audio interface and can achieve the interface with analog/digital audio systems via BNC/RCA/OPT-connector.

■ Ordering guide

AKD4141-A --- Evaluation board for AK4141
(Cable for connecting with printer port of IBM-AT,compatible PC and control software are packed with this. This control software does not support Windows NT.)

FUNCTION

- **DIT/DIR with optical input/output**
- **10pin Header for digital audio I/F and serial control I/F**
- **BNC connector for an external clock input**

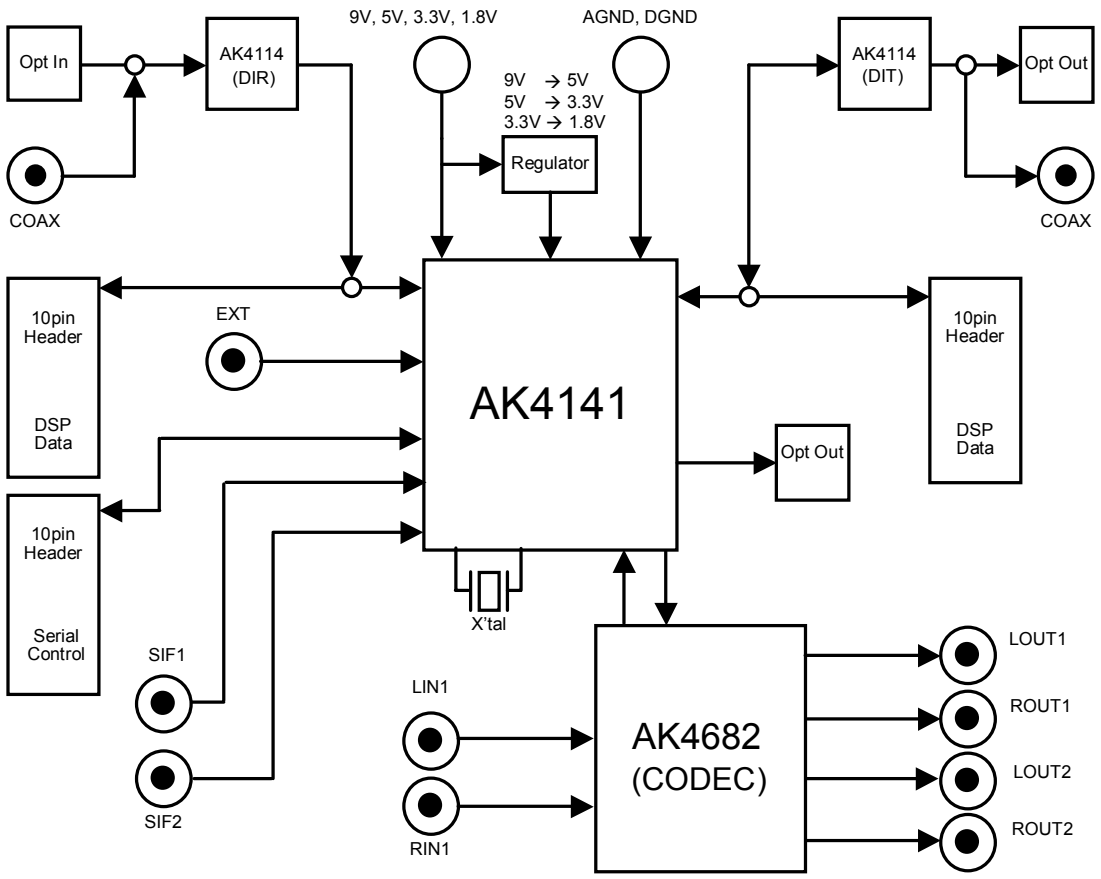


Figure 1. AKD4141 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual

Evaluation Board Manual

■ Operation sequence

1) Set up the power supply lines.

(1-1) In case of using the regulator.<Default>

[9V] (red)	=	+9V	(for regulator and PVDD of AK4682)
[TVDD] (red)	=	open	
[AVDD1] (red)	=	open	
[AVDD2] (red)	=	open	
[Logic] (red)	=	open	
[DVDD] (red)	=	open	
[AGND] (black)	=	0V	(analog ground)
[DGND] (black)	=	0V	(digital ground)

(Note) TVDD, AVDD1, AVDD2 of AK4141 and Logic is supplied "3.3V" from regulator (T2).
DVDD of AK4141 is supplied "1.8V" from regulator (T3).
AVDD1, AVDD2, DVDD1 and DVDD2 of AK4682 is supplied "5V" from regulator (T1).

(1-2) In case of using the power supply connectors.

[9V] (red)	=	+9V	(for PVDD of AK4682)
[TVDD] (red)	=	+3.3V	(for TVDD of AK4682 and AK4141)
[AVDD1] (red)	=	+3.3V	(for AVDD of AK4141)
[AVDD2] (red)	=	+3.3 V	(for AVDD2 of AK4141)
[Logic] (red)	=	+3.3V	(for VDD of AK4114 (DIR, DIT) and logic)
[DVDD] (red)	=	+1.8V	(for DVDD of AK4141)
[AGND] (black)	=	0V	(analog ground)
[DGND] (black)	=	0V	(digital ground)

(Note) AVDD1, AVDD2, DVDD1 and DVDD2 of AK4682 is supplied "5V" from regulator (T1).

2) Set up the jumper pins and switches. (See the followings.)

3) Power on.
The AK4141, AK4682, AK4114 (DIR), AK4114 (DIT) should be reset once bringing toggle SW "L" upon power-up. Please refer to Talble 1.on this page about setting of toggle SW.

■ Setting of the toggle SW

SW2	PDN_AK4141	PDN SW of AK4141 (U2). Keep "H" during normal operation.
SW3	PDN-CODEC	PDN SW of AK4682 (U5). Keep "H" during normal operation. Keep "L" when AK4682 is not used.
SW5	PDN-DIR	PDN SW of AK4114 (U7). Keep "H" during normal operation. Keep "L" when AK4114 is not used.
SW7	PDN-DIT	PDN SW of AK4114 (U9). Keep "H" during normal operation. Keep "L" when AK4114 is not used.

Table 1. Setting of the toggle SW

■ Indication for LED

LED1	INT	Output of INT pin of the AK4141 (U2). Turns on when PLL of the AK4141 (U2) is unlocked.
LED2	INT0	Output of INT0 pin of the AK4114 (U7). Turns on when the AK4114 (U7) is unlocked.

Table 2. Indication for LED

■ Setting of jumper pins

No	Name	Setting
21	TVDD	TVDD power supply REG: TVDD is supplied from regulator (T2). "TVDD" connector should be open.<Default> TM: TVDD is supplied from "TVDD" connector.
23	AVDD1	AVDD1 power supply REG: AVDD1 is supplied from regulator (T2). "AVDD1" connector should be open.<Default> TM: AVDD1 is supplied from "AVDD1" connector.
24	AVDD2	AVDD2 power supply REG: AVDD2 is supplied from regulator (T2). "AVDD2" connector should be open.<Default> TM: AVDD2 is supplied from "AVDD2" connector.
26	Logic	VDD (Logic) power supply REG: VDD is supplied from regulator (T2). "Logic" connector should be open.<Default> TM: VDD is supplied from "Logic" connector.
22	DVDD	DVDD power supply REG: DVDD is supplied from regulator (T3). "DVDD" connector should be open.<Default> TM: DVDD is supplied from "DVDD" connector.
25	GND	Analog GND and Digital GND Open: Separated. Short: Common. <Default>
20	M/S CODEC	Mode Setting of AK4682 Master: Master Mode. Slave: Slave Mode. <Default>
27	TXIN	Input of AK4141's TXIN OPT: OPT of PORT3 (RX). GND: GND. <Default>
28	RX	Input of AK4114 (DIR)'s RX OPT: OPT of PORT3 (RX). <Default> COAX: BNC of J10 (COAX).
34	TX	Output of AK4114 (DIT)'s TX1 OPT: OPT of PORT5 (TX) <Default> COAX: BNC of J11 (COAX)
2	EXT-T	Termination of J2 (External Clock) Open: No termination. <Default> Short: 51Ω.
132	MCKI	Input of AK4141's MCKI DIR: IMCLK. <Default> EXT: External clock from J11.

4	LRCK5	Input of AK4141's LRCK5 OLRCK: OLRCK. ILRCK: ILRCK. <Default>
5	SCLK5	Input of AK4141's SCLK5 OBICK: OBICK. IBICK: IBICK. <Default>
6	LRCK4	Input of AK4141's LRCK4 OLRCK: OLRCK. ILRCK: ILRCK. <Default>
7	SCLK4	Input of AK4141's SCLK4 OBICK: OBICK IBICK: IBICK <Default>
9	SDTI5	Input of AK4141's SDTI5 DIR: SDTO of DIR (U7) <Default> ADC: SDTOB of AK4682 (U5). GND: GND.
12	SDTI4	Input of AK4141's SDTI4 DIR: SDTI of DIR (U7) <Default> ADC: SDTOB of AK4682 (U5). GND: GND.
13	SDTI3	Input of AK4141's SDTI3 DIR: SDTI of DIR (U7) <Default> ADC: SDTOB of AK4682 (U5). GND: GND.
15	SDTI2	Input of AK4141's SDTI2 DIR: SDTI of DIR (U7) <Default> ADC: SDTOB of AK4682 (U5). GND: GND.
17	SDTI1	Input of AK4141's SDTI2 DIR: SDTI of DIR (U7) <Default> ADC: SDTOB of AK4682 (U5). GND: GND.
8	SDTO	Input of DIT (U9)'s DAUX SDTO1: Output of AK4141's SDTO1 <Default> SDTO2: Output of AK4141's SDTO2 SDTO3: Output of AK4141's SDTO3
14	SDTIA1	Input of AK4682 (U5)'s SDTIA1 SDTO1: Output of AK4141's SDTO1 <Default> SDTO2: Output of AK4141's SDTO2 SDTO3: Output of AK4141's SDTO3
16	SDTIA2	Input of AK4682 (U5)'s SDTIA2 SDTO1: Output of AK4141's SDTO1 <Default> SDTO2: Output of AK4141's SDTO2 SDTO3: Output of AK4141's SDTO3
32	IMCLK	IMCLK and DIR (U7)'s MCKO1 Open: Separated. Short: Connected. <Default>
31	ILRCK	ILRCK and DIR (U7)'s LRCK Open: Separated. Short: Connected. <Default>
29	IBICK1	IBICK and DIR (U7)'s BICK Open: Separated. Short: Connected. <Default>

30	SDTI	SDTI and DIR (U7)'s SDTO Open: Separated. Short: Connected. <Default>
33	IBICK2	Polarity of IBICK THR: Through. <Default> INV: Invert.
39	ILRCK	ILRCK and DIT (U9)'s LRCK Open: Separated. <Default> Short: Connected.
38	OLRCK	OLRCK and DIT (U9)'s LRCK Open: Separated. <Default> Short: Connected.
37	IBICK	IBICK and DIT (U9)'s BICK Open: Separated. <Default> Short: Connected.
36	OBICK1	OBICK and DIT (U9)'s BICK Open: Separated. <Default> Short: Connected.
35	SDTO	SDTO and DIT (U9)'s DAUX Open: Separated. <Default> Short: Connected.
41	OBICK2	Polarity of OBICK THR: Through. <Default> INV: Invert.

Table 3. Setting of jumper pins

■ Evaluation mode

The setup sequence from the initial state

The AKD4141 can evaluate various mode using AK4682 (CODEC), AK4114 (DIR) and AK4114 (DIT). Set jumper pins and SW to condition to evaluate. About AK4141 and AK4682, refer to each datasheet. About DIR and DIT, refer to Table 5.~ Table 10. in this manual.
Follows are setting examples of AK4141's decoder.

Measurement path :
- SIF (J1) → AK4141 (Stereo decoder) → DAC (AK4682) → LOUT1/ROUT1
- SIF (J1) → AK4141 (Stereo decoder) → DIT (AK4141) → TX (PORT1)

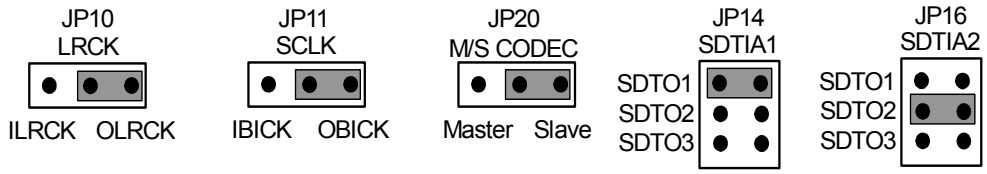
Setting of AK4141 :
Using X'tal Oscillator, Master mode MCLK=256fjs, fs=48kHz.

(1) Setting of MCLK. X'tal Oscillator (X1) is used.
12.288MHz (fs=48kHz, MCLK=256fs) is equipped on the board by initial setting.
When evaluate it in other conditions, please attach a X'tal oscillator according to evaluation mode.

(2) Setting of DIP SW1.
(2-1) Setting of Master Mode
Please set MSN (No.6) of DIP SW1 to "H". (Master Mode : MCKI=256fs)

(2-2) Setting of SIF input. Please set 6M5 pin and 4M5[2-0] pin according to carrier frequency.
(2-2-1) In case of including the 6.5MHz carrier.
6M5 (No.5) of DIP SW1 = "L" : L NICAM.
6M5 (No.5) of DIP SW1 = "H" : D/K
(2-2-2) In case of including the 4.5MHz carrier.
4M5[2-0] (No.4-2) of DIP SW1 = "LHL" : EIAJ.
4M5[2-0] (No.4-2) of DIP SW1 = "LLH" : M-Korea.
4M5[2-0] (No.4-2) of DIP SW1 = "LLL" : PAL (Chroma Carrier)
4M5[2-0] (No.4-2) of DIP SW1 = "HLL" : FM-Stereo Radio EU
4M5[2-0] (No.4-2) of DIP SW1 = "HHH" : FM-Stereo Radio US
(Note.) The details please refer to Table 4. in this manual.

(3) Setting of the jumper pins. Jumper pins should be set as follows.
Please set JP14 and JP16 according to the output of AK4141.
The following are setting examples of JP14=SDTO1 and JP16=SDTO2.



(4) Please set toggle SW2 (AK4141) to "H".

(5) Please write register of AK4141 with control software.
The following is register setting from the initial state of AK4141.

01H : MCKE bit & MCKD bit "0" → "1" (MCKO output for AK4682 : MCKO=256fs)

(6) Please supply SIF signal from J1 (SIF1).

(7) Please write register of AK4141 with control software.
41H : ASD bit = "0" → "1". (Automatic system detection ON)

(8) Please set toggle SW3 (CODEC) to “H”.

(9) Please write register of AK4682 with control software.
The following is register setting from the initial state of AK4682.

1. 02H : DIFA[1-0] bit “11” → “10” (Audio interface format : Left justified)
(Note) In case of AK4141 evaluation using AK4682, it is necessary to correspond to audio interface format for AK4141 and AK4682. Audio interface format of AK4141’s initial state is Left justified.

■ Setting of DIP SW

(1). Setting of SW1 (AK4141)

SW1 No.	Name	ON ("H")	OFF ("L")	Default
1	IIS	Audio Data Format Select Pin. ORed with ODIF bit, ORed with IDIF0 bit. "L": 24 bit Left Justified if IDIF0 bit = "0" (default). "H": 24/16 bit IIS.		L
2	4M50	Decoder Standard Preference Control 0 for 4.5MHz carrier.		L
3	4M51	4M5 [2:0] pin		L
4	4M52	"LLL": PAL (Chroma Carrier) "LLH": M-Korea "LHL": EIAJ "LHH": Reserved "HLL": FM-Stereo Radio EU "HLH": FM-Stereo Radio EU "HHL": FM-Stereo Radio EU "HHH": FM-Stereo Radio US This Pin is internally XORed with 4M5[2-0] bit (default = "011").		L
5	6M5	Decoder Standard Preference Control for 6.5MHz carrier. "L": SECAM L NICAM "H": D/K1, D/K2, D/K3 or D/K NICAM This Pin is internally XORed with 6M5 bit (default = "0").		L
6	MSN	Master Mode Select Pin. ORed with CKS [1:0] bits. "L": Slave mode if CKS [2:0] bits = "000" (default). "H": Master mode of MCLK=256fs if CKS2 bit = "0" (default).		L
7	CAD0	Chip Address 0 pin. Should match CAD0 bit in IIC first byte.		L
8	CAD1	Chip Address 1 pin. Should match CAD1 bit in IIC first byte.		L

Table 4. SW1 Setting

(2). Setting of SW4 (DIR: AK4114)

SW4 No.	Name	ON ("H")	OFF ("L")	Default
1	DIF2	AK4114 Output Audio Interface Format Setting refer to Table 6.		H
2	DIF1			L
3	DIF0			L
4	CM1	AK4114 Clock Mode Setting Fixed to "L".		L
5	CM0			L
6	OCKS1	AK4114 Master Clock Frequency Setting refer to Table 7		H
7	OCKS0			L

Table 5. SW4 Setting

Mode	DIF2 pin	DIF1 pin	DIF0 pin	SDTO Format	LRCK		BICK		
						I/O		I/O	
0	L	L	L	16bit, Right justified	H/L	O	64fs	O	
1	L	L	H	18bit, Right justified	H/L	O	64fs	O	
2	L	H	L	20bit, Right justified	H/L	O	64fs	O	
3	L	H	H	24bit, Right justified	H/L	O	64fs	O	
4	H	L	L	24bit, Left justified	H/L	O	64fs	O	(Default)
5	H	L	H	24bit, I^2S Compatible	L/H	O	64fs	O	
6	H	H	L	24bit, Left justified	H/L	I	64-128fs	I	
7	H	H	H	24bit, I^2S Compatible	L/H	I	64-128fs	I	

Table 6. AK4114 Output Audio Interface Format Setting

Mode	OCKS1 pin	OCKS0 pin	MCKO1	fs (max)	
0	L	L	256fs	96 kHz	
1	L	H	256fs	96 kHz	
2	H	L	512fs	48 kHz	(Default)
3	H	H	128fs	192 kHz	

Table 7. AK4114 Master Clock Frequency Setting

(3). Setting of SW6 (DIT: AK4114)

SW6 No.	Name	ON ("H")	OFF ("L")	Default
1	DIF2	AK4114 Input Audio Interface Format Setting refer to Table 9.		H
2	DIF1			L
3	DIF0			L
4	CM1	AK4114 Clock Mode Setting Fixed to "L".		L
5	CM0	AK4114 Clock Mode Setting Fixed to "H".		H
6	OCKS1	AK4114 Master Clock Frequency Setting refer to Table 10.		L
7	OCKS0			L

Table 8. SW6 Setting

Mode	DIF2 pin	DIF1 pin	DIF0 pin	DAUX Format	LRCK		BICK		
						I/O		I/O	
0	L	L	L	24bit, Left justified	H/L	O	64fs	O	
1	L	L	H	24bit, Left justified	H/L	O	64fs	O	
2	L	H	L	24bit, Left justified	H/L	O	64fs	O	
3	L	H	H	24bit, Left justified	H/L	O	64fs	O	
4	H	L	L	24bit, Left justified	H/L	O	64fs	O	(Default)
5	H	L	H	24bit, I^2S Compatible	L/H	O	64fs	O	
6	H	H	L	24bit, Left justified	H/L	I	64-128fs	I	
7	H	H	H	24bit, I^2S Compatible	L/H	I	64-128fs	I	

Table 9. AK4114 Input Audio Interface Format Setting

Mode	OCKS1 pin	OCKS0 pin	MCKO1	fs (max)	
0	L	L	256fs	96 kHz	(Default)
1	L	H	256fs	96 kHz	
2	H	L	512fs	48 kHz	
3	H	H	128fs	192 kHz	

Table 10. AK4114 Master Clock Frequency Setting

■ Serial Control

The AK4141 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT2 (CTRL) with PC by 10 wire flat cable packed with the AKD4141.

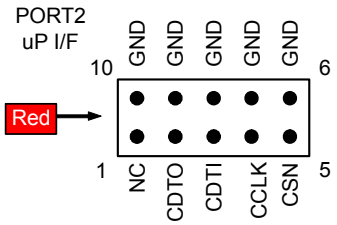


Figure 2. Connect of 10 wire flat cable

Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4141-A according to previous term.

2. Connect IBM-AT compatible PC with AKD4141-A by 10-line type flat cable (packed with AKD4141-A). Take care of the direction of 10pin header. (Please install the driver in the CD-ROM when this control software is used on Windows 2000/XP. Please refer "Installation Manual of Control Software Driver by AKM device control software". In case of Windows95/98/ME, this installation is not needed. This control software does not operate on Windows NT.)

3. Insert the CD-ROM labeled "AK4141-A Evaluation Kit" into the CD-ROM drive.

4. Access the CD-ROM drive and double-click the icon of "akd4141.exe" and "akd4682 .exe" to set up the control program.

5. Then please evaluate according to the follows.

■ Operation flow

Keep the following flow.

1. Set up the control program according to explanation above.
2. Click "Port Reset" button.
3. Click "Write default" button

■ Explanation of each buttons

[Port Reset] :	Set up the USB interface board (AKDUSBIF-A) .
[Write default] :	Initialize the register of AK4141.
[All Write] :	Write all registers that is currently displayed.
[All Read] :	Read all registers of the AK4141.
[Function1] :	Dialog to write data by keyboard operation.
[Function2] :	Dialog to write data by keyboard operation.
[Function3] :	The sequence of register setting can be set and executed.
[Function4] :	The sequence that is created on [Function3] can be assigned to buttons and executed.
[Function5]:	The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed.
[SAVE] :	Save the current register setting.
[OPEN] :	Write the saved values to all register.
[Write] :	Dialog to write data by mouse operation.
[Read]:	Dialog to read data by mouse operation.

■ Indication of data

Input data is indicated on the register map. Red letter indicates "H" or "1" and blue one indicates "L" or "0". Blank is the part that is not defined in the datasheet.

■ Explanation of each dialog

1. [Write Dialog] : Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the [Write] button corresponding to each register to set up the dialog. If you check the check box, data becomes "H" or "1". If not, "L" or "0".

If you want to write the input data to AK4141, click [OK] button. If not, click [Cancel] button.

2. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input registers address in 2 figures of hexadecimal.
Data Box: Input registers data in 2 figures of hexadecimal.

If you want to write the input data to AK4141, click [OK] button. If not, click [Cancel] button.

3. [Function2 Dialog] : Dialog to evaluate VOL

Address Box: Input registers address in 2 figures of hexadecimal.
Start Data Box: Input starts data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4141 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK4141, click [OK] button. If not, click [Cancel] button.

4. [Save] and [Open]

4-1. [Save]

Save the current register setting data. The extension of file name is “akr”.

<Operation flow>
(1) Click [Save] Button.
(2) Set the file name and push [Save] Button. The extension of file name is “akr”.

4-2. [Open]

The register setting data saved by [Save] is written to AK4141. The file type is the same as [Save].

<Operation flow>
(1) Click [Open] Button.
(2) Select the file (*.akr) and Click [Open] Button.

5. [Function3 Dialog]

The sequence of register setting can be set and executed.

(1) Click [F3] Button.

(2) Set the control sequence.
Set the address, Data and Interval time. Set "-1" to the address of the step where the sequence should be paused.

(3) Click [Start] button. Then this sequence is executed.

The sequence is paused at the step of Interval="-1". Click [START] button, the sequence restarts from the paused step.

This sequence can be saved and opened by [Save] and [Open] button on the Function3 window. The extension of file name is "aks".

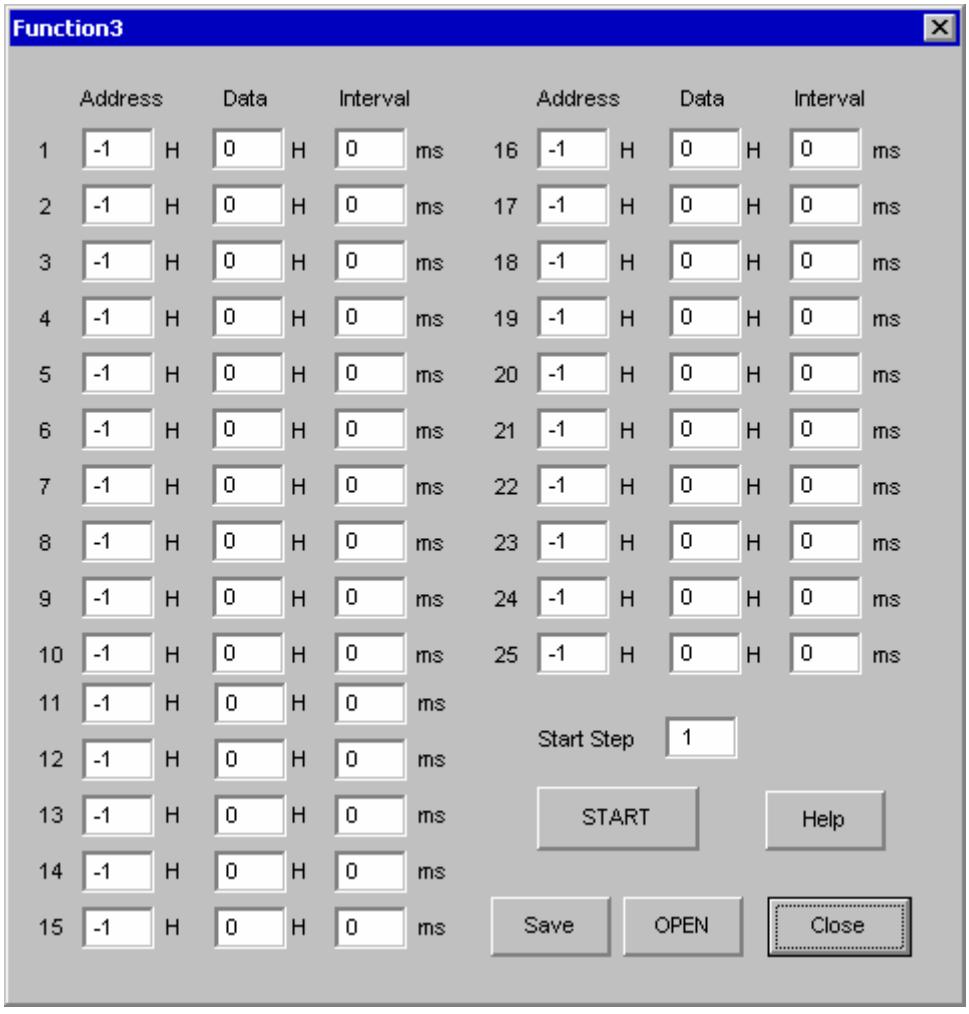


Figure 3. Window of [F3]

6. [Function4 Dialog]

The sequence that is created on [Function3] can be assigned to buttons and executed. When [F4] button is clicked, the window as shown in Figure 4. opens.

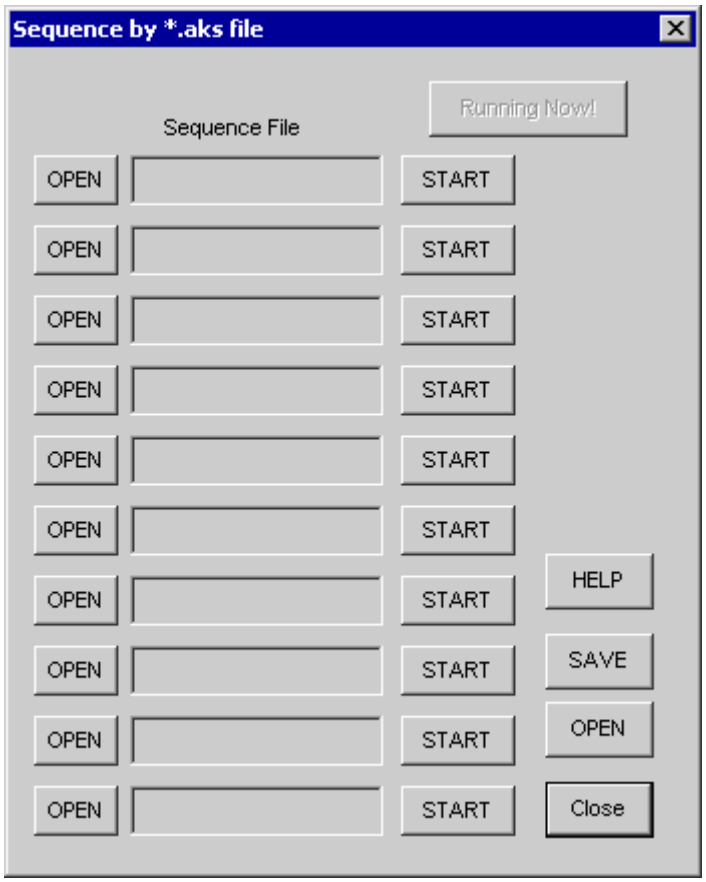


Figure 4. [F4] window

6-1. [OPEN] buttons on left side and [START] buttons

(1) Click [OPEN] button and select the sequence file (*.aks).

The sequence file name is displayed as shown in Figure 5.

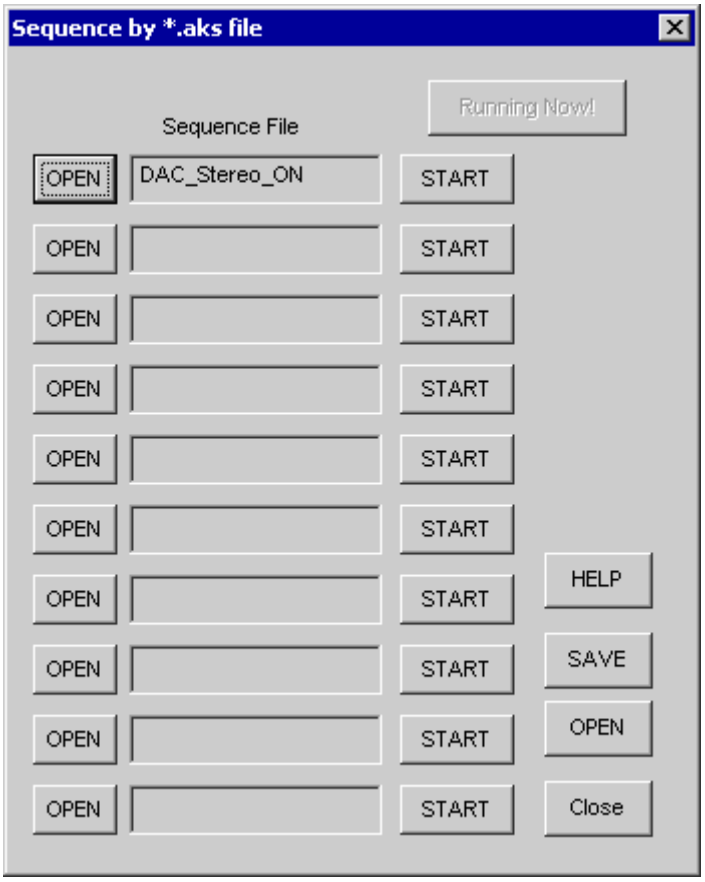


Figure 5. [F4] window (2)

(2) Click [START] button, then the sequence is executed.

6-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The sequence file names can assign be saved. The file name is *.ak4.

[OPEN] : The sequence file names assign that are saved in *.ak4 are loaded.

6-3. Note

(1) This function doesn't support the pause function of sequence function.

(2) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(3) When the sequence is changed in [Function3], the file should be loaded again in order to reflect the change.

7. [Function5 Dialog]

The register setting that is created by [SAVE] function on main window can be assigned to buttons and executed. When [F5] button is clicked, the following window as shown in Figure 6.opens.

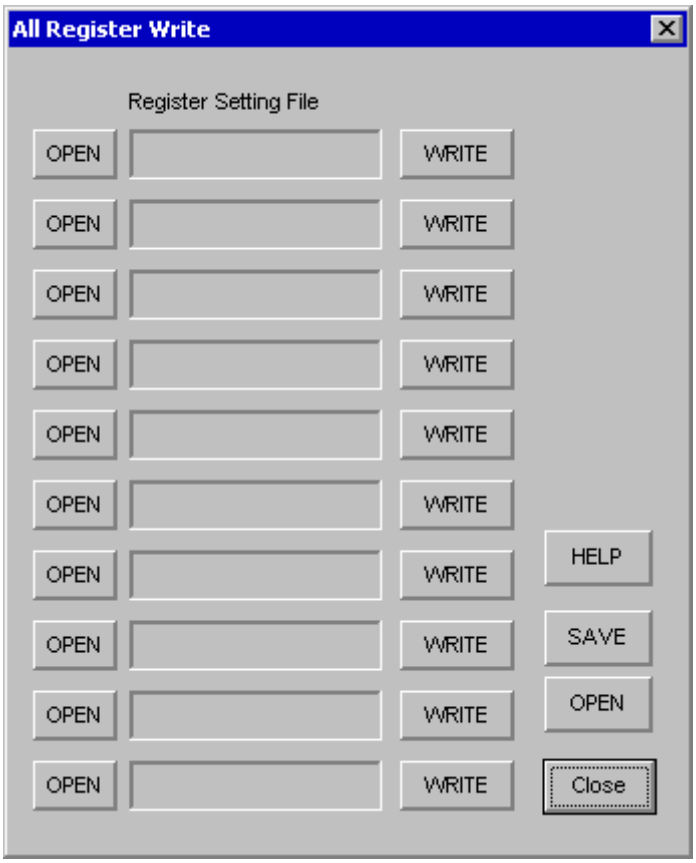


Figure 6. [F5] window

7-1. [OPEN] buttons on left side and [WRITE] button

(1) Click [OPEN] button and select the register setting file (*.akr).

The register setting file name is displayed as shown in Figure 7.

(2) Click [WRITE] button, then the register setting is executed.

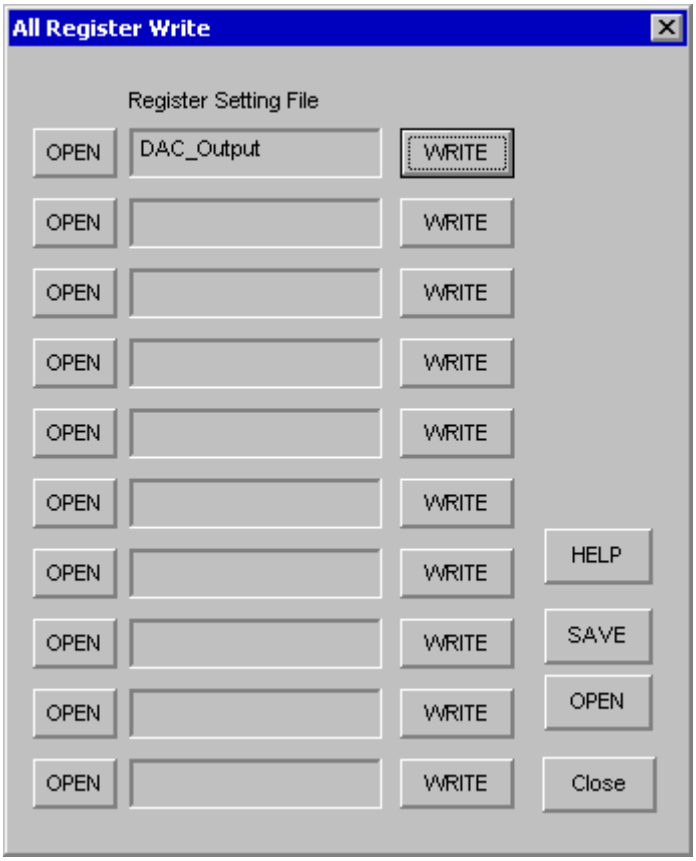


Figure 7. [F5] windows(2)

7-2. [SAVE] and [OPEN] buttons on right side

[SAVE] : The register setting file names assign can be saved. The file name is *.ak5.

[OPEN] : The register setting file names assign that are saved in *.ak5 are loaded.

7-3. Note

(1) All files need to be in same folder used by [SAVE] and [OPEN] function on right side.

(2) When the register setting is changed by [Save] Button in main window, the file should be loaded again in order to reflect the change.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision, System Two Cascade
  ROHDE & SCHWARZ, TV TEST TRANSMITTER SFM
- fs : 48kHz
- Power Supply : AVDD = TVDD = 3.3V, DVDD = 1.8V
- Temperature : Room

[Measurement Results]

FM Characteristics (BG A2)		Result (Lch / Rch)	Unit
S / (N+D)	0dB Input	63.2 / 68.4	dB
S / N	No Signal, A-weighting	69.5 / 73.4	dB
NICAM Characteristics (BG NICAM)		Result (Lch / Rch)	Unit
S / (N+D)	0dB Input	67.4 / 67.3	dB
Dynamic Range	-60dB Input, A-weighting	79.0 / 78.8	dB
AM Characteristics (L)		Result (Mono)	Unit
S / (N+D)	0dB Input	40.1	dB
S / N	No Signal, A-weighting	72.2	dB

[Plots]

FM : BG A2

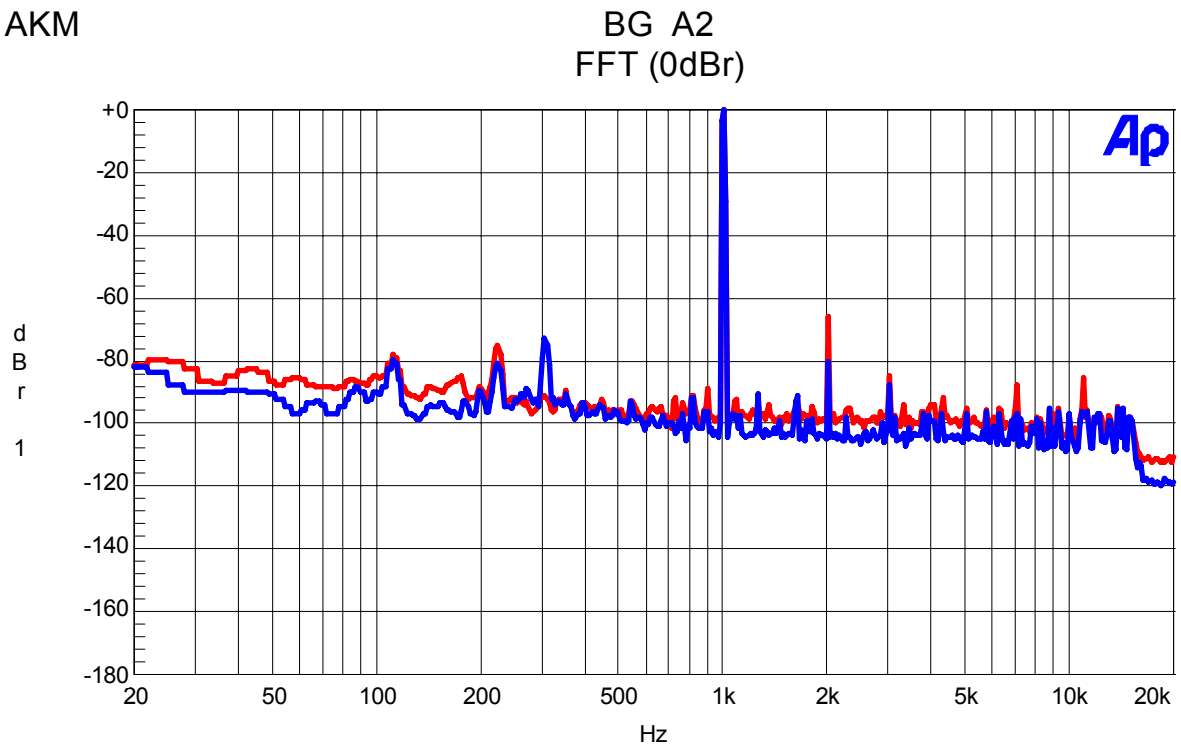


Figure 8. FFT (0dB Input)

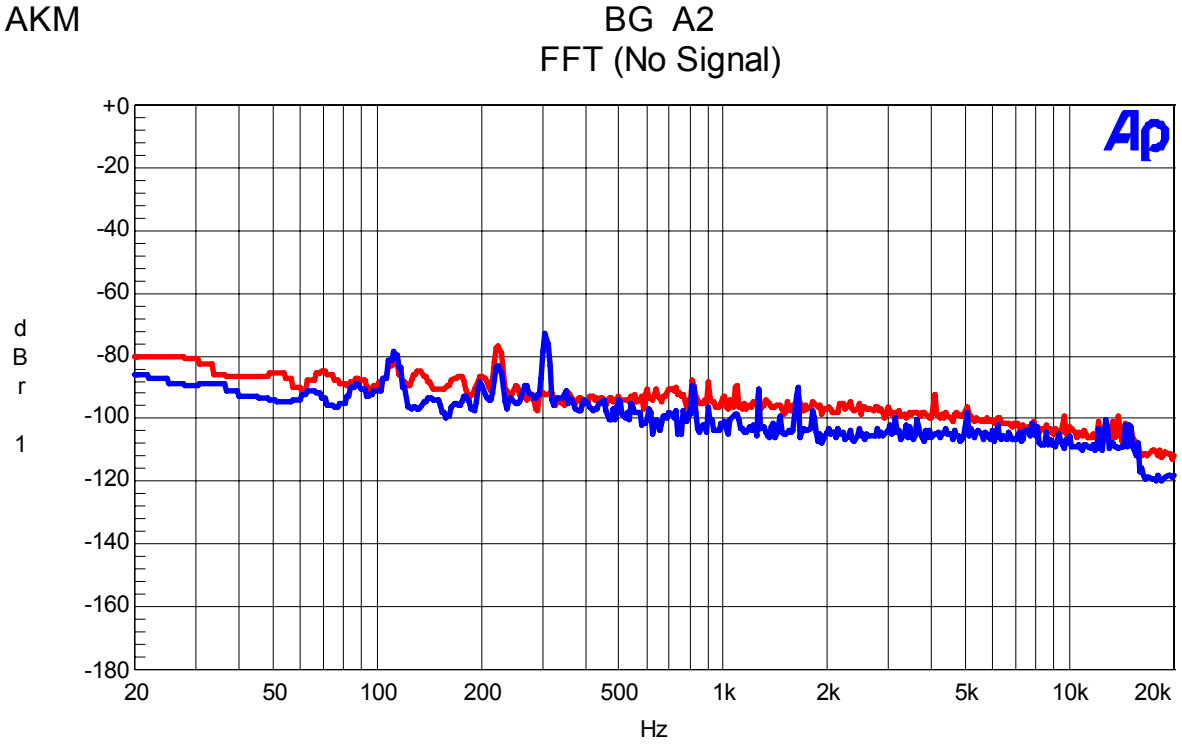


Figure 9. FFT (No Signal)

NICAM : BG NICAM

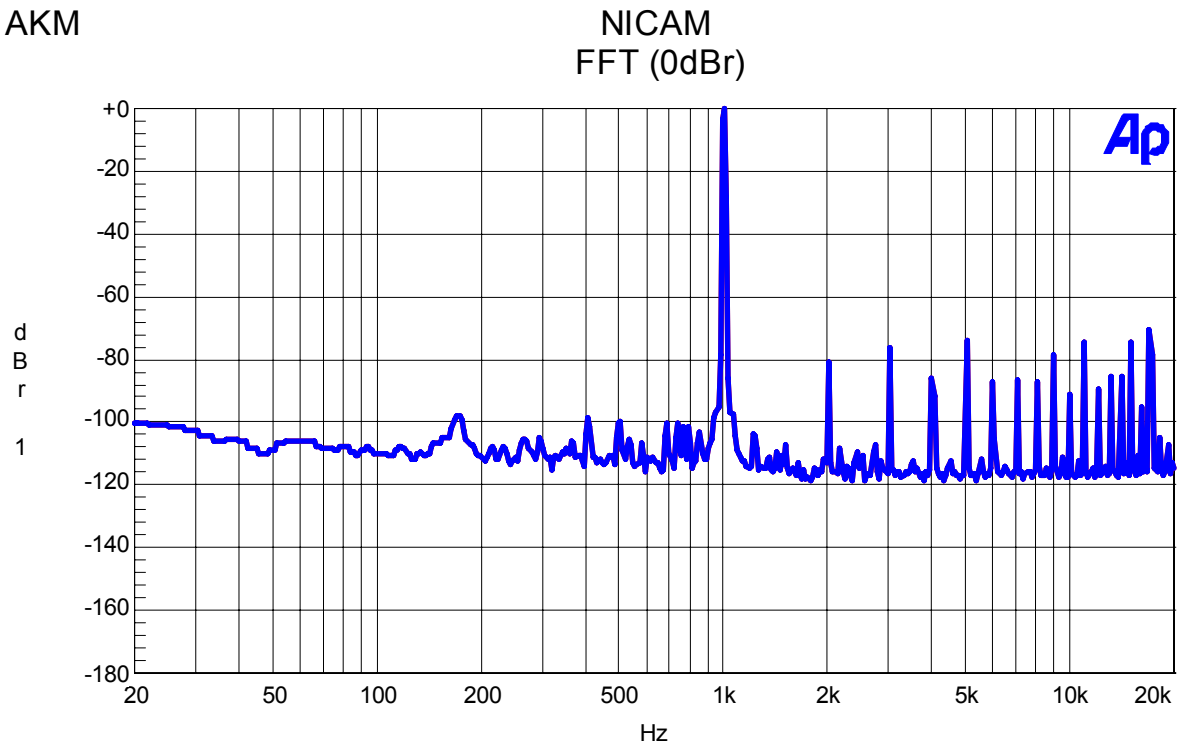


Figure 10. FFT (0dB Input)

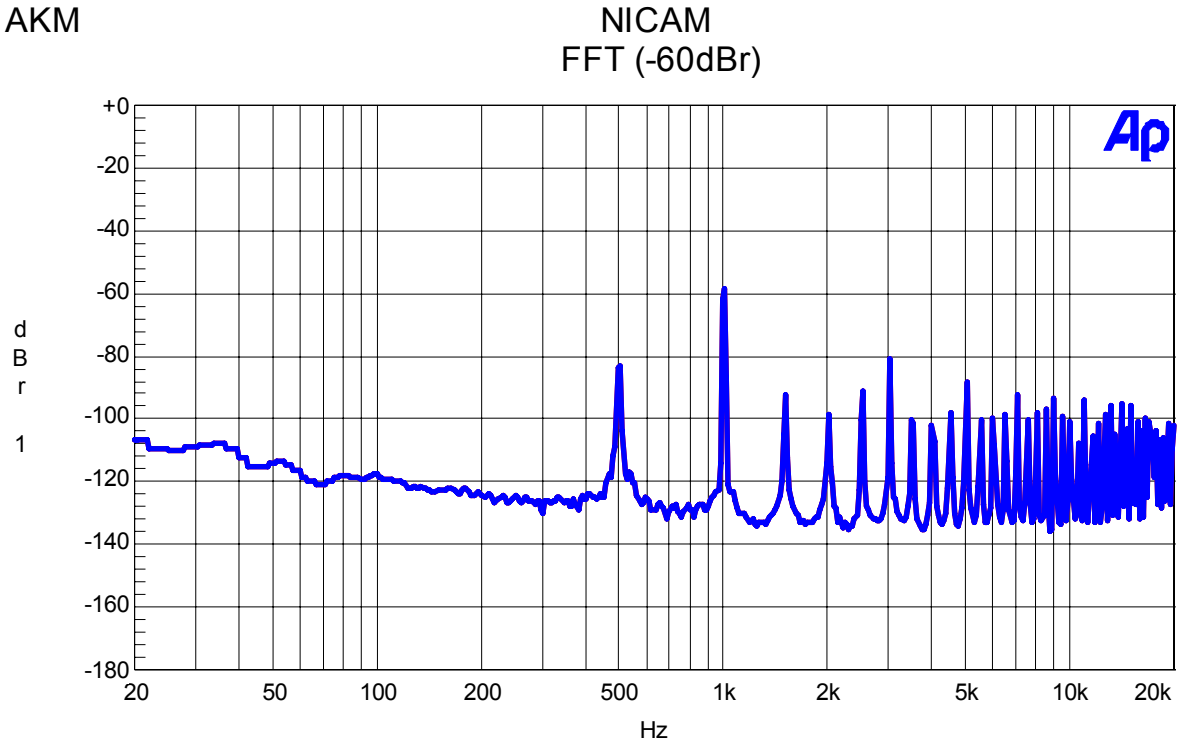


Figure 11. FFT (-60dB Input)

AM : L

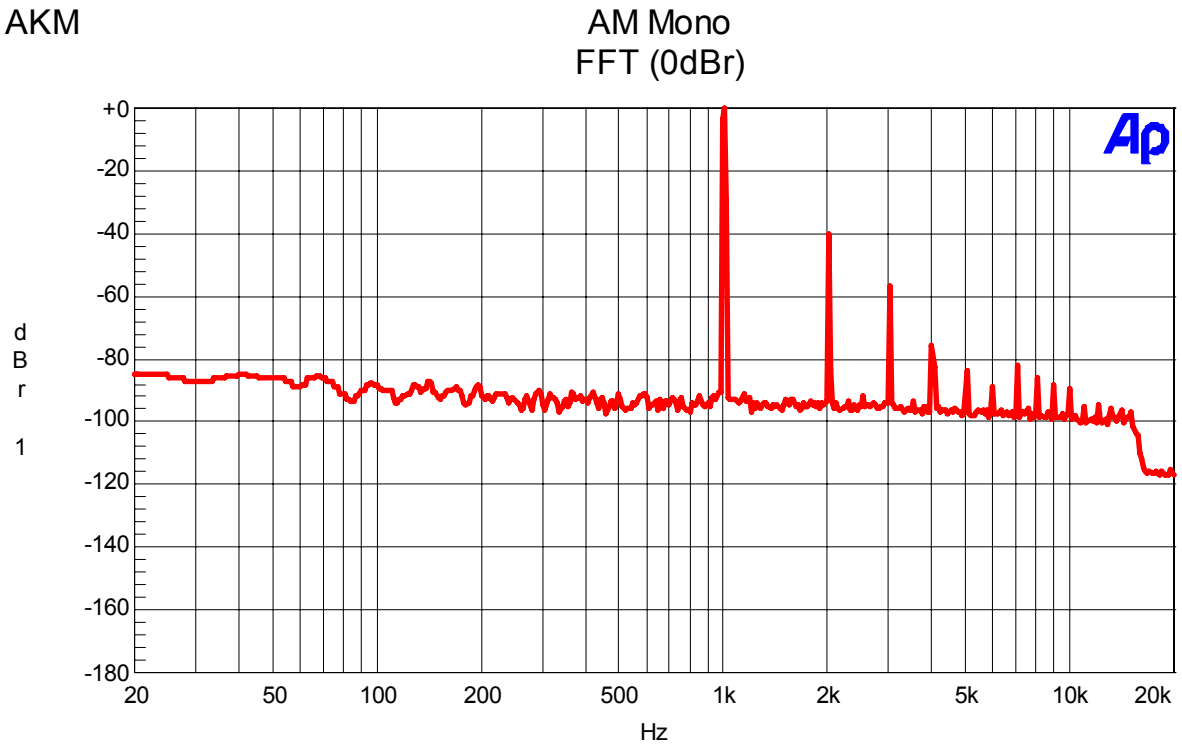


Figure 12. FFT (0dB Input)

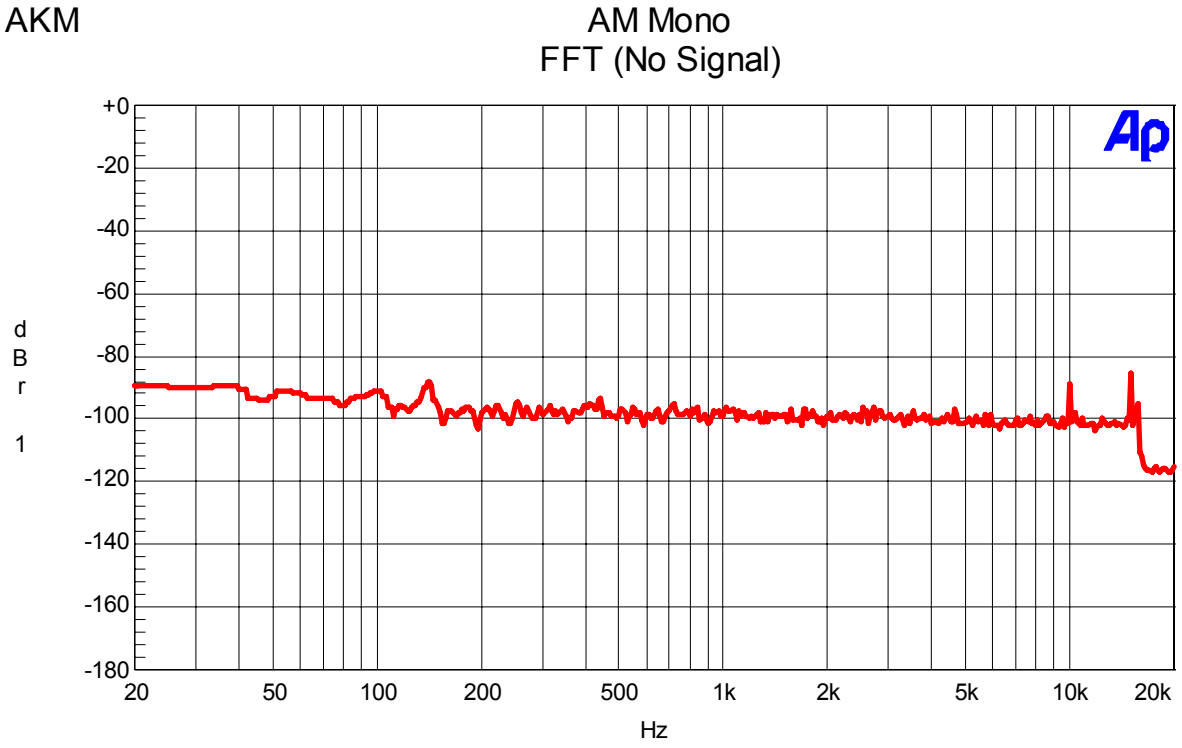


Figure 13. FFT (No Signal)

Revision History

Date (yy/mm/dd)	Manual Revision	Board Revision	Reason	Page	Contents
07/05/30	KM088100	0	First Edition		
07/06/26	KM088101	1	Change	24	Circuit diagram was changed. C12: 0.1uF → 1uF
07/11/13	KM088102	2	Change		Device revision was changed. Rev.A → Rev.B
			Change	24	Circuit diagram was changed. C14: 47nF → 4.7nF
			Addition	19-22	Table data and plot data were added.

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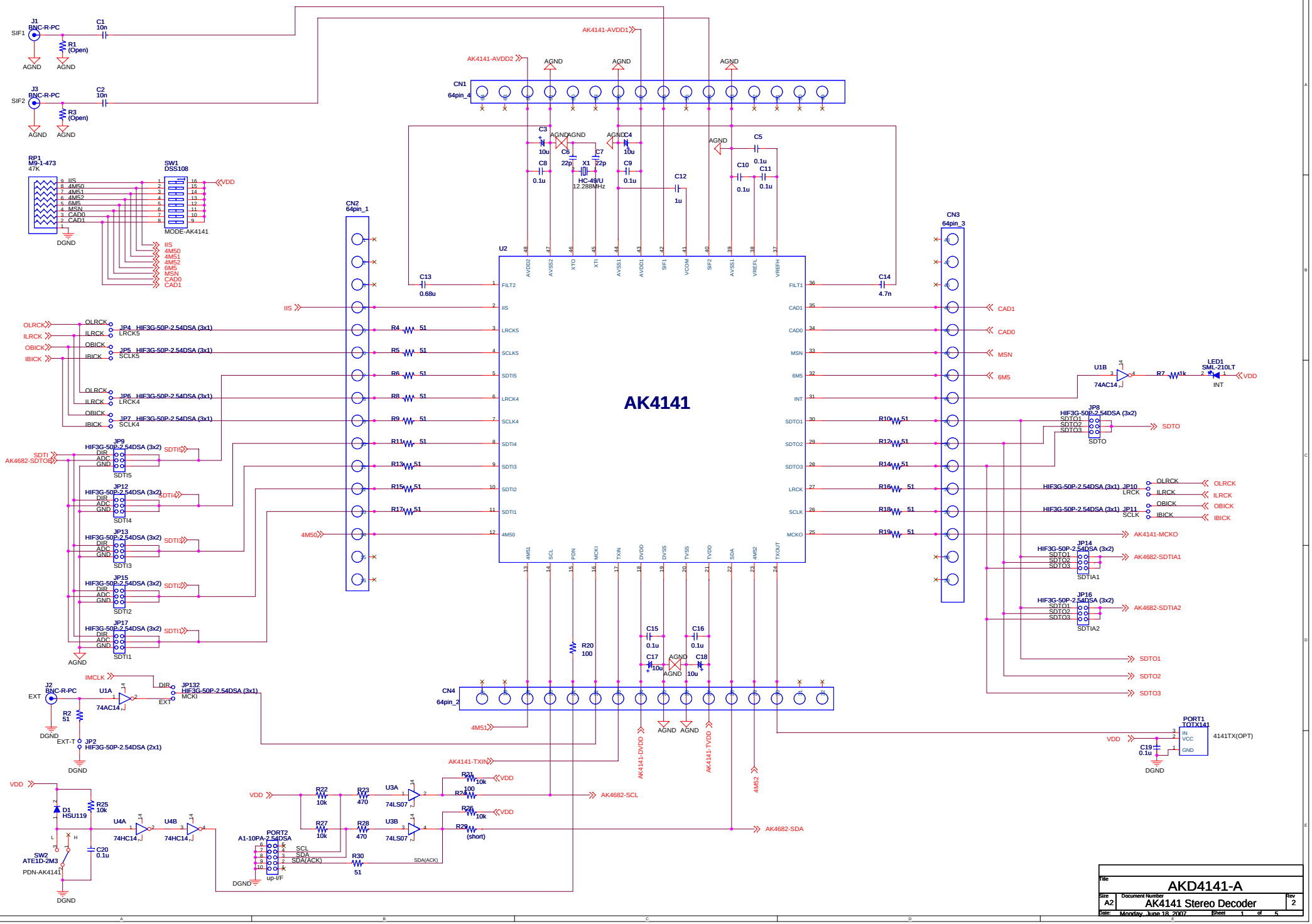

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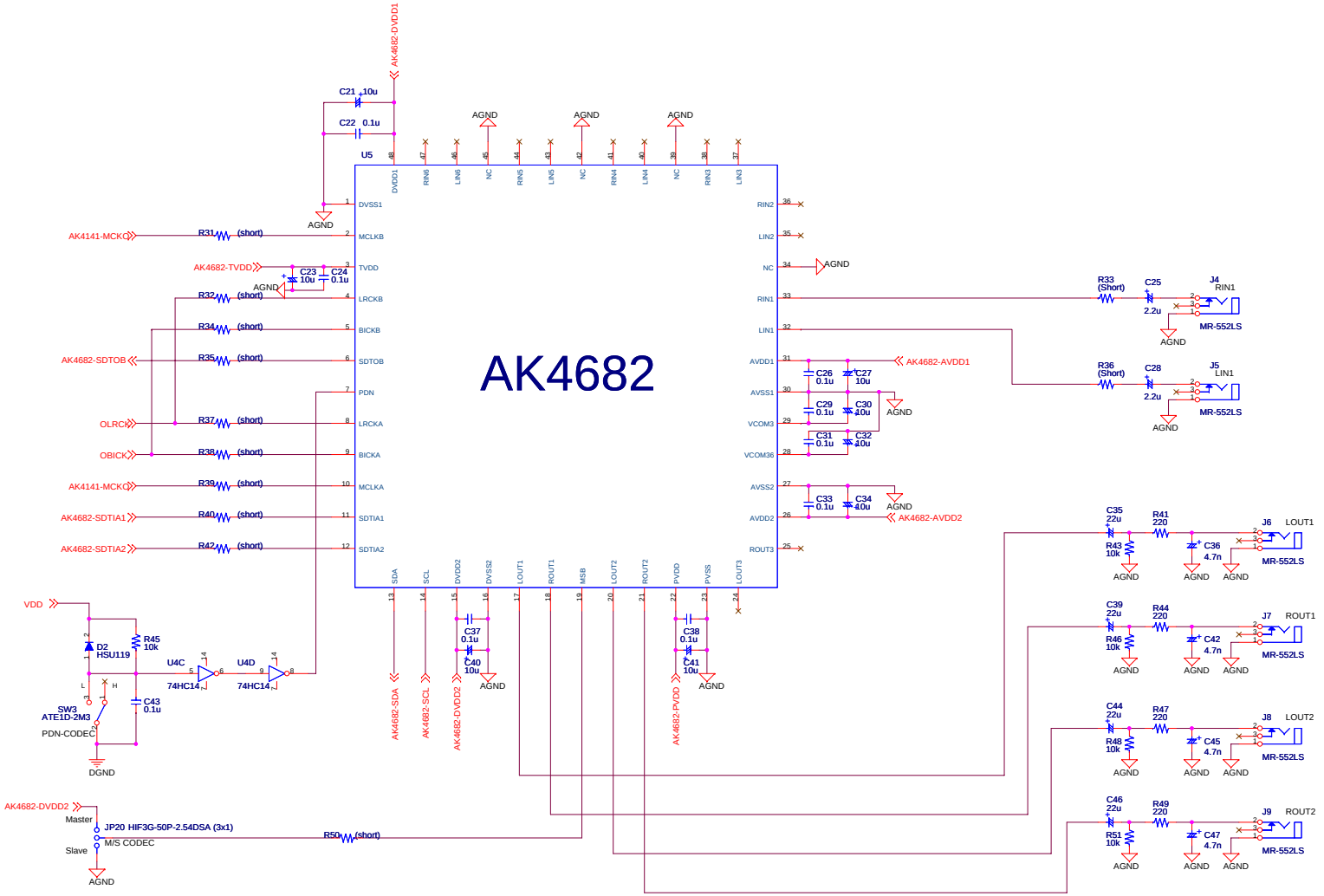
Size: A2	Document Number: AK4141 Stereo Decoder	Rev: 2
Date: Monday, June 18, 2007	Sheet 1 of 5	



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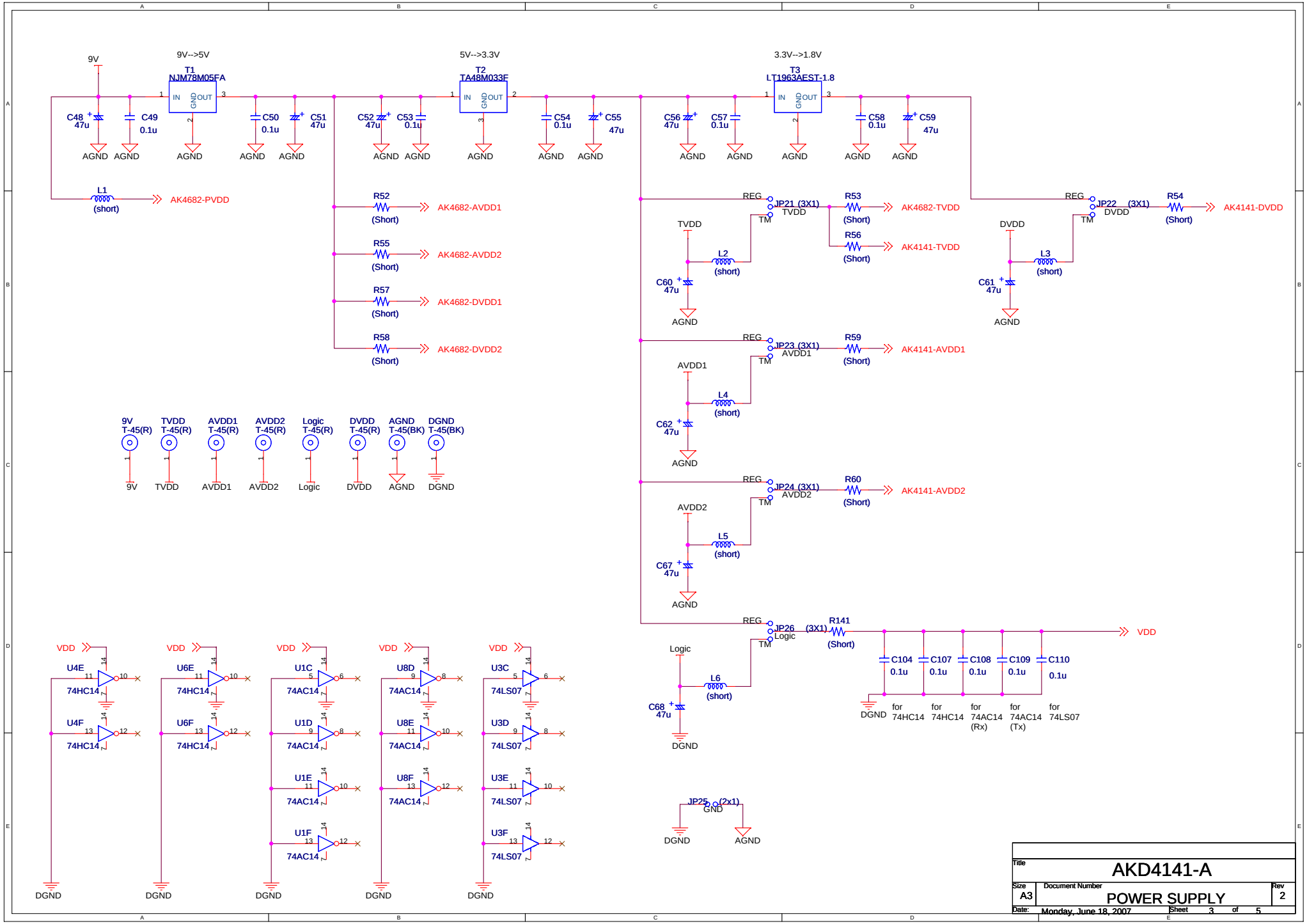
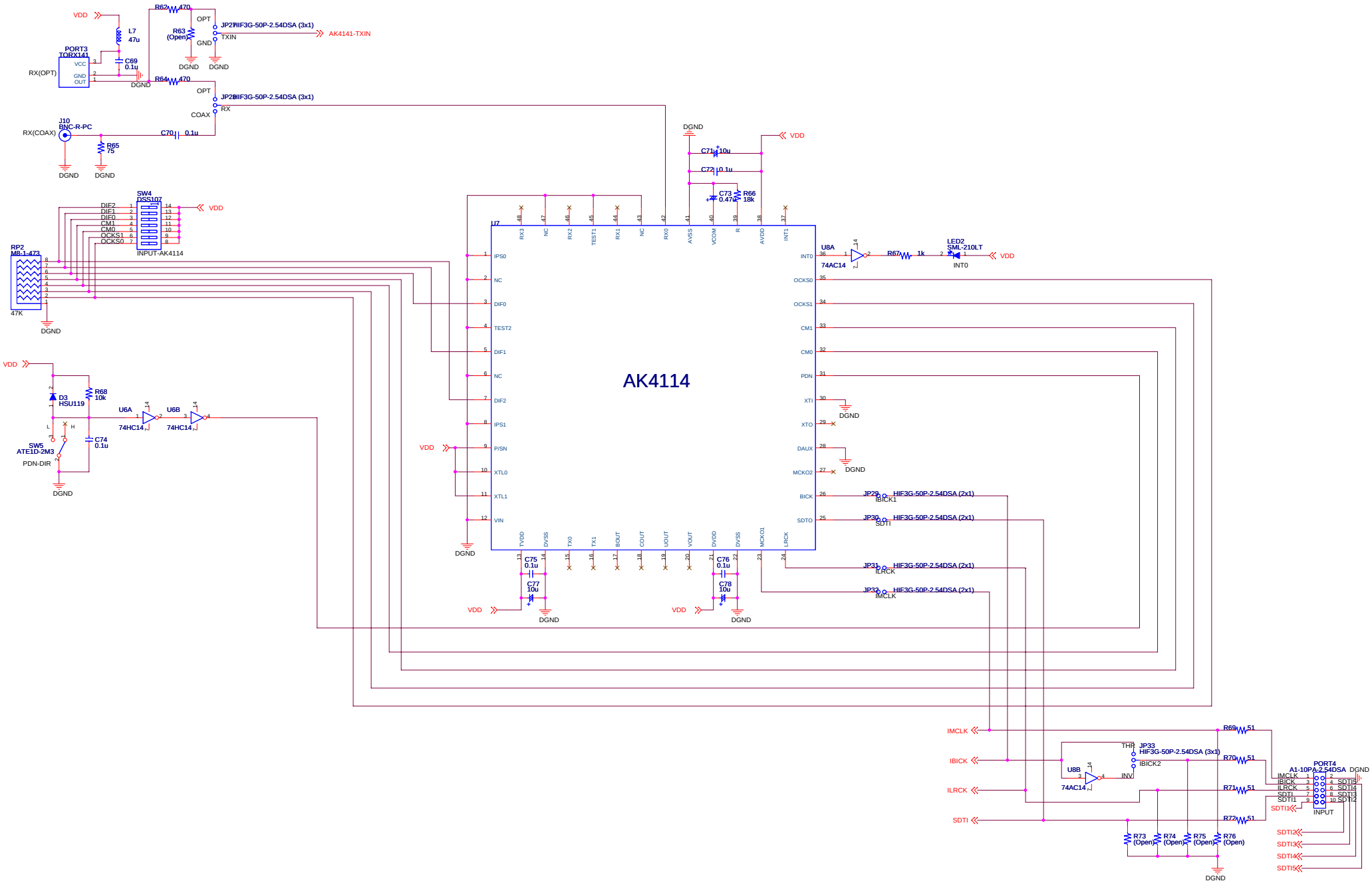
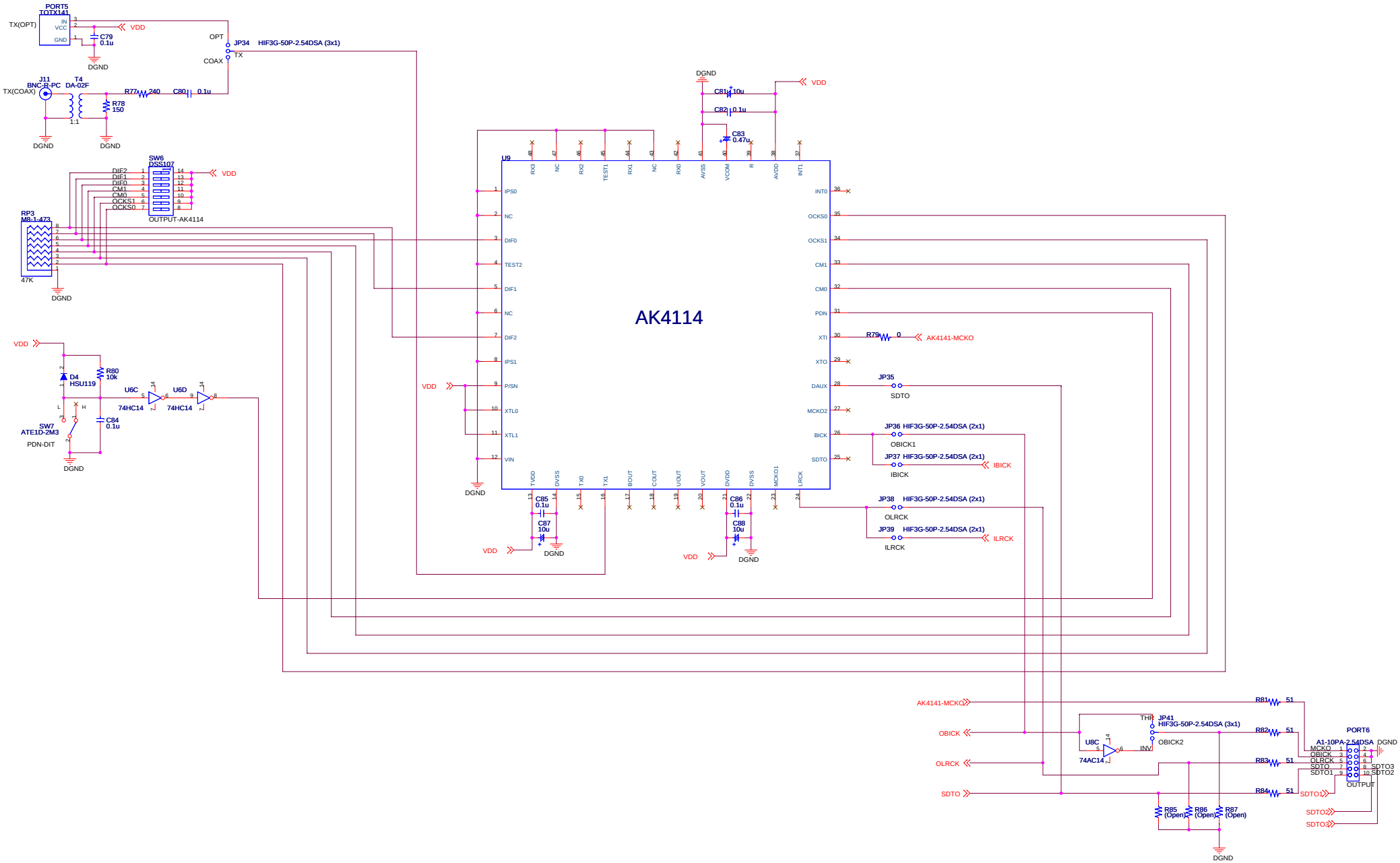
Size: A2	Document Number: AK4682 CODEC	Rev: 2
Date: Tuesday, November 13, 2007	Sheet 2 of 5	


9V
9V-->5V
T1
NJM78M05FA
5V-->3.3V
T2
TA48M033F
3.3V-->1.8V
T3
LT1963AEST-1.8
C48 47u
C49 0.1u
C50 0.1u
C51 47u
C52 47u
C53 0.1u
C54 0.1u
C55 47u
C56 47u
C57 0.1u
C58 0.1u
C59 47u
AGND
L1 (short)
AK4682-PVDD
R52 (Short)
AK4682-AVDD1
R55 (Short)
AK4682-AVDD2
R57 (Short)
AK4682-DVDD1
R58 (Short)
AK4682-DVDD2
REG
JP21 (3X1)
TVDD
TM
R53 (Short)
AK4682-TVDD
R56 (Short)
AK4141-TVDD
L2 (short)
C60 47u
JP22 (3X1)
DVDD
R54 (Short)
AK4141-DVDD
L3 (short)
C61 47u
JP23 (3X1)
AVDD1
R59 (Short)
AK4141-AVDD1
L4 (short)
C62 47u
JP24 (3X1)
AVDD2
R60 (Short)
AK4141-AVDD2
L5 (short)
C67 47u
JP26 (3X1)
Logic
R141 (Short)
VDD
L6 (short)
C68 47u
C104 0.1u
C107 0.1u
C108 0.1u
C109 0.1u
C110 0.1u
for 74HC14
for 74HC14
for 74AC14 (Rx)
for 74AC14 (Tx)
for 74LS07
DGND
9V T-45(R)
TVDD T-45(R)
AVDD1 T-45(R)
AVDD2 T-45(R)
Logic T-45(R)
DVDD T-45(R)
AGND T-45(BK)
DGND T-45(BK)
U4E 74HC14
U4F 74HC14
U6E 74HC14
U6F 74HC14
U1C 74AC14
U1D 74AC14
U1E 74AC14
U1F 74AC14
U8D 74AC14
U8E 74AC14
U8F 74AC14
U3C 74LS07
U3D 74LS07
U3E 74LS07
U3F 74LS07
JP25 (2x1)
GND
Title
AKD4141-A
Size A3
Document Number
POWER SUPPLY
Rev 2
Date: Monday, June 18, 2007
Sheet 3 of 5


AK4114
AK4141-TXIN
INPUT-AK4114
INPUT
AKD4141-A
S/PDIF INPUT
Monday, June 18, 2007
Sheet 4 of 5
Rev 2



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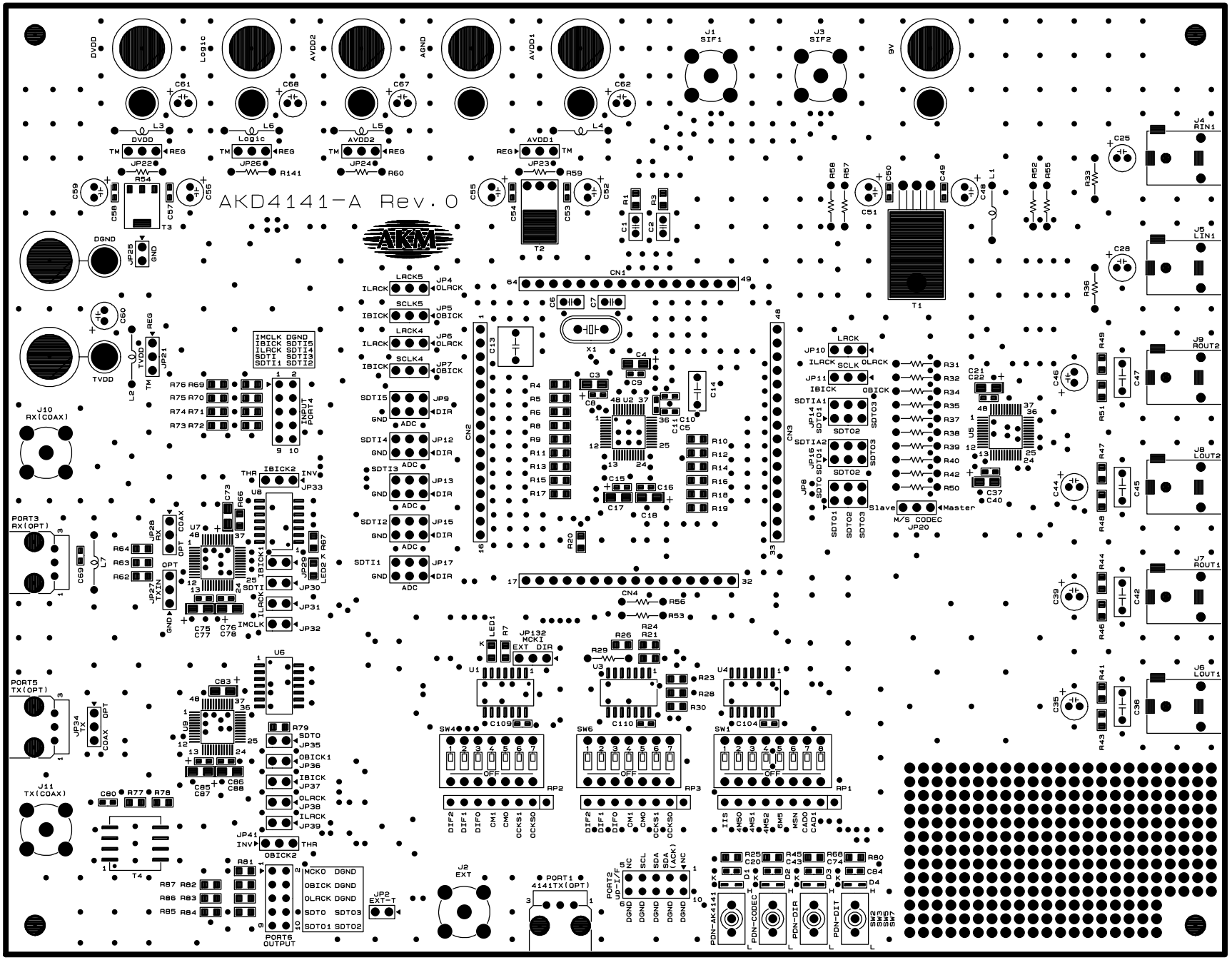
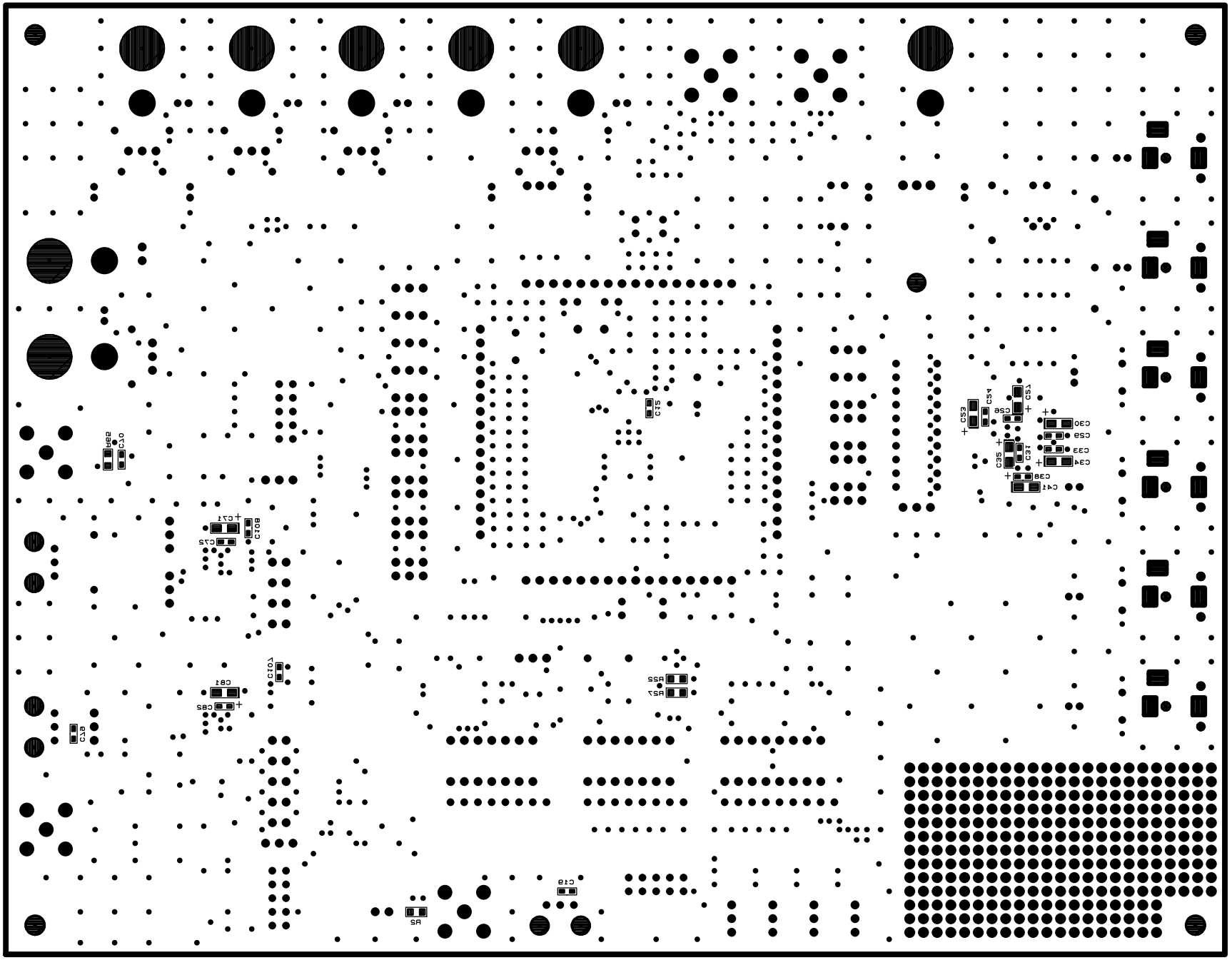
Size A2	Document Number S/PDIF OUTPUT	Rev 2
Date: Tuesday, November 13, 2007	Sheet 5 of 5	



AKD4141-A L1 SILK



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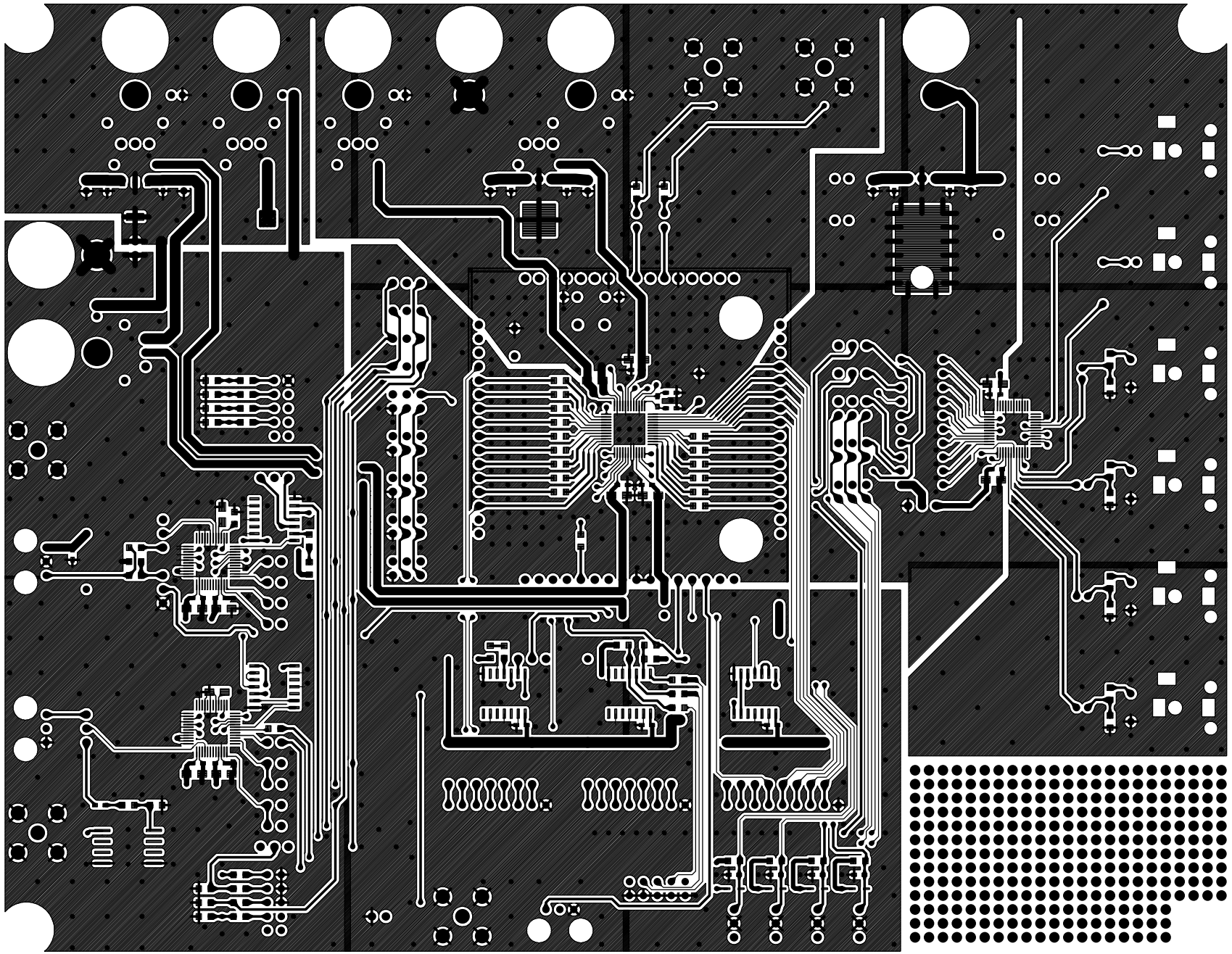

AKD4141-A L1

AKD4141-A LS