

8192MB DDR3L – SDRAM ECC DIMM

240 Pin unbuffered ECC DIMM

SLU08G72K1BD2SA-xxRT

8GByte in FBGA Technology

RoHS compliant

Options:

- Data Rate / Latency Marking
 DDR3 1333 MT/s CL9 -CC
 DDR3 1600 MT/s CL11 -DC

- Module Density
 8GByte with 18 dies and 2 ranks

- Standard Grade (T_A) 0°C to 70°C
(T_C) 0°C to 85°C
 E-Grade (T_A) 0°C to 85°C
(T_C) 0°C to 95°C *)
 W-Grade (T_A) -40°C to 85°C
(T_C) -40°C to 95°C *)

The refresh rate has to be doubled when 85°C < T_C < 95°C

Environmental Requirements:

- Operating temperature (ambient)
 Standard Grade 0°C to 70°C
 E-Grade 0°C to 85°C
 W-Grade -40°C to 85°C
- Operating Humidity
 10% to 90% relative humidity, noncondensing
- Operating Pressure
 105 to 69 kPa (up to 10000 ft.)
- Storage Temperature
 -55°C to 100°C
- Storage Humidity
 5% to 95% relative humidity, noncondensing
- Storage Pressure
 1682 PSI (up to 5000 ft.) at 50°C

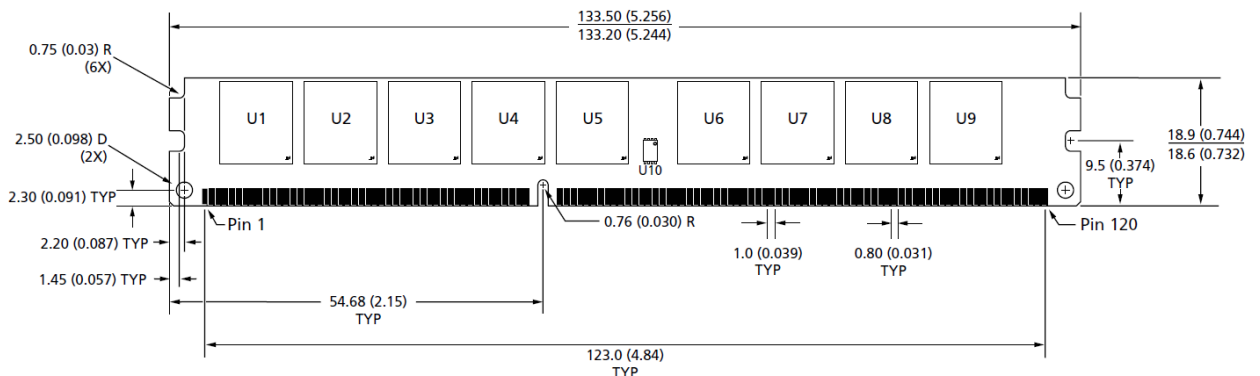
Features:

- 240-pin 72-bit DDR3 Dual-In-Line Double Data Rate Synchronous DRAM module with ECC
- Module organization: dual rank 1G x 72
- V_{DD} = 1.35V and 1.5V
- V_{DDQ} = 1.35V and 1.5V
- 1.5V I/O (SSTL_15 compatible)
- Supports ECC, error detection and correction
- On-board I²C temperature sensor with integrated serial presence-detect (SPD) EEPROM (according to JEDEC JESD21C)
- **Finish Process: OSP with 30µ" AU on contact fingers**
- This module is fully pin and functional compatible to the JEDEC PC3-12800 spec. and JEDEC- Standard MO-269. (see www.jedec.org)
- The pcb and all components are manufactured according to the RoHS compliance specification [EU Directive 2002/95/EC Restriction of Hazardous Substances (RoHS)]

- **DDR3L - SDRAM component Samsung K4B4G0846D**
- 512Mx8 DDR3 SDRAM in PG-TFBGA-78 package
- 8-bit pre-fetch architecture
- Programmable CAS Latency, CAS Write Latency, Additive Latency, Burst Length and Burst Type.
- On-Die-Termination (ODT) and Dynamic ODT for improved signal integrity.
- Refresh. Self Refresh and Power Down Modes.
- ZQ Calibration for output driver and ODT.
- System Level Timing Calibration Support via Write Leveling and Multi Purpose Register (MPR) Read Pattern.

Figure: mechanical dimensions¹

¹if no tolerances specified ± 0.15mm



This Swissbit module is an industry standard 240-pin 8-byte DDR3 SDRAM Dual-In-line Memory Module (UDIMM) which is organized as x72 high speed CMOS memory arrays. The module uses internally configured octal-bank DDR3 SDRAM devices. The module uses double data rate architecture to achieve high-speed operation. DDR3 SDRAM modules operate from a differential clock (CK and CK#). READ and WRITE accesses to a DDR3 SDRAM module is burst-oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. The burst length is either four or eight locations. An auto precharge function can be enabled to provide a self-timed row precharge that is initiated at the end of a burst access. The DDR3 SDRAM devices have a multibank architecture which allows a concurrent operation that is providing a high effective bandwidth. A self refresh mode is provided and a power-saving "power-down" mode. All inputs and all full drive-strength outputs are SSTL_15 compatible.

The module can operate either at DDR3 mode (1.50V VDD) or DDR3L mode (1.35V VDD)

The DDR3 SDRAM module uses the serial presence detect (SPD) function implemented via serial EEPROM using the standard I2C protocol. This nonvolatile storage device contains 256 bytes. The first 128 bytes are utilized by the DIMM manufacturer (Swissbit) to identify the module type, the module's organization and several timing parameters. The second 128 bytes are available to the end user.

Module Configuration

Organization	DDR3 SDRAMs used	Row Addr.	Device Bank Addr.	Column Addr.	Refresh	Module Bank Select
1G x 72bit	18 x 512M x 8bit (4Gbit)	16	BA0, BA1, BA2	10	8k	S0#, S1#

Module Dimensions

in mm

133.35 (long) x 18.75 (high) x 4.00 [max] (thickness)

Timing Parameters

Part Number	Module Density	Transfer Rate	Clock Cycle/Data bit rate	Latency
SLU08G72K1BD2SA-CCRT	8GByte	10.6 GB/s	1.5ns/1333MT/s	9-9-9
SLU08G72K1BD2SA-DCRT	8GByte	12.8 GB/s	1.25ns/1600MT/s	11-11-11

Pin Name

A0 – A9, A11 – A15	Address Inputs
A10/AP	Address Input / Autoprecharge Bit
A12/BC#	Address Input / Burst chop
BA0 – BA2	Bank Address Inputs
DQ0 – DQ63	Data Input / Output
CB0 – CB7	ECC check bits
DM0 – DM8	Input Data Mask
DQS0 – DQS8	Data Strobe, positive line
DQS0# - DQS8#	Data Strobe, negative line (only used when differential data strobe mode is enabled)
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
CKE0 – CKE1	Clock Enable
S0#, S1#	Chip Select
CK0 – CK1	Clock inputs, positive line

CK0# – CK1#	Clock inputs, negative line
Event#	Temperature event: The EVENT# pin is asserted by the temperature sensor when critical
V _{DD}	Supply Voltage (1.35V -0.067V/+0.1V and 1.5V ± 0.075V)
V _{REFDQ}	Reference voltage: DQ, DM (V _{DD} /2)
V _{REFCA}	Reference voltage: Control, command, and address (V _{DD} /2)
V _{SS}	Ground
V _{TT}	Termination voltage: Used for control, command, and address (V _{DD} /2).
V _{DDSPD}	Serial EEPROM Positive Power Supply
SCL	Serial Clock for Presence Detect
SDA	Serial Data Out for Presence Detect
SA0 – SA2	Presence Detect Address Inputs
ODT0, ODT1	On-Die Termination
NC	No Connection

Pin Configuration

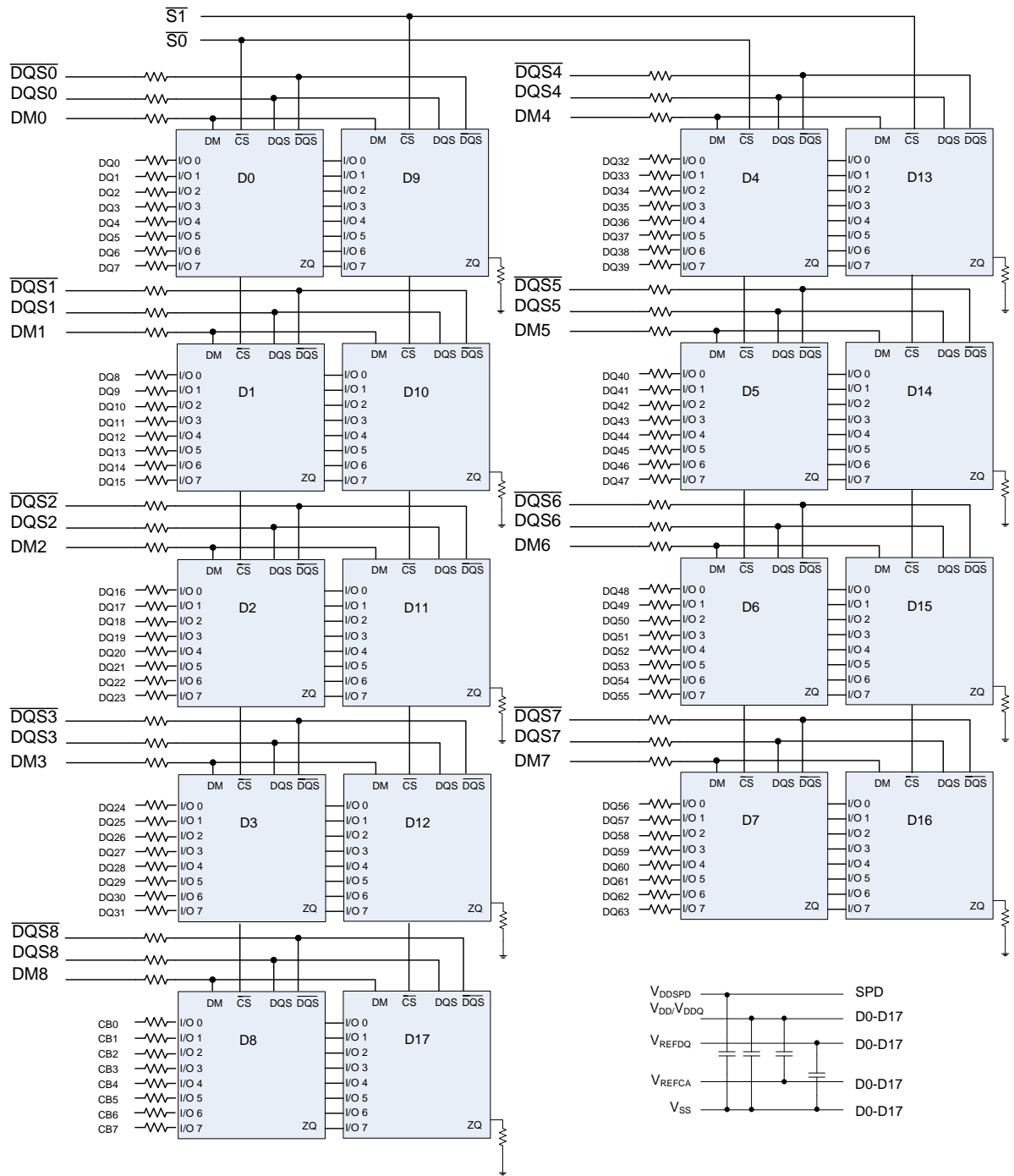
Frontside									
PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol	PIN	Symbol
1	V _{REFDQ}	27	DQ18	49	NC(V _{TT})	75	V _{DD}	101	V _{SS}
2	V _{SS}	28	DQ19	50	CKE0	76	S1#	102	DQS6#
3	DQ0	29	V _{SS}	51	V _{DD}	77	ODT1	103	DQS6
4	DQ1	30	DQ24	52	BA2	78	V _{DD}	104	V _{SS}
5	V _{SS}	31	DQ25	53	NC(Err_Out#)	79	NC(S2#)	105	DQ50
6	DQS0#	32	V _{SS}	54	V _{DD}	80	V _{SS}	106	DQ51
7	DQS0	33	DQS3#	55	A11	81	DQ32	107	V _{SS}
8	V _{SS}	34	DQS3	56	A7	82	DQ33	108	DQ56
9	DQ2	35	V _{SS}	57	V _{DD}	83	V _{SS}	109	DQ57
10	DQ3	36	DQ26	58	A5	84	DQS4#	110	V _{SS}
11	V _{SS}	37	DQ27	59	A4	85	DQS4	111	DQS7#
12	DQ8	38	V _{SS}	60	V _{DD}	86	V _{SS}	112	DQS7
13	DQ9	39	CB0	61	A2	87	DQ34	113	V _{SS}
14	V _{SS}	40	CB1	62	V _{DD}	88	DQ35	114	DQ58
15	DQS1#	41	V _{SS}	63	CK1	89	V _{SS}	115	DQ59
16	DQS1	42	DQS8#	64	CK1#	90	DQ40	116	V _{SS}
17	V _{SS}	43	DQS8	65	V _{DD}	91	DQ41	117	SA0
18	DQ10	44	V _{SS}	66	V _{DD}	92	V _{SS}	118	SCL
19	DQ11	45	CB2	67	V _{REFCA}	93	DQS5#	119	SA2
20	V _{SS}	46	CB3	68	NC(Par_In)	94	DQS5	120	V _{TT}
21	DQ16	47	V _{SS}	69	V _{DD}	95	V _{SS}		
22	DQ17	48	NC(V _{TT})	70	A10/ AP	96	DQ42		
23	V _{SS}			71	BA0	97	DQ43		
24	DQS2#			72	V _{DD}	98	V _{SS}		
25	DQS2			73	WE#	99	DQ48		
26	V _{SS}			74	CAS#	100	DQ49		

Signals in brackets (...) may be connected at the DIMM socket, but are not used on the DIMM

Backside									
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	V _{SS}	147	DQ23	169	CKE1	195	ODT0	221	DM6(DQS15)
122	DQ4	148	V _{SS}	170	V _{DD}	196	A13	222	NC(DQS15#)
123	DQ5	149	DQ28	171	A15)	197	V _{DD}	223	V _{SS}
124	V _{SS}	150	DQ29	172	A14	198	NC(S3#)	224	DQ54
125	DM0(DQS9)	151	V _{SS}	173	V _{DD}	199	V _{SS}	225	DQ55
126	NC(DQS9#)	152	DM3(DQS12)	174	A12, BC#	200	DQ36	226	V _{SS}
127	V _{SS}	153	NC(DQS12#)	175	A9	201	DQ37	227	DQ60
128	DQ6	154	V _{SS}	176	V _{DD}	202	V _{SS}	228	DQ61
129	DQ7	155	DQ30	177	A8	203	DM4(DQS13)	229	V _{SS}
130	V _{SS}	156	DQ31	178	A6	204	NC(DQS13#)	230	DM7(DQS16)
131	DQ12	157	V _{SS}	179	V _{DD}	205	V _{SS}	231	NC(DQS16#)
132	DQ13	158	CB4	180	A3	206	DQ38	232	V _{SS}
133	V _{SS}	159	CB5	181	A1	207	DQ39	233	DQ62
134	DM1(DQS10)	160	V _{SS}	182	V _{DD}	208	V _{SS}	234	DQ63
135	NC(DQS10#)	161	DM8(DQS17)	183	V _{DD}	209	DQ44	235	V _{SS}
136	V _{SS}	162	NC(DQS17#)	184	CK0	210	DQ45	236	V _{DDSPD}
137	DQ14	163	V _{SS}	185	CK0#	211	V _{SS}	237	SA1
138	DQ15	164	CB6	186	V _{DD}	212	DM5(DQS14)	238	SDA
139	V _{SS}	165	CB7	187	EVENT#	213	NC(DQS14#)	239	V _{SS}
140	DQ20	166	V _{SS}	188	A0	214	V _{SS}	240	V _{TT}
141	DQ21	167	NC(TEST)	189	V _{DD}	215	DQ46		
142	V _{SS}	168	RESET#	190	BA1	216	DQ47		
143	DM2(DQS11)			191	V _{DD}	217	V _{SS}		
144	NC(DQS11#)			192	RAS#	218	DQ52		
145	V _{SS}			193	S0#	219	DQ53		
146	DQ22			194	V _{DD}	220	V _{SS}		

Signals in brackets (...) may be connected at the DIMM socket, but are not used on the DIMM

FUNCTIONAL BLOCK DIAGRAM 8192MB DDR3 SDRAM DIMM, 2 RANKS AND 18 COMPONENTS



- BA0-BA2 → BA0-BA2: SDRAM D0-D17
- A0-A15 → A0-A15: SDRAM D0-D17
- RAS → RAS: SDRAM D0-D17
- CAS → CAS: SDRAM D0-D17
- WE → WE: SDRAM D0-D17
- ODT0 → ODT: SDRAM D0-D8
- ODT1 → ODT: SDRAM D9-D17
- CKE0 → CKE: SDRAM D0-D8
- CKE1 → CKE: SDRAM D9-D17
- CK0,CK1 → CK: SDRAM D0-D17
- CK0,CK1 → CK: SDRAM D0-D17
- RESET → RESET: SDRAM D0-D17

Notes:

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationship must be maintained as shown.
3. DQ, DM, DQS/DQS resistors: Refer to associated topology diagram.
4. Refer to the appropriate clock wiring topology under the DIMM wiring details section of the JEDEC document.
5. For each DRAM, a unique ZQ resistor is connected to GND. The ZQ resistor is 240Ω±1%.
6. Refer to associated figure for SPD details.

MAXIMUM ELECTRICAL DC CHARACTERISTICS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
V_{DD} Supply Voltage relative to V_{SS}	V_{DD}	-0.4	1.975	V
I/O V_{DD} Supply Voltage relative to V_{SS}	V_{DDQ}	-0.4	1.975	V
Voltage on any pin relative to V_{SS}	V_{IN}, V_{OUT}	-0.4	1.975	V
INPUT LEAKAGE CURRENT Any input $0V \leq V_{IN} \leq V_{DD}$, V_{REF} pin $0V \leq V_{IN} \leq 0.95V$ (All other pins not under test = 0V)	I_I			μA
Command/Address RAS#, CAS#, WE#, S#, CKE		-16	16	
CK, CK#		-16	16	
DM		-2	2	
OUTPUT LEAKAGE CURRENT (DQ's and ODT are disabled; $0V \leq V_{OUT} \leq V_{DDQ}$)	I_{OZ}	-5	5	μA
DQ, DQS, DQS#				
V_{REF} LEAKAGE CURRENT ; V_{REF} is on a valid level	I_{VREF}	-8	8	μA

DDR3L (1.35V) DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.283	1.35	1.450	V
I/O Supply Voltage	V_{DDQ}	1.283	1.35	1.450	V
I/O Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V
I/O Termination Voltage (system)	V_{TT}	$0.49 \times V_{DDQ} - 20mV$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ} + 20mV$	V
Input High (Logic 1) Voltage	$V_{IH(DC90)}$	$V_{REF} + 90mV$		$V_{DDQ} + 0.3$	V

DDR3 (1.50V) DC OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{DD}	1.425	1.5	1.575	V
I/O Supply Voltage	V_{DDQ}	1.425	1.5	1.575	V
I/O Reference Voltage	V_{REF}	$0.49 \times V_{DDQ}$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ}$	V
I/O Termination Voltage (system)	V_{TT}	$0.49 \times V_{DDQ} - 20mV$	$0.50 \times V_{DDQ}$	$0.51 \times V_{DDQ} + 20mV$	V
Input High (Logic 1) Voltage	$V_{IH(DC)}$	$V_{REF} + 0.1$		$V_{DDQ} + 0.3$	V
Input Low (Logic 0) Voltage	$V_{IL(DC)}$	-0.3		$V_{REF} - 0.1$	V

AC INPUT OPERATING CONDITIONS

PARAMETER/ CONDITION	SYMBOL	MIN	MAX	UNITS
Input High (Logic 1) Voltage	$V_{IH(AC)}$	$V_{REF} + 0.175$	-	V
Input Low (Logic 0) Voltage	$V_{IL(AC)}$	-	$V_{REF} - 0.175$	V

CAPACITANCE

At DDR3 data rates, it is recommended to simulate the performance of the module to achieve optimum values. When inductance and delay parameters associated with trace lengths are used in simulations, they are significantly more accurate and realistic than a gross estimation of module capacitance. Simulations can then render a considerably more accurate result. JEDEC modules are now designed by using simulations to close timing budgets.

I_{DD} Specifications and Conditions

(0°C ≤ T_{CASE} ≤ + 85°C°, V_{DDQ} = +1.35V, V_{DD} = +1.35V)

Parameter & Test Condition	Symbol	max.		Unit
		12800 CL11	10600 CL9	
OPERATING CURRENT *) : One device bank Active-Precharge; t _{RC} = t _{RC} (I _{DD}); t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; DQ inputs changing once per clock cycle; Address and control inputs changing once every two clock cycles	I _{DD0}	324	315	mA
OPERATING CURRENT *) : One device bank; Active-Read-Precharge; I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RC} = t _{RC} (I _{DD}), t _{RAS} = t _{RAS} MIN (I _{DD}), t _{RCD} = t _{RCD} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address inputs changing once every two clock cycles; Data Pattern is same as I _{DD4W}	I _{DD1}	414	396	mA
PRECHARGE POWER-DOWN CURRENT: All device banks idle; Power-down mode; t _{CK} = t _{CK} (I _{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V _{REF}	Fast Exit I _{DD2P}	144	144	mA
	Slow Exit	144	144	
PRECHARGE QUIET STANDBY CURRENT: All device banks idle; t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH; All Control and Address bus inputs are not changing; DQ's are floating at V _{REF}	I _{DD2Q}	180	180	mA
PRECHARGE STANDBY CURRENT: All device banks idle; t _{CK} = t _{CK} (I _{DD}); CKE is HIGH, CS# is HIGH; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD2N}	198	198	mA
ACTIVE POWER-DOWN CURRENT: All device banks open; t _{CK} = t _{CK} (I _{DD}); CKE is LOW; All Control and Address bus inputs are not changing; DQ's are floating at V _{REF} (always fast exit)	I _{DD3P}	198	198	mA
ACTIVE STANDBY CURRENT: All device banks open; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD3N}	378	360	mA
OPERATING READ CURRENT: All device banks open, Continuous burst reads; One module rank active; I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD4R}	684	603	mA

Parameter & Test Condition	Symbol	max.		Unit
		12800 CL11	10600 CL9	
OPERATING WRITE CURRENT: All device banks open, Continuous burst writes; One module rank active; BL = 4, CL = CL (I _{DD}), AL = 0; t _{CK} = t _{CK} (I _{DD}), t _{RAS} = t _{RAS} MAX (I _{DD}), t _{RP} = t _{RP} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD4W}	684	603	mA
BURST REFRESH CURRENT: t _{CK} = t _{CK} (I _{DD}); refresh command at every t _{RFC} (I _{DD}) interval, CKE is HIGH, CS# is HIGH between valid commands; All other Control and Address bus inputs are changing once every two clock cycles; DQ inputs changing once per clock cycle	I _{DD5}	1782	1782	mA
SELF REFRESH CURRENT: CK and CK# at 0V; CKE ≤ 0.2V; All other Control and Address bus inputs are floating at V _{REF} ; DQ's are floating at V _{REF}	I _{DD6}	216	216	mA
OPERATING CURRENT*) : Four device bank interleaving READs, I _{OUT} = 0mA; BL = 4, CL = CL (I _{DD}), AL = t _{RCD} (I _{DD}) - 1 x t _{CK} (I _{DD}); t _{CK} = t _{CK} (I _{DD}), t _{RC} = t _{RC} (I _{DD}), t _{RRD} = t _{RRD} (I _{DD}), t _{RCD} = t _{RCD} (I _{DD}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are not changing during DESELECT; DQ inputs changing once per clock cycle	I _{DD7}	1206	1179	mA

*) Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

TIMING VALUES USED FOR I_{DD} MEASUREMENT

I _{DD} MEASUREMENT CONDITIONS			
SYMBOL	12800 CL11	10600 CL9	Unit
CL (I _{DD})	11	9	t _{CK}
t _{RCD} (I _{DD})	13.75	13.5	ns
t _{RC} (I _{DD})	48.75	49.5	ns
t _{RRD} (I _{DD})	6.25	6	ns
t _{CK} (I _{DD})	1.25	1.5	ns
t _{RAS} MIN (I _{DD})	35	36	ns
t _{RAS} MAX (I _{DD})	70'200	70'200	ns
t _{RP} (I _{DD})	13.75	13.5	ns
t _{RFC} (I _{DD})	260	260	t _{CK}

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS		12800 CL11		10600 CL9			
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	Unit	
Clock cycle time	CL = 11	t _{CK} (11)	1.25	1.5	-	-	ns
	CL = 10	t _{CK} (10)	1.5	<1.875	1.5	<1.875	ns
	CL = 9	t _{CK} (9)	1.5	<1.875	1.5	<1.875	ns
	CL = 8	t _{CK} (8)	1.875	<2.5	1.875	<2.5	ns
	CL = 7	t _{CK} (7)	1.875	<2.5	1.875	<2.5	ns
	CL = 6	t _{CK} (6)	2.5	3.3	2.5	3.3	ns
	CL = 5	t _{CK} (5)	3.0	3.3	3.0	3.3	ns
Read CMD to 1 st data	t _{AA}	13.75	-	13.5	-	ns	
CK high-level width	t _{CH} (avg)	0.47	0.53	0.47	0.53	t _{CK}	
CK low-level width	t _{CL} (avg)	0.47	0.53	0.47	0.53	t _{CK}	
Data-out high-impedance window from CK/CK#	t _{HZ}	-	225	-	250	ps	
Data-out low-impedance window from CK/CK#	t _{LZ}	-450	225	-500	250	ps	
DQ and DM input pulse width (for each input)	t _{DIPW}	360	-	400	-	ps	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	t _{QH}	0.38	-	0.38	-	t _{CK} (AVG)	
DQS input high pulse width	t _{DQSH}	0.45	0.55	0.45	0.55	t _{CK}	
DQS input low pulse width	t _{DQSL}	0.45	0.55	0.45	0.55	t _{CK}	
DQS read preamble	t _{RPRE}	0.9	Note ¹	0.9	Note ¹	t _{CK}	
DQS read postamble	t _{RPST}	0.3	Note ²	0.3	Note ²	t _{CK}	
DQS write preamble	t _{WPRE}	0.9	-	0.9	-	t _{CK}	
DQS write postamble	t _{WPST}	0.3	-	0.3	-	t _{CK}	

¹ The maximum preamble is bound by t_{LZDQS} (MAX)

² The maximum postamble is bound by t_{HZDQS} (MAX)

The DQ, DQS setup and hold times as well as Command/Address setup and hold times need to be calculated using the respective component data sheets with derating tables and the driver slew rate in combination with the JEDEC min/max routing information

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)
 $(0^{\circ}\text{C} \leq T_{\text{CASE}} \leq +85^{\circ}\text{C}; V_{\text{DDQ}} = +1.5\text{V} \pm 0.075\text{V}, V_{\text{DD}} = +1.5\text{V} \pm 0.075\text{V})$

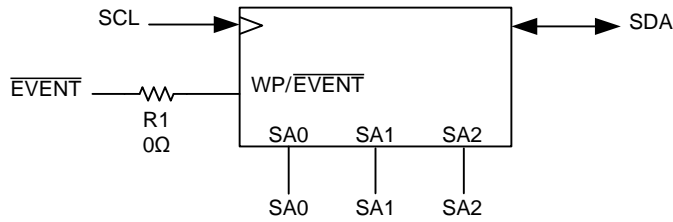
AC CHARACTERISTICS		12800 CL11		10600 CL9		Unit
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	
CAS# to CAS# command delay	t_{CCD}	4	-	4	-	t_{CK}
ACTIVE to ACTIVE (same bank) command period	t_{RC}	48.75	-	49.5	-	ns
ACTIVE bank <i>a</i> to ACTIVE bank <i>b</i> command	t_{RRD}	max 4nCK,6ns	-	max 4nCK,6ns	-	ns
ACTIVE to READ or WRITE delay	t_{RCD}	13.75	-	13.5	-	ns
Four bank Activate period	t_{FAW}	1K Page size	30	-	30	ns
		2K Page size	40	-	45	
ACTIVE to PRECHARGE command	t_{RAS}	35	70'200	36	70'200	ns
Internal READ to precharge command delay	t_{RTP}	max 4nCK,7.5ns	-	max 4nCK,7.5ns	-	ns
Write recovery time	t_{WR}	15	-	15	-	ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{\text{WR}} + t_{\text{RP}}/t_{\text{CK}}$	-	$t_{\text{WR}} + t_{\text{RP}}/t_{\text{CK}}$	-	ns
Internal WRITE to READ command delay	t_{WTR}	max 4nCK,7.5ns	-	max 4nCK,7.5ns	-	ns
PRECHARGE command period	t_{RP}	13.75	-	13.5	-	ns
LOAD MODE command cycle time	t_{MRD}	4	-	4	-	t_{CK}
REFRESH to ACTIVE or REFRESH to REFRESH command interval	t_{RFC}	260	70'200	260	70'200	ns
Average periodic refresh interval	t_{REFI}	0 °C ≤ T _{CASE} ≤ 85 °C	-	7.8	-	7.8
		85 °C < T _{CASE} ≤ 95 °C	-	3.9	-	3.9
RTT turn-on from ODTL on reference	t_{AON}	-225	225	-250	250	ps
RTT turn-on from ODTL off reference	t_{AOF}	0.3	0.7	0.3	0.7	t_{CK}
Asynchronous RTT turn-on delay (power Down with DLL off)	t_{AONPD}	2	8,5	2	8,5	ns
Asynchronous RTT turn-off delay (power Down with DLL off)	t_{AOFPD}	2	8,5	2	8,5	ns
RTT dynamic change skew	t_{ADC}	0.3	0.7	0.3	0.7	t_{CK}
First DQS, DQS# rising edge	t_{WLMRD}	40	-	40	-	t_{CK}
DQS, DQS# delay	t_{WLDQSEN}	25	-	25	-	t_{CK}

DDR3 SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

(0°C ≤ T_{CASE} ≤ + 85°C; V_{DDQ} = +1.5V ± 0.075V, V_{DD} = +1.5V ± 0.075V)

AC CHARACTERISTICS		12800 CL11		10600 CL9		Unit
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	
Exit reset from CKE HIGH to a valid command	t _{XPR}	max 5nCK, t _{REC} + 10ns	-	max 5nCK, t _{REC} + 10ns	-	t _{CK}
Begin power supply ramp to power supplies stable	t _{VDDPR}	-	200	-	200	ms
RESET# LOW to power supplies stable	t _{RPS}	0	200	-	200	ms
RESET# LOW to I/O and RTT High-Z	t _{IOz}	-	20	-	20	ns
Exit precharge power-down to any non-READ command	t _{XP}	max 3nCK,6ns	-	max 3nCK,6ns	-	t _{CK}
CKE minimum high/low time	t _{CKE}	max 3nCK, 5ns	-	max 3nCK, 5.625ns	-	t _{CK}

Temperature Sensor with Serial Presence-Detect EEPROM



Temperature Sensor with Serial Presence-Detect EEPROM Operating Conditions

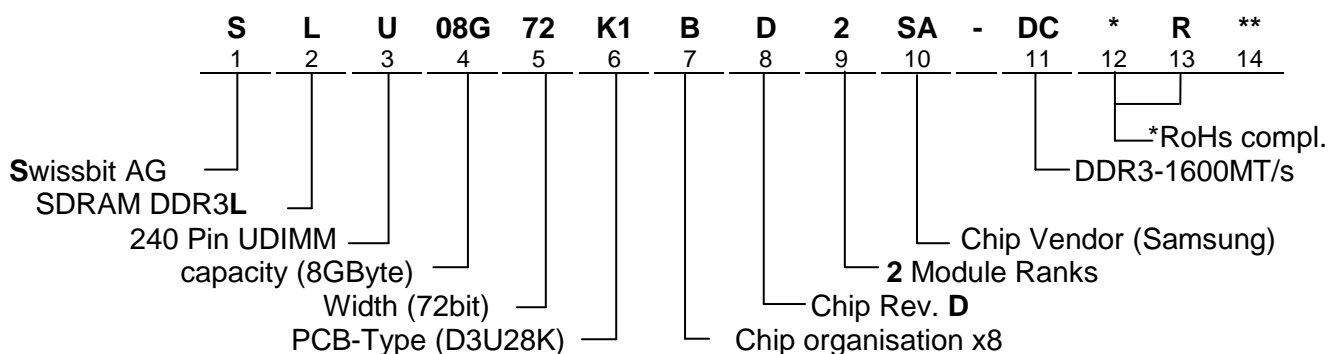
Parameter / Condition	Symbol	MIN	MAX	Unit
Supply voltage	V _{DDSPD}	+3	+3.6	V
Supply current: V _{DD} = 3.3V	I _{DD}		+2.0	mA
Input high voltage: Logic 1; SCL, SDA	V _{IH}	+1.45	V _{DDSPD} +1	V
Input low voltage: Logic 0; SCL, SDA	V _{IL}	-	550	mV
Output low voltage: I _{OUT} = 2.1mA	V _{OL}	-	400	mV
Input current	I _{IN}	-5.0	5.0	µA
Temperature sensing range		T.B.D	T.B.D	°C
Temperature sensor accuracy		T.B.D	T.B.D	°C

SERIAL PRESENCE-DETECT MATRIX

Byte	Byte Description	12800 CL11	10600 CL9
0	CRC RANGE, EEPROM BYTES, BYTES USED	0x92	
1	SPD REVISION	0x12	
2	DRAM DEVICE TYPE	0x0B	
3	MODULE TYPE (FORM FACTOR)	0x02	
4	SDRAM DEVICE DENSITY & BANKS	0x04	
5	SDRAM DEVICE ROW & COLUMN COUNT	0x21	
6	BYTE 6 RESERVED	0x02	
7	MODULE RANKS & DEVICE DQ COUNT	0x09	
8	ECC TAG & MODULE MEMORY BUS WIDTH	0x0B	
9	FINE TIMEBASE DIVIDEND/DIVISOR	0x11	
10	MEDIUM TIMEBASE DIVIDEND	0x01	
11	MEDIUM TIMEBASE DIVISOR	0x08	
12	MIN SDRAM CYCLE TIME ($t_{CK\ MIN}$)	0x0A	0x0C
13	BYTE 13 RESERVED	0x00	
14	CAS LATENCIES SUPPORTED (CL4 => CL11)	0xFE	0x3E
15	CAS LATENCIES SUPPORTED (CL12 => CL18)	0x00	
16	MIN CAS LATENCY TIME ($t_{AA\ MIN}$)	0x69	
17	MIN WRITE RECOVERY TIME ($t_{WR\ MIN}$)	0x78	
18	MIN RAS# TO CAS# DELAY ($t_{RCD\ MIN}$)	0x69	
19	MIN ROW ACTIVE TO ROW ACTIVE DELAY ($t_{RRD\ MIN}$)	0x30	
20	MIN ROW PRECHARGE DELAY ($t_{RP\ MIN}$)	0x69	
21	UPPER NIBBLE FOR t_{RAS} & t_{RC}	0x11	
22	MIN ACTIVE TO PRECHARGE DELAY ($t_{RAS\ MIN}$)	0x18	0x20
23	MIN ACTIVE TO ACTIVE/REFRESH DELAY ($t_{RC\ MIN}$)	0x81	0x89
24	MIN REFRESH RECOVERY DELAY ($t_{RFC\ MIN}$) LSB	0x20	
25	MIN REFRESH RECOVERY DELAY ($t_{RFC\ MIN}$) MSB	0x08	
26	MIN INTERNAL WRITE TO READ CMD DELAY ($t_{WTR\ MIN}$)	0x3C	
27	MIN INTERNAL READ TO PRECHARGE CMD DELAY ($t_{RTP\ MIN}$)	0x3C	
28	MIN FOUR ACTIVE WINDOW DELAY ($t_{FAW\ MIN}$) MSB	0x00	
29	MIN FOUR ACTIVE WINDOW DELAY ($t_{FAW\ MIN}$) LSB	0xF0	
30	SDRAM DEVICE OUTPUT DRIVERS SUPPORTED	0x83	
31	SDRAM DEVICE THERMAL & REFRESH OPTIONS	0x01	

Byte	Byte Description	12800 CL11	10600 CL9
32	DDR3-MODULE THERMAL SENSOR	0x80	
33-59	BYTES 32-59 RESERVED	0x00	
60	MODULE HEIGHT (NOMINAL)	0x03	
61	MODULE THICKNESS (MAX)	0x11	
62	REFERENCE RAW CARD ID (RC K1)	0x09	
63	ADDRESS MAPPING EDGE CONECTOR TO DRAM	0x01	
64-116	BYTES 64-116 RESEVED	0x00	
117	MODULE MFR ID (LSB)	0x83	
118	MODULE MFR ID (MSB)	0xDA	
119	MODULE MFR LOCATION ID	0x01 (Switzerland) 0x02 (Germany) 0x03 (USA)	
120	MODULE MFR YEAR	X	
121	MODULE MFR WEEK	X	
122-125	MODULE SERIAL NUMBER	X	
126-127	CRC	0xD1FB	0xE524
128-145	MODULE PART NUMBER	"SLU08G72K1BD2SA-xx"	
146	MODULE DIE REV	X	
147	MODULE PCB REV	X	
148	DRAM DEVICE MFR ID (LSB)	0x80	
149	DRAM DEVICE MFR (MSB)	0xCE	
150-175	MFR RESERVED BYTES 150-175	0xFF	
176-255	CUSTOMER RESERVED BYTES 176-255	0xFF	

Part Number Code



* optional / additional information

** Thermal Sensor

Revision History		
Revision	Changes	Date
1.0	First release	17.02.2014

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CE Declaration of Conformity

We

Manufacturer: Swissbit AG
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declare under our sole responsibility that the product

Product Type: 8GB DDR3L ECC UDIMM
Brand Name: SWISSMEMORY™
Product Series: DDR3L UDIMM
Part Number: SLU08G72K1BD2SA-xxxRT

to which this declaration relates is in conformity with the following directives:

2002/96/EC Category 3 (WEEE)

following the provisions of Directive

Restriction of the use of certain hazardous substances 2011/65/EU

Swissbit AG, February 2014



Manuela Kögel
Head of Quality Management