

ESD PROTECTION DEVICE

STAND-OFF VOLTAGE – **12.0** Volts POWER DISSIPATION – **500**WATTS

GENERAL DESCRIPTION

The L50ESDL12VH4-2 has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltages caused by ESD (electrostatic discharge), EFT (electrical fast transients), and lightning.

FEATURES

- Protects two I/O lines
- Max. peak pulse power : Ppp = 500W at tp = 8/20 us.
- Low Capacitance : 8pF Typical
- Low clamping voltage
- IEC 61000-4-2, level 4 (ESD), > ±15KV (air); > ±8KV (contact).
- IEC 61000-4-5 (Lightning) 0.5kV, 12A (8/20µs)

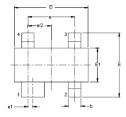
APPLICATION

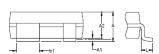
- ADSL
- Industrial Electronics
- RS-422 Interfaces
- Portable Electronics
- Microcontroller Input Protection
- WAN/LAN Equipment

MECHANICAL DATA

- Case Material: "Green" molding compound UL flammability classification 94V-0 (No Br.Sb, Cl)
- Terminals: Lead Free Plating (Matte Tin Finish), solderable per J-STD-002 and JESD22-B/02.
- Moisture Sensitivity: Leve 1 per J-STD-020C
- Component in accordance to RoHs 2002/95/EC

SOT-143







SOT-143						
DIM.	MIN.	MAX.				
Α	0.80	1.22				
A1	0.013	0.15				
A2	0.75	1.07				
b	0.30	0.51				
b1	0.76	0.94				
D	2.80	3.04				
Е	2.10	2.64				
E1	1.20	1.4				
е	1.92 BSC					
e1	0.20 BSC					
L	0.40	0.60				
All Dimensions in millimeter						

PIN A SSIGNMENT			
1	Ground		
2, 3	Input Line		
4	Vcc		



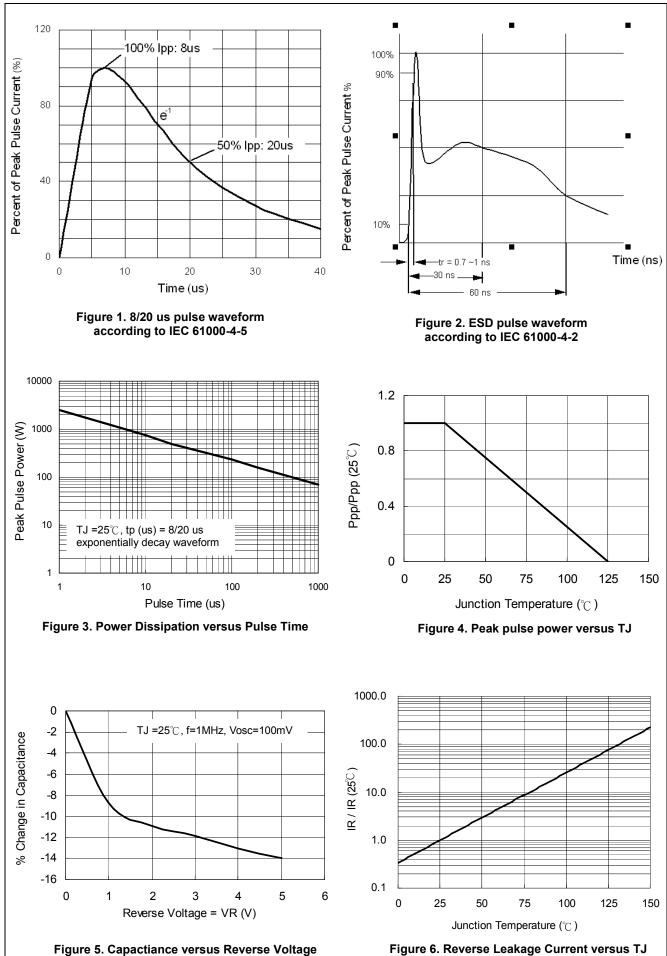
MAXIMUM RATINGS (Tj= 25℃ unless otherwise noticed)

Rating		Value	Unit
Peak Pulse Power (tp = 8/20us)	Ppk	500 (Max)	W
Peak Pulse Current (tp = 8/20us)	Ipp	16	Α
Operating Junction Temperature Range	TJ	-55 to + 125	$^{\circ}\mathbb{C}$
Storage Temperature Range Tstg		-55 to + 150	$^{\circ}\!\mathbb{C}$
Soldering Temperature, t max = 10s	TL	260	$^{\circ}\mathbb{C}$

ELECTRICAL CHARACTERISTICS (Tj= 25°C unless otherwise noticed)

Parameter	Symbol	Conditions	MIn	Тур	Max	Unit
Reverse standoff voltage	V_{RWM}				12	V
Breakdown voltage	VBR	IR = 1 mA	13.3			V
Reverse leakage current	IRM	V _{DRM} =12V			1	uA
Clamping Voltage		I_{PP} = 5A, tp = 8/20µs			24	V
	V _C	I_{PP} =16A, tp = 8/20 μ s			31	
Junction Capacitance	_	Between I/O pins and Ground $V_R = 0V$, $f = 1MHz$		8	10	- pF
	C _J	Between I/O pins $V_R = 0V, f = 1MHz$		4	5	
				REV. 1	, Oct-2010	, KSIR31







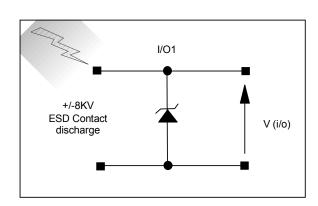


Figure 7. ESD Test Configuration

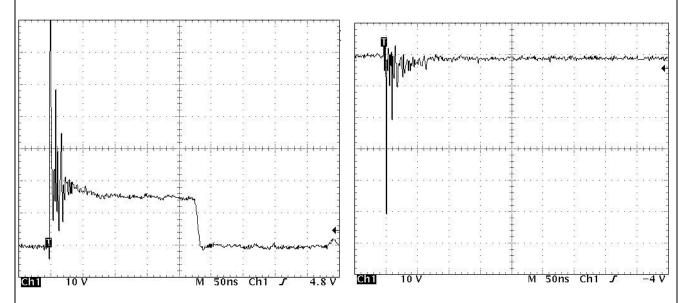


Figure 8. Clamped +8 kV ESD voltage waveform

Figure 9. Clamped -8 kV ESD voltage waveform



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