

CXDM4060N

**SURFACE MOUNT SILICON
N-CHANNEL
ENHANCEMENT-MODE
MOSFET**

**SOT-89 CASE****APPLICATIONS:**

- Load/Power switches
- Power supply converter circuits
- Battery powered portable equipment

MAXIMUM RATINGS: ($T_A=25^\circ\text{C}$)

	SYMBOL		UNITS
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	20	V
Continuous Drain Current (Steady State)	I_D	6.0	A
Maximum Pulsed Drain Current, $t_p=10\mu\text{s}$	I_{DM}	20	A
Power Dissipation	P_D	1.2	W
Operating and Storage Junction Temperature	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Thermal Resistance	Θ_{JA}	104	$^\circ\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS: ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I_{GSSF}, I_{GSSR}	$V_{GS}=20\text{V}, V_{DS}=0$			100	nA
I_{DSS}	$V_{DS}=32\text{V}, V_{GS}=0$			1.0	μA
BV_{DSS}	$V_{GS}=0, I_D=250\mu\text{A}$	40			V
$V_{GS(\text{th})}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	1.0	1.7	3.0	V
V_{SD}	$V_{GS}=0, I_S=1.0\text{A}$			1.0	V
$r_{DS(\text{ON})}$	$V_{GS}=10\text{V}, I_D=6.0\text{A}$		20	31	$\text{m}\Omega$
$r_{DS(\text{ON})}$	$V_{GS}=4.5\text{V}, I_D=5.0\text{A}$		30	45	$\text{m}\Omega$
$Q_{g(\text{tot})}$	$V_{DS}=20\text{V}, V_{GS}=10\text{V}, I_D=6.0\text{A}$		12		nC
Q_{gs}	$V_{DS}=20\text{V}, V_{GS}=10\text{V}, I_D=6.0\text{A}$		2.0		nC
Q_{gd}	$V_{DS}=20\text{V}, V_{GS}=10\text{V}, I_D=6.0\text{A}$		2.2		nC
C_{rss}	$V_{DS}=20\text{V}, V_{GS}=0, f=1.0\text{MHz}$		64		pF
C_{iss}	$V_{DS}=20\text{V}, V_{GS}=0, f=1.0\text{MHz}$		730		pF
C_{oss}	$V_{DS}=20\text{V}, V_{GS}=0, f=1.0\text{MHz}$		58		pF
t_{on}	$ V_{DS}=20\text{V}, V_{GS}=10\text{V}, I_D=1.0\text{A} $		27		ns
t_{off}	$ R_G=3.0\Omega, R_L=3.3\Omega $		33		ns


www.centralsemi.com
DESCRIPTION:

The CENTRAL SEMICONDUCTOR CXDM4060N is a high current silicon N-Channel enhancement-mode MOSFET, designed for high speed pulsed amplifier and driver applications. This MOSFET offers high current, low $r_{DS(\text{ON})}$, low threshold voltage, and low leakage current.

MARKING: FULL PART NUMBER**FEATURES:**

- Low $r_{DS(\text{ON})}$ (20m Ω TYP @ $V_{GS}=10\text{V}$)
- High current ($I_D=6.0\text{A}$)
- Logic level compatibility

SYMBOL		UNITS
V_{DS}	40	V
V_{GS}	20	V
I_D	6.0	A
I_{DM}	20	A
P_D	1.2	W
T_J, T_{stg}	-55 to +150	$^\circ\text{C}$
Θ_{JA}	104	$^\circ\text{C}/\text{W}$

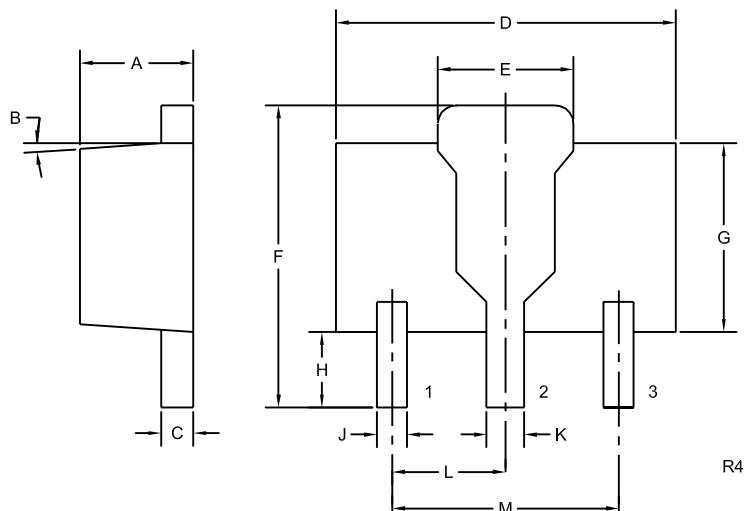
R2 (1-April 2013)

CXDM4060N

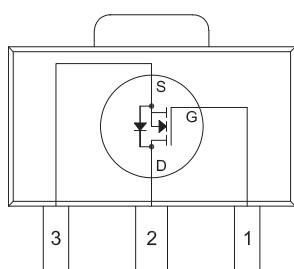
SURFACE MOUNT SILICON
N-CHANNEL
ENHANCEMENT-MODE
MOSFET



SOT-89 CASE - MECHANICAL OUTLINE



PIN CONFIGURATION



(Top View)
Tab is common to pin 2

LEAD CODE:

- 1) Gate
- 2) Drain
- 3) Source

MARKING: FULL PART NUMBER

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.067	1.40	1.70
B	4°		4°	
C	0.014	0.018	0.35	0.46
D	0.173	0.185	4.40	4.70
E	0.064	0.074	1.62	1.87
F	0.146	0.177	3.70	4.50
G	0.090	0.106	2.29	2.70
H	0.028	0.051	0.70	1.30
J	0.014	0.019	0.36	0.48
K	0.017	0.023	0.44	0.58
L	0.059		1.50	
M	0.118		3.00	

SOT-89 (REV: R4)

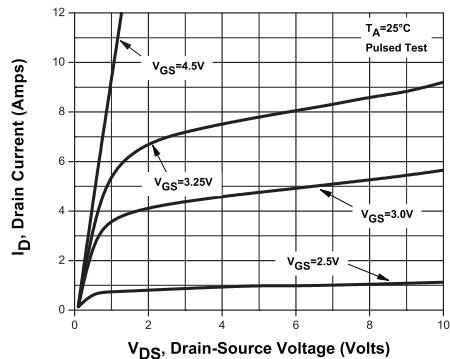
CXDM4060N

**SURFACE MOUNT SILICON
N-CHANNEL
ENHANCEMENT-MODE
MOSFET**

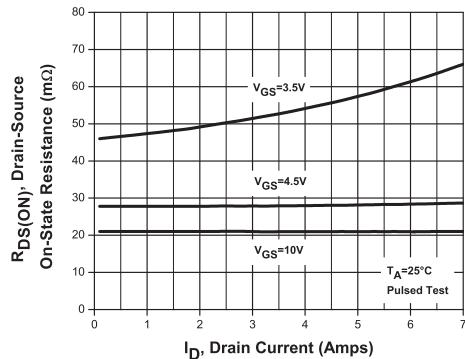


TYPICAL ELECTRICAL CHARACTERISTICS

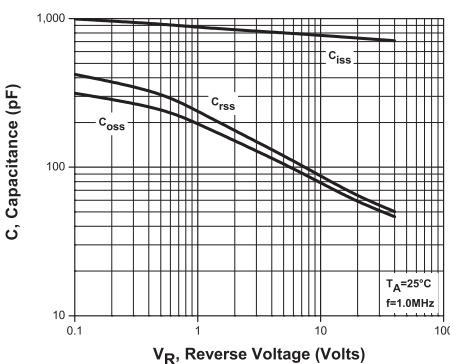
Output Characteristics



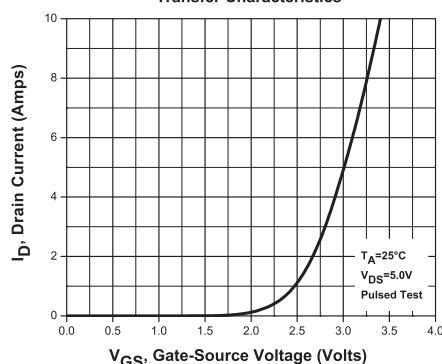
Drain Source On Resistance



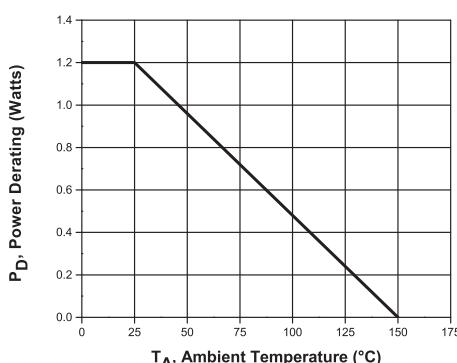
Capacitance



Transfer Characteristics



Power Derating



R2 (1-April 2013)