RDA5807P

SINGLE-CHIP BROADCAST FM RADIO TUNER

Rev.1.0–Aug.2008

1 General Description

The RDA5807P is a single-chip broadcast FM stereo radio tuner with fully integrated synthesizer, IF selectivity and MPX decoder. The tuner uses the CMOS process, support multi-interface and require the least external component. The package size is 4X4mm^2 and is completely adjustment-free. All these make it very suitable for portable devices.

The RDA5807P has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions.

The RDA5807P can be tuned to the worldwide frequency band.

The RDA5807P is pin-to-pin compatible to RDA5800,RDA5800C and RDA5802.

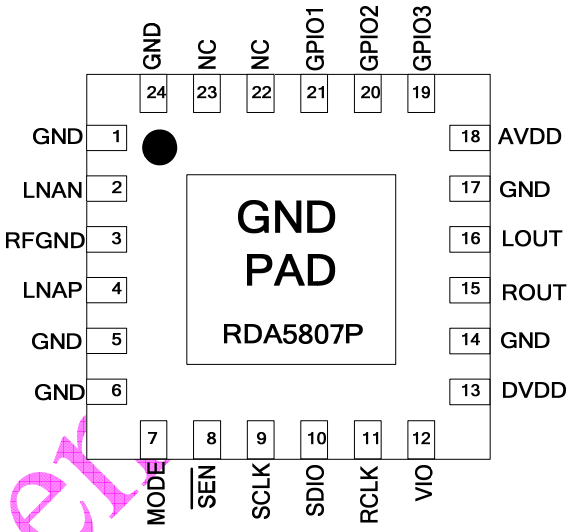


Figure 1-1. RDA5807P Top View

1.1 Features

- CMOS single-chip fully-integrated FM tuner
- Low power consumption
  - Total current consumption lower than 17.5mA at 3.3V power supply
- Support worldwide frequency band
  - 76 -108 MHz
- Digital low-IF tuner
  - Image-reject down-converter
  - High performance A/D converter
  - IF selectivity performed internally
- Fully integrated digital frequency synthesizer
  - Fully integrated on-chip RF and IF VCO
  - Fully integrated on-chip loop filter
- Autonomous search tuning
- Support crystal oscillator
- 32.768 KHz 12M,24M,13M,26M,19.2M,38.4MHz Reference clock
- 2-wire and 3-wire serial control bus interface
- Digital auto gain control (AGC)
  - Mono/stereo switch
  - Soft mute
  - High cut
- Signal dependent mono to stereo blend [Stereo Noise Cancelling (SNC)]
- Adjustment-free stereo decoder
- Autonomous search tuning function
- Bass boost
- Standby mode
- Programmable de-emphasis (50/75 μs)
- Directly support 32Ω resistance loading
- Integrated LDO regulator
  - 2.7 to 5.5 V operation voltage
- 4X4mm 24 pin QFN package

1.2 Applications

- Cellular handsets
- MP3, MP4 players
- Portable radios
- PDAs, Notebook PCs

2 Table of Contents

3 Functional Description

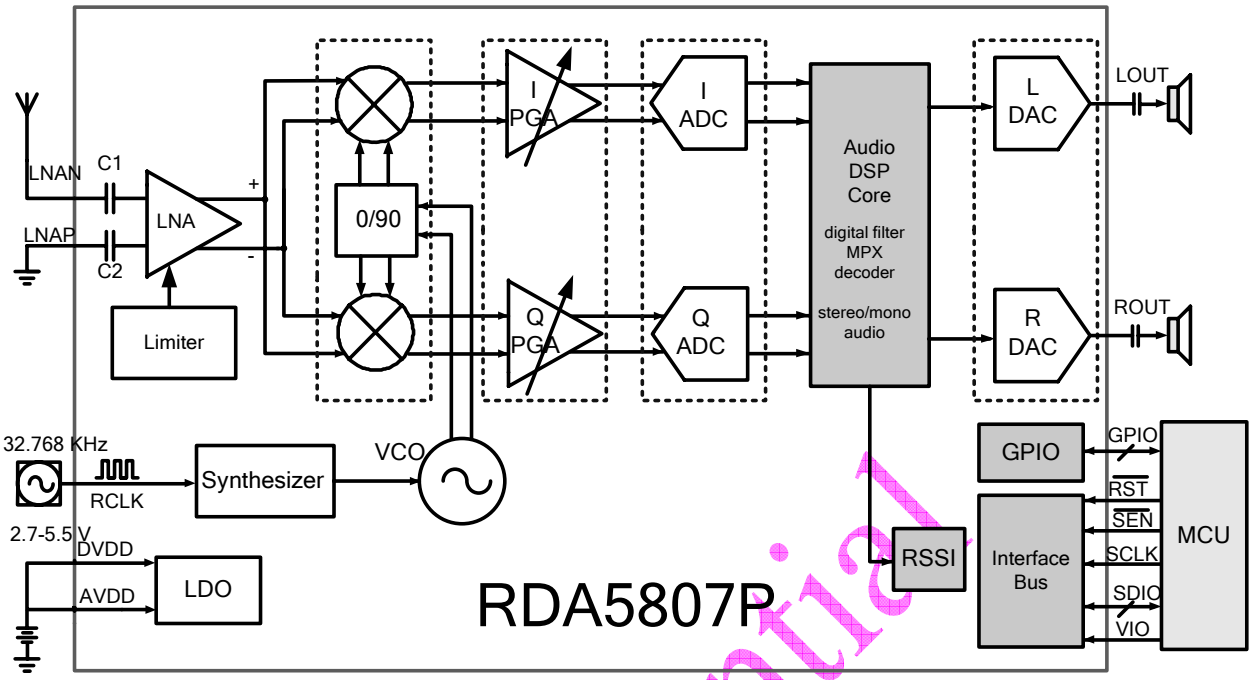


Figure 3-1. RDA5807P FM Tuner Block Diagram

3.1 FM Receiver

The receiver uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduces complexity, and integrates a low noise amplifier (LNA) supporting the FM broadcast band (76 to 108MHz), a quadrature image-reject mixer, a programmable gain control (PGA), a high resolution analog-to-digital converters (ADCs), an audio DSP and a high-fidelity digital-to-analog converters (DACs).

The LNA has differential input ports (LNAP and LNAN). The LNA default input resistance is 150 Ohm under single or dual input mode. It default input common mode voltage is GND.

The limiter prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

The quadrature mixer down converts the LNA output differential RF signal to low-IF, it also has image-reject function.

The PGA amplifies the mixer output IF signal and then digitized with ADCs.

The DSP core finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

The DACs convert digital audio signal to analog and change the volume at same time. The DACs has low-pass feature and -3dB frequency is about 30 KHz.

3.2 Synthesizer

The frequency synthesizer generates the local oscillator signal which divide to quadrature, then be used to down convert the RF input to a constant low intermediate frequency (IF). The synthesizer reference clock is 32.768 KHz,12M, 24M, 13M, 26M, 19.2M, 38.4MHz. select by **CLK MODE[2:0] BIT.**

3.3 Power Supply

The RDA5807P integrated one LDO which supplies power to the chip. The external supply voltage range is 2.7-5.5 V.

3.4 RESET and Control Interface select

The RDA5807P is RESET itself When VIO is Power up. And also support soft reset. The control interface is select by MODE Pin. The MODE Pin is low ,I2C Interface is select. The MODE Pin is set to VIO, SPI Interface is select.

The RDA5807P could enter into a power-down mode to reduce power consumption.
In power-down mode, analog and digital circuitry are both disabled, while maintaining register configuration and keeping control interface active.
Details refer to *RDA5807P Programming Guide*.

3.5 Control Interface

The RDA5807P supports I^2C control interface. User could program the chip through the bus.

The I^2C interface is compliant to I^2C Bus Specification 2.1. It includes two pins: SCLK and SDIO. An I^2C interface transfer begins with START condition, a command byte and data bytes, each byte has a followed ACK (or NACK) bit, and ends with STOP condition. The command byte includes a 7-bit chip address and an R/W bit. The ACK (or NACK) is always sent out by receiver. When in write transfer, data bytes is written out from MCU, and when in read transfer, data bytes is read out from RDA5807P. There is no visible register address in I^2C interface transfers.

RDA5807P always gives out ACK after every byte, and MCU gives out STOP condition when register programming is finished. For read transfer, after command byte from MCU, RDA5807P sends out the first register high byte, then the first register low byte, then the second register high byte, till receives NACK from MCU. MCU gives out ACK for data bytes besides last data byte. MCU gives out NACK for last data byte, and then RDA5807P will return the bus to MCU, and MCU will give out STOP condition.
The RDA5807P supported two type I^2C interface:RDA5807P Mode and TEA5767 Mode. The different register defined in different interface Mode.
Details refer to *RDA5807P Programming Guide*.

3.6 GPIO Outputs

The RDA5807P has three GPIOs and only used in RDA5807P Mode. The function of GPIOs could programmed with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0] and I2SEN.

If I2SEN is set to low, GPIO pins could be programmed to output low or high or high-Z, or be programmed to output interrupt and stereo indicator with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0]. GPIO2 could be programmed to output a low interrupt (interrupt will be generated only with interrupt enable bit STCIEN is set to high) when seek/tune process completes. GPIO3 could be programmed to output stereo indicator bit ST.

Constant low, high or high-Z functionality is available regardless of the state of VA and VD supplies or the ENABLE bit.

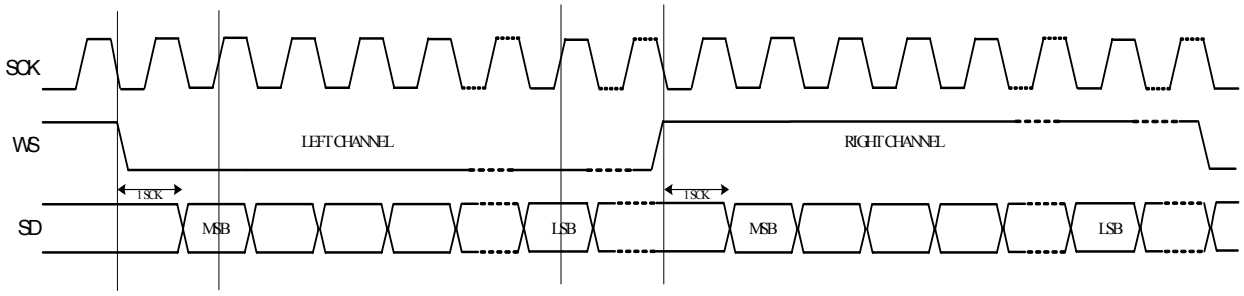


Figure 3-2. I2S Digital Audio Format

4 Electrical Characteristics

Table 4-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
AVDD	Analog Supply Voltage	2.7	3.3	5.5	V
DVDD	Digital Supply Voltage	2.7	3.3	5.5	V
V_{IO}	Interface Supply Voltage	1.5	-	3.6	V
T_{amb}	Ambient Temperature	-20	27	+70	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*DVDD	V
V_{IH}	CMOS High Level Input Voltage	0.7*VDD		DVDD	V
V_{TH}	CMOS Threshold Voltage		0.5*VDD		V

Table 4-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VIO	Interface Supply Voltage	-0.5		+4	V
T_{amb}	Ambient Temperature	-40		+90	°C
I_{IN}	Input Current (1)	-10		+10	mA
V_{IN}	Input Voltage(1)	-0.3		VIO+0.3	V
V_{lna}	LNA FM Input Level			-20	dBm

Notes:

1. for Pin: SCLK, SDIO, $\overline{SEN}$, $\overline{RST}$.

Table 4-3 Power Consumption Specification

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 ℃, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITION	TYP	UNIT
I_A	Analog Supply Current	ENABLE=1	15	mA
I_D	Digital Supply Current	ENABLE=1	2.5	mA
I_{VIO}	Interface Supply Current	SCLK and RCLK inactive	1	μA
I_{APD}	Analog Powerdown Current	ENABLE=0	2	μA
I_{DPD}	Digital Powerdown Current	ENABLE=0	2	μA

5 Receiver Characteristics

Table 5-1 Receiver Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
General specifications						
F_{in}	FM Input Frequency	BAND=0	87		108	MHz
		BAND=1	76		91	MHz
V_{rf}	Sensitivity[1,2,3]	(S+N)/N=26dB		1.5	2	μV EMF
R_{in}	LNA Input Resistance [7]			150		Ω
C_{in}	LNA Input Capacitance [7]		2	4	6	pF
$IP3_{in}$	Input IP3[4]	AGCD=1	80		-	dBμV
α_{am}	AM Suppression[1,2]	m=0.3	40	-	-	dB
S_{200}	Adjacent Channel Selectivity	±200KHz	45		-	dB
V_{AFL}; V_{AFR}	Left and Right Audio Frequency Output Voltage (Pins LOUT and ROUT)	Volume_dac[3:0] =1111		110		mV
(S+N)/N	Maximum Signal Plus Noise to Noise Ratio[1,2,3,5]		54	60	-	dB
α_{SCS}	Stereo Channel Separation		35	-	-	dB
THD	Audio Total Harmonic Distortion[1,3,6]			0.3	0.5	%
α_{AOI}	Audio Output L/R Imbalance				1	dB
R_L	Audio Output Loading Resistance	Single-ended	32	-	-	Ω
Pins LNAN, LNAP, LOUT, ROUT and NC(22,23)						
V_{com_rfin}	Pins LNAN and LNAP Input Common Mode Voltage			**Float**		V
V_{com}	Audio Output Common Mode Voltage[8]		1.2	1.25	1.3	V
V_{com_nc}	Pins NC (22, 23) Common Mode Voltage		0.45	0.5	0.55	V
! The NC(22, 23) pins SHOULD BE left floating.						

Notes:

1. F_{in}=76 to 108MHz; F_{mod}=1KHz; de-emphasis=75μs; MONO=1; L=R unless noted otherwise;
2. Δf=22.5KHz;
3. B_{AF} = 300Hz to 15KHz, RBW <=10Hz;
4. $|f_2-f_1|$>1MHz, $f_0=2xf_1-f_2$, AGC disable, F_{in}=76 to 108MHz;
5. P_{RF}=60dB$_U$V;
6. Δf=75KHz.
7. Measured at V_{EMF} = 1 m V, f_{RF} = 76 to 108MHz
8. At LOUT and ROUT pins

6 Serial Interface

6.1 I²C Interface Timing

Table 6-1 I²C Interface Timing Characteristics

(VDD = 2.7 to 5.5 V, T_A = -25 to 85 °C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Frequency	f_{scl}		0	-	400	KHz
SCLK High Time	t_{high}		0.6	-	-	μs
SCLK Low Time	t_{low}		1.3	-	-	μs
Setup Time for START Condition	$t_{su:sta}$		0.6	-	-	μs
Hold Time for START Condition	$t_{hd:sta}$		0.6	-	-	μs
Setup Time for STOP Condition	$t_{su:sto}$		0.6	-	-	μs
SDIO Input to SCLK↑ Setup	$t_{su:dat}$		100	-	-	ns
SDIO Input to SCLK↓ Hold	$t_{hd:dat}$		0	-	900	ns
STOP to START Time	t_{buf}		1.3	-	-	μs
SDIO Output Fall Time	$t_{f:out}$		20+0.1C_b	-	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{r:in}$ / $t_{f:in}$		20+0.1C_b	-	300	ns
Input Spike Suppression	t_{sp}		-	-	50	ns
SCLK, SDIO Capacitive Loading	C_b		-	-	50	pF
Digital Input Pin Capacitance					5	pF

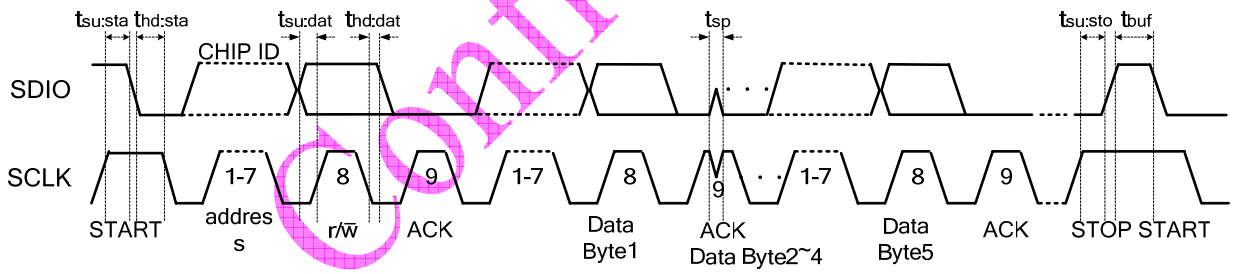


Figure 6-1. I²C Interface Write Timing Diagram

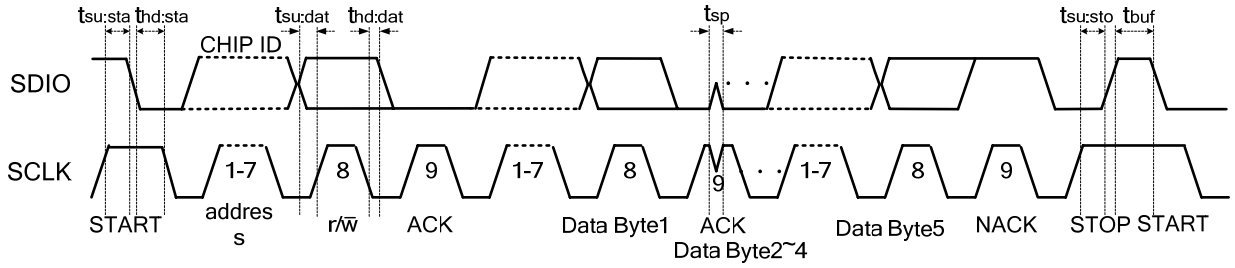


Figure 6-2. I²C Interface Read Timing Diagram

7 7 Pins Description

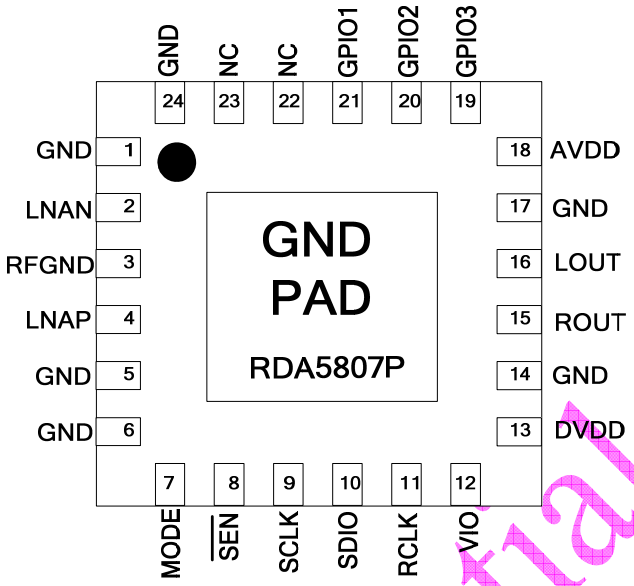
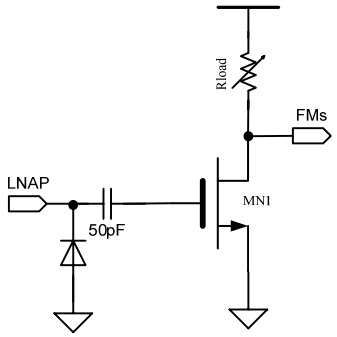
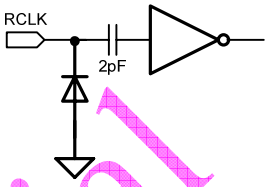
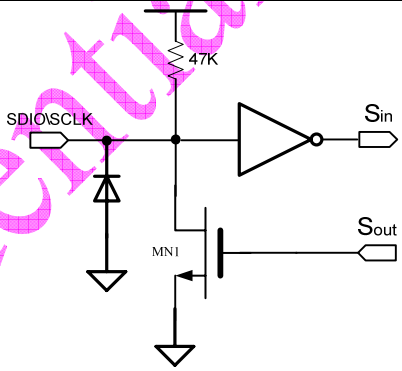
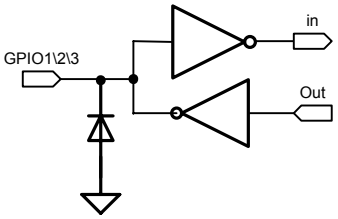


Figure 7-1. RDA5807P Top View

Table 7-1 RDA5807P Pins Description

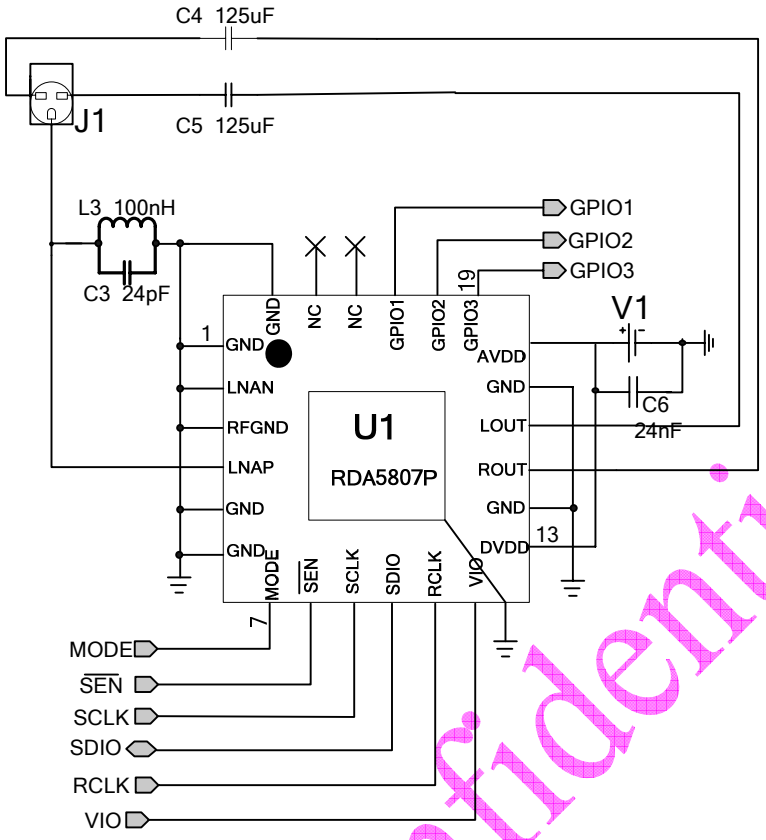
SYMBOL	PIN	DESCRIPTION
GND	1,5,6,14,17,24	Ground. Connect to ground plane on PCB
LNAN,LNAP	2,4	LNA input port. For single-ended input, LNAN should be connected to RFGND
RFGND	3	LNA ground. Connect to ground plane on PCB
MODE	7	Control Interface select The MODE Pin is low ,I2C Interface is select. The MODE Pin is set to VIO, SPI Interface is select.
$\overline{SEN}$	8	Latch enable (active low) input for serial control bus
SCLK	9	Clock input for serial control bus
SDIO	10	Data input/output for serial control bus
RCLK	11	External reference clock input
VIO	12	Power supply for I/O
DVDD	13	Power supply for digital section
ROUT,LOUT	15,16	Right/Left audio output
AVDD	18	Power supply for analog section
GPIO1,GPIO2,GPIO3	19,20,21	General purpose input/output
NC	22,23	No Connect

Table 7-2 Internal Pin Configuration

SYMBOL	PIN	DESCRIPTION
LNAN/LNAP	2/4	
RCLK	11	
SCLK/SDIO	9/10	
GPIO1/GPIO2/GPIO3	19/20/21	

8 Application Diagram

8.1 Audio Loading Resistance Larger than 32Ω & TCXO Application:



Notes:

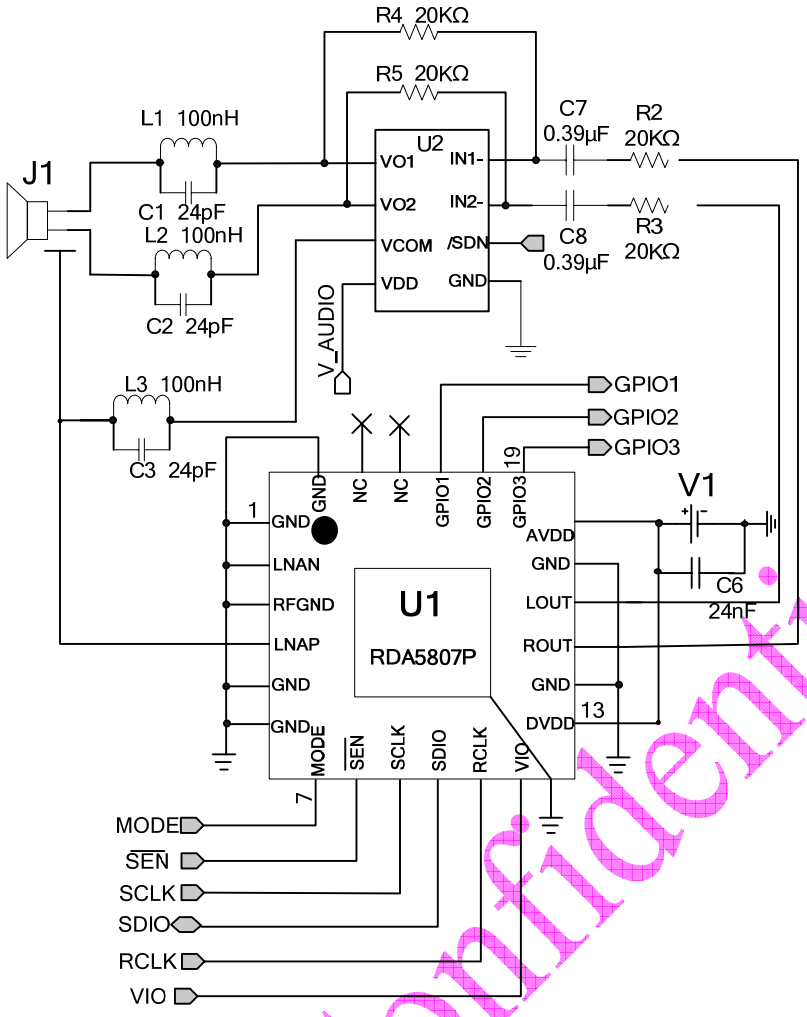
1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5807P Chip;
3. V1: Analog and Digital Power Supply (2.7~5.5V);
4. FM Choke (L3 and C3) for Audio Common and LNA Input Common;
5. Pins NC(22, 23), Should be Leaved Floating;
6. Set MODE to select control interface(GND—I2C,VIO—SPI);
6. Place C6 Close to AVDD pin.

Figure 8-1. RDA5807P FM Tuner Application Diagram (TCXO Application)

8.1.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5807P	Broadcast FM Radio Tuner	RDA
J1		Common 32Ω Resistance Headphone	
L3/C3	100nH/24pF	LC Chock for LNA Input	Murata
C4,C5	125μF	Audio AC Couple Capacitors	Murata
C6	24nF	Power Supply Bypass Capacitor	Murata

8.2 Audio Loading Resistance Lower than 32Ω & TCXO Application:



Notes:

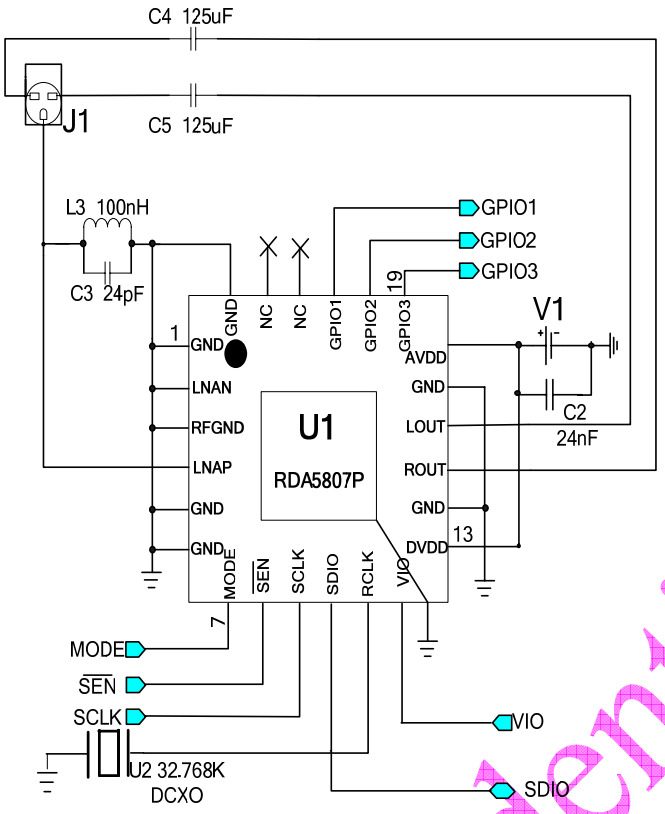
1. J1: Resistance Lower than 32Ω Audio Speaker or Headphone
2. U1: RDA5807P Chip
3. V1: Analog and Digital Power Supply (2.7~5.5V)
4. FM Choke (L3 and C3) for Audio Common and LNA Input Common
5. Pins NC(22, 23),Should be Leaved Floating;
6. Set MODE to select control interface(GND—I2C,VIO—SPI);
7. Place C6 Close to AVDD pin
8. Changing the Resistor R4 and R5 Value can Change the Output Volume.
9. Place U2 Close to U1

Figure 8-2. RDA5807P FM Tuner Application Diagram (Audio Amplifier Application)

8.2.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5807P	Broadcast FM Radio Tuner	RDA
U2	RDA2892	Audio Amplifier	RDA
J1		Audio Speaker	
L1/C1; L2/C2	100nH/24pF	LC Chock for Audio Output	Murata
L3/C3	100nH/24pF	LC Chock for LNA Input	Murata
C6	24nF	Power Supply Bypass Capacitor	Murata
R4,R5	20KΩ	Audio Amplifier Feedback Resistors	Murata
R2/C7; R3/C8	20KΩ/0.39μF	Audio High-passed Filter and Amplifier Input Resistors	Murata

8.3 Audio Loading Resistance Larger than 32Ω & DCXO Application:



Notes:

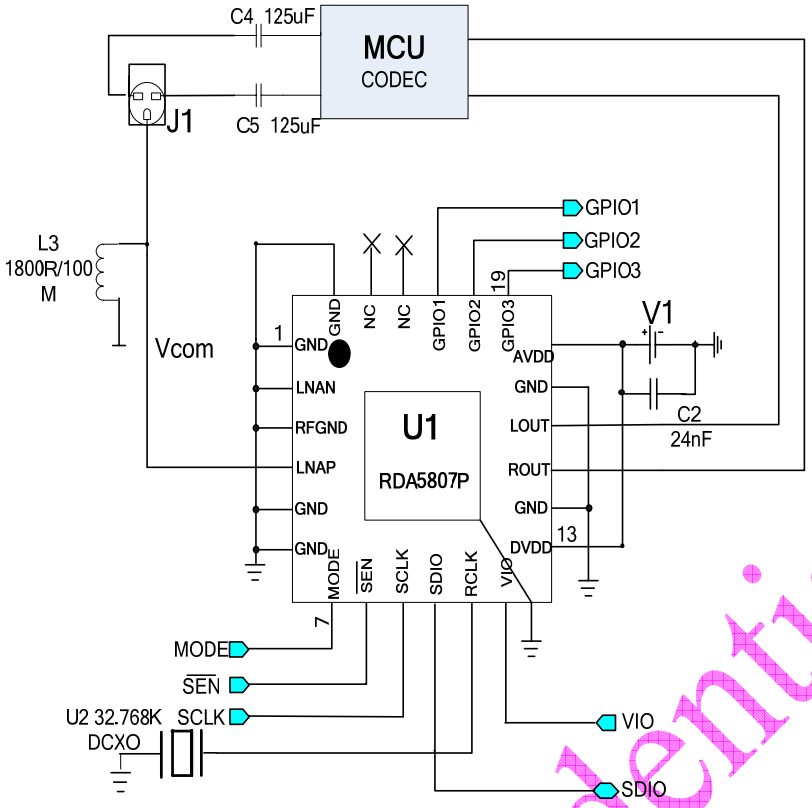
1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5807P Chip;
3. U2: 32.768KHz Crystal oscillator
4. V1: Analog and Digital Power Supply (2.7~5.5V);
5. FM Choke (L3 and C3) for Audio Common and LNA Input Common;
6. Pins NC(22, 23) Should be Leaved Floating;
7. Set MODE to select control interface(GND—I2C,VIO—SPI);
8. Place C2 Close to AVDD pin.

Figure 8-3. RDA5807P FM Tuner Application Diagram (DCXO Application)

8.3.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5807P	Broadcast FM Radio Tuner	RDA
U2	DCXO	Crystal oscillator 32.768KHz	<=50PPM
J1		Common 32Ω Resistance Headphone	
L3/C3	100nH/24pF	LC Chock for LNA Input	Murata
C4,C5	125μF	Audio AC Couple Capacitors	Murata
C2	24nF	Power Supply Bypass Capacitor	Murata

8.4 MCU CODEC Application:



Notes:

1. J1: Common 32Ω Resistance Headphone;
2. U1: RDA5807P Chip;
3. U2: 32.768KHz Crystal oscillator
3. V1: Analog and Digital Power Supply (2.7~5.5V);
4. FM Choke L3 for LNA Input Common;
5. Pins NC(22, 23) Should be Leaved Floating;
6. Set MODE to select control interface(GND—I2C,VIO—SPI);
7. Place C2 Close to AVDD pin.

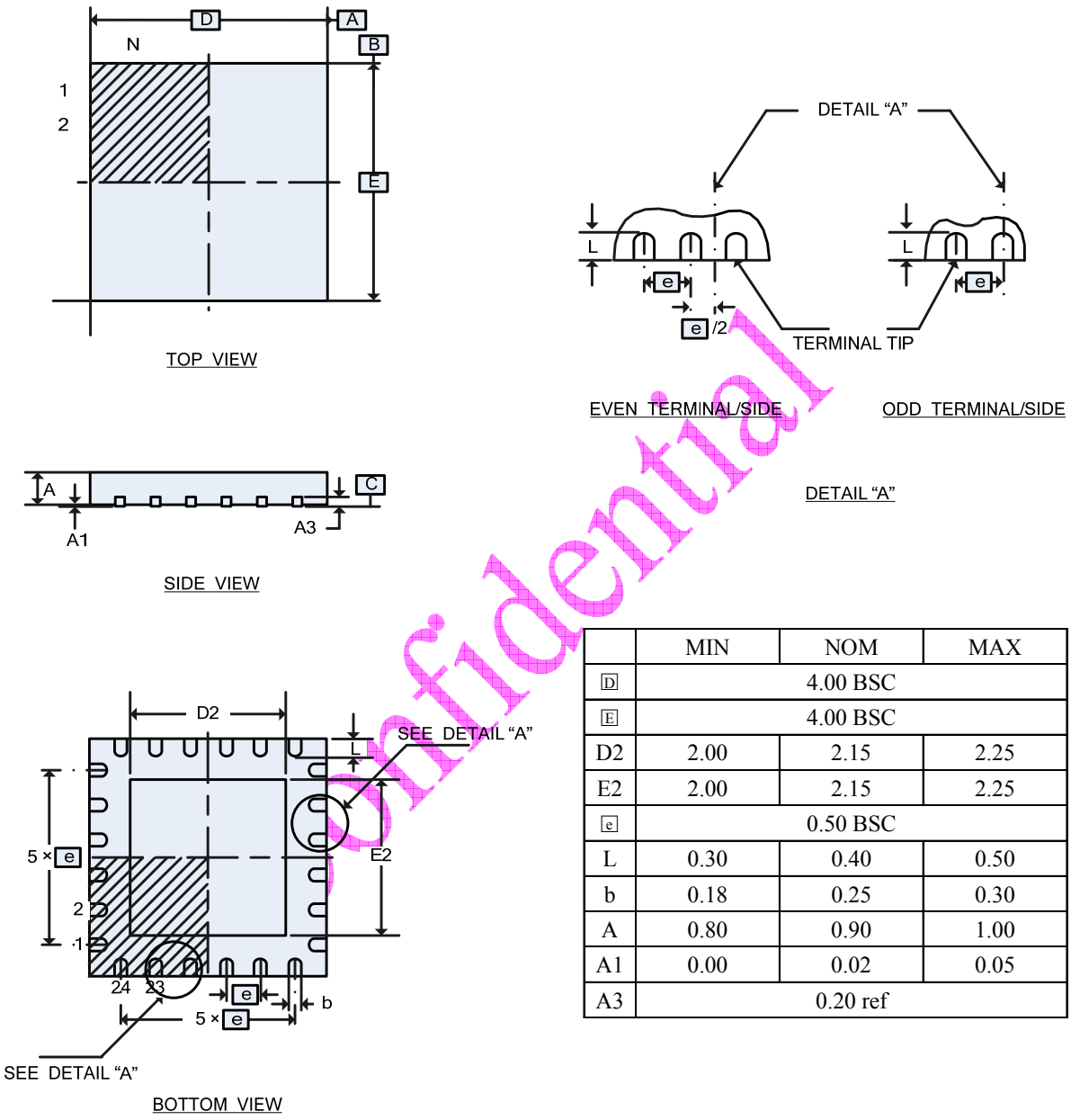
Figure 8-4. RDA5807P FM Tuner Application Diagram (DCXO+MCU CODEC Application)

8.4.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5807P	Broadcast FM Radio Tuner	RDA
U2	DCXO	Crystal oscillator 32.768KHz	<=50PPM
J1		Common 32Ω Resistance Headphone	
L3	1800R/100M	Common for LNA Input	Murata
C4,C5	125μF	Audio AC Couple Capacitors	Murata
C2	24nF	Power Supply Bypass Capacitor	Murata

9 Package Physical Dimension

Figure 9-1 illustrates the package details for the RDA5807P. The package is lead-free and RoHS-compliant.



	MIN	NOM	MAX
D		4.00 BSC	
E		4.00 BSC	
D2	2.00	2.15	2.25
E2	2.00	2.15	2.25
e		0.50 BSC	
L	0.30	0.40	0.50
b	0.18	0.25	0.30
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A3		0.20 ref	

Figure 9-1 24-Pin 4x4 Quad Flat No-Lead (QFN)

10 PCB Land Pattern：

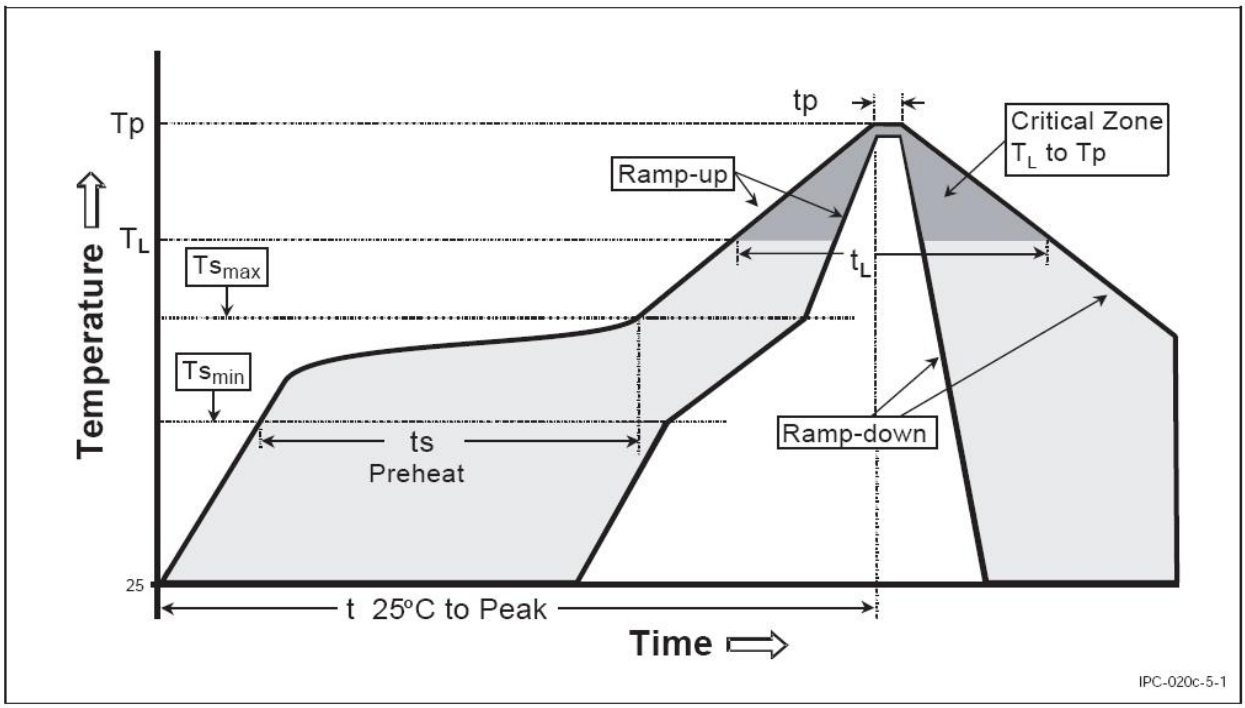


Figure 10-1.Classification Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183 °C 60-150seconds	 217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak Temperature	6 minutes max.	8 minutes max.

Table-I Classification Reflow Profiles

Package Thickness	Volume mm^3 <350	Volume mm^3 ⩾350
＜2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
⩾2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 ＜350	Volume mm^3 350-2000	Volume mm^3 ＞2000
＜1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
⩾2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Table – III Pb-free Process – Package Classification Reflow Temperatures

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever

is required to control the profile process but at no time will it exceed – 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process **shall** be evaluated using the “lead free” classification temperatures and profiles defined in Table-I II III whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

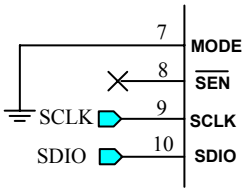
Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

11 Change list

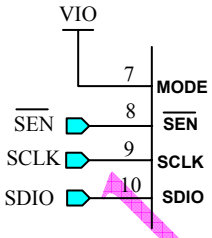
REV	DATE	AUTHOR	CHANGE DESCRIPTION
V1.0	2008-8-26	Xiaoqi You	Original Draft.

12 Notes：

1：通过硬件电路设置芯片工作总线控制模式，详细电路如下图：



附图：I2C 总线电路接口电路



SPI 总线电路接口电路

附图：I^2C总线电路接口电路

13 Contact Information

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