MC34001, B
MC34002, B
MC34004, B

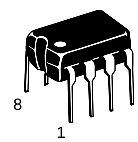
JFET Input Operational Amplifiers

These low cost JFET input operational amplifiers combine two state–of–the–art analog technologies on a single monolithic integrated circuit. Each internally compensated operational amplifier has well matched high voltage JFET input devices for low input offset voltage. The BIFET technology provides wide bandwidths and fast slew rates with low input bias currents, input offset currents, and supply currents.

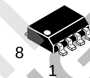
The ON Semiconductor BIFET family offers single, dual and quad operational amplifiers which are pin–compatible with the industry standard MC1741, MC1458, and the MC3403/LM324 bipolar devices. The MC34001/34002/34004 series are specified from 0° to +70°C.

- Input Offset Voltage Options of 5.0 mV and 10 mV Maximum
- Low Input Bias Current: 40 pA
- Low Input Offset Current: 10 pA
- Wide Gain Bandwidth: 4.0 MHz
- High Slew Rate: 13 V/µs
- Low Supply Current: 1.4 mA per Amplifier
- High Input Impedance: 10^{12} Ω
- High Common Mode and Supply Voltage Rejection Ratios: 100 dB
- Industry Standard Pinouts

JFET INPUT OPERATIONAL AMPLIFIERS

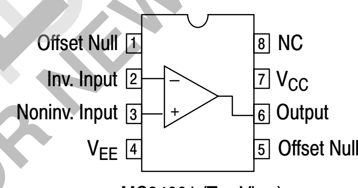


P SUFFIX
PLASTIC PACKAGE
CASE 626

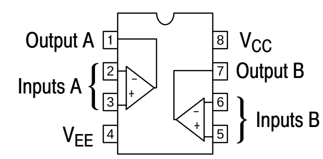


D SUFFIX
PLASTIC PACKAGE
CASE 751
(SO–8)

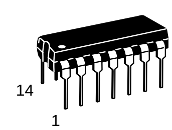
PIN CONNECTIONS



MC34001 (Top View)

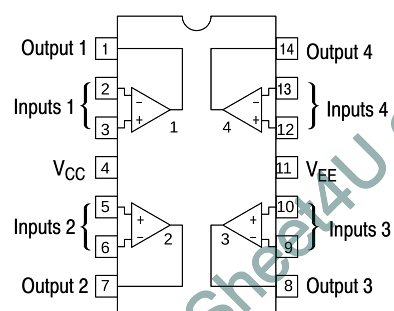


MC34002 (Top View)



P SUFFIX
PLASTIC PACKAGE
CASE 646

PIN CONNECTIONS



MC34004 (Top View)

ORDERING INFORMATION

Op Amp Function	Device	Operating Temperature Range	Package
Single	MC34001BD, D	T_A = 0° to+ 70°C	SO–8
	MC34001BP, P		Plastic DIP
Dual	MC34002BD, D	T_A = 0° to +70°C	SO–8
	MC34002BP, P		Plastic DIP
Quad	MC34004BP, P	T_A = 0° to +70°C	Plastic DIP

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}, V_{EE}	±18	V
Differential Input Voltage (Note 1)	V_{ID}	±30	V
Input Voltage Range	V_{IDR}	±16	V
Open Short Circuit Duration	t_{SC}	Continuous	
Operating Ambient Temperature Range	T_A	0 to +70	°C
Operating Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C

NOTES: 1. Unless otherwise specified, the absolute maximum negative input voltage is equal to the negative power supply.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = 25°C, unless otherwise noted.)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 k) MC3400XB MC3400X	V_{IO}	 — —	 3.0 5.0	 5.0 10	mV
Average Temperature Coefficient of Input Offset Voltage R_S ≤ 10 k, T_A = T_{low} to T_{high} (Note 2)	$\Delta V_{IO}/\Delta T$	—	10	—	μV/°C
Input Offset Current (V_{CM} = 0) (Note 3) MC3400XB MC3400X	I_{IO}	 — —	 25 25	 100 100	pA
Input Bias Current (V_{CM} = 0) (Note 3) MC3400XB MC3400X	I_{IB}	 — —	 50 50	 200 200	pA
Input Resistance	r_i	—	10^{12}	—	Ω
Common Mode Input Voltage Range	V_{ICR}	±11 —	+15 –12	— —	V
Large Signal Voltage Gain (V_O = ±10 V, R_L = 2.0 k) MC3400XB MC3400X	A_{VOL}	 50 25	 150 100	 — —	V/mV
Output Voltage Swing (R_L ≥ 10 k) (R_L ≥ 2.0 k)	V_O	 ±12 ±10	 ±14 ±13	 — —	V
Common Mode Rejection Ratio (R_S ≤ 10 k) MC3400XB MC3400X	CMRR	 80 70	 100 100	 — —	dB
Supply Voltage Rejection Ratio (R_S ≤ 10 k) (Note 4) MC3400XB MC3400X	PSRR	 80 70	 100 100	 — —	dB
Supply Current (Each Amplifier) MC3400XB MC3400X	I_D	 — —	 1.4 1.4	 2.5 2.7	mA
Slew Rate (A_V = 1.0)	SR	—	13	—	V/μs
Gain–Bandwidth Product	GBW	—	4.0	—	MHz
Equivalent Input Noise Voltage (R_S = 100 Ω, f = 1000 Hz)	e_n	—	25	—	$nV/\sqrt{Hz}$
Equivalent Input Noise Current (f = 1000 Hz)	i_n	—	0.01	—	$pA/\sqrt{Hz}$

NOTES: 2. T_{low} = 0°C for MC34001/34001B, MC34002, MC34004/34004B; T_{high} = +70°C for MC34001/34001B, MC34002, MC34004/34004B

3. The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heatsink is recommended if input bias current is to be kept to a minimum.
4. Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = –15 V, T_A = T_{low} to T_{high} [Note 2].)

Characteristics	Symbol	Min	Typ	Max	Unit
Input Offset Voltage (R_S ≤ 10 k)	V_{IO}				mV
MC3400XB		—	—	7.0	
MC3400X		—	—	13	
Input Offset Current (V_{CM} = 0) (Note 3)	I_{IO}				nA
MC3400XB		—	—	4.0	
MC3400X		—	—	4.0	
Input Bias Current (V_{CM} = 0) (Note 3)	I_{IB}				nA
MC3400XB		—	—	8.0	
MC3400X		—	—	8.0	
Common Mode Input Voltage Range	V_{ICR}	±11	—	—	V
Large Signal (V_O = ±10 V, R_L = 2.0 k)	A_{VOL}				V/mV
MC3400XB		25	—	—	
MC3400X		15	—	—	
Output Voltage Swing	V_O				V
(R ≥ 10 k)		±12	—	—	
(R ≥ 2.0 k)		±10	—	—	
Common Mode Rejection Ratio (R_S ≤ 10 k)	CMRR				dB
MC3400XB		80	—	—	
MC3400X		70	—	—	
Supply Voltage Rejection Ratio (R_S ≤ 10 k) (Note 4)	PSRR				dB
MC3400XB		80	—	—	
MC3400X		70	—	—	
Supply Current (Each Amplifier)	I_D				mA
MC3400XB		—	—	2.8	
MC3400X		—	—	3.0	

NOTES: 2. T_{low} = 0°C for MC34001/34001B; MC34002; MC34004/34004B — T_{high} = +70°C for MC34001/34001B; … MC34002; °C MC34004/34004B

3. The input bias currents approximately double for every 10°C rise in junction temperature, T_J. Due to limited test time, the input bias currents are correlated to junction temperature. Use of a heatsink is recommended if input bias current is to be kept to a minimum.
4. Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Figure 1. Input Bias Current versus Temperature

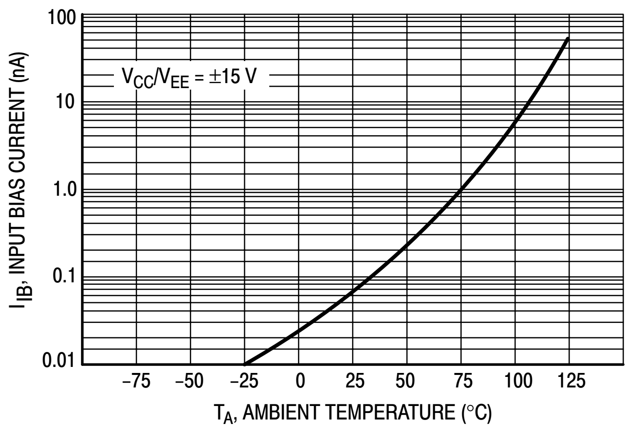


Figure 2. Output Voltage Swing versus Frequency

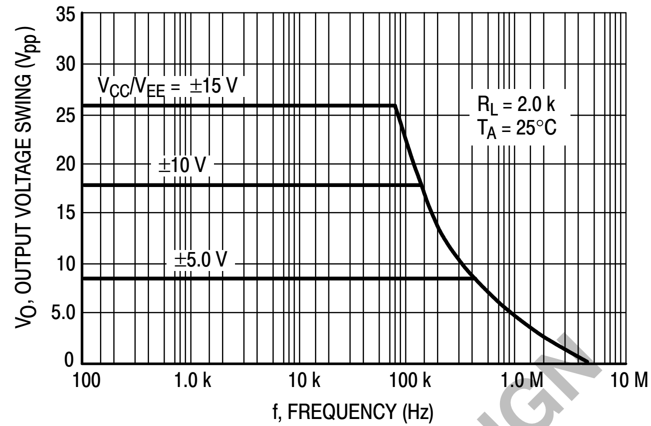


Figure 3. Output Voltage Swing versus Load Resistance

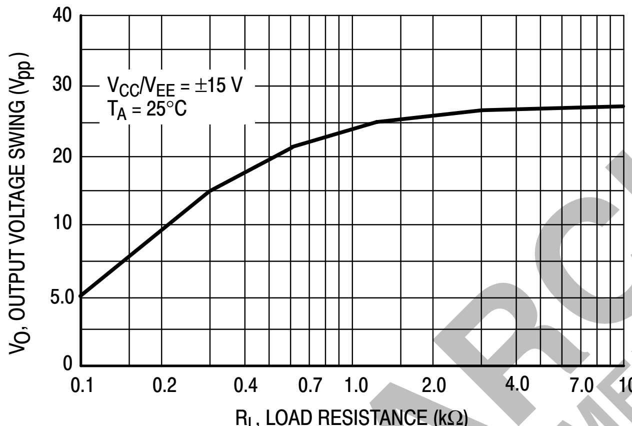


Figure 4. Output Voltage Swing versus Supply Voltage

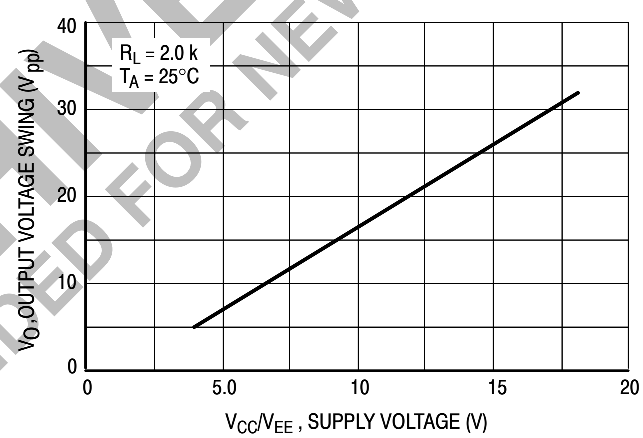


Figure 5. Output Voltage Swing versus Temperature

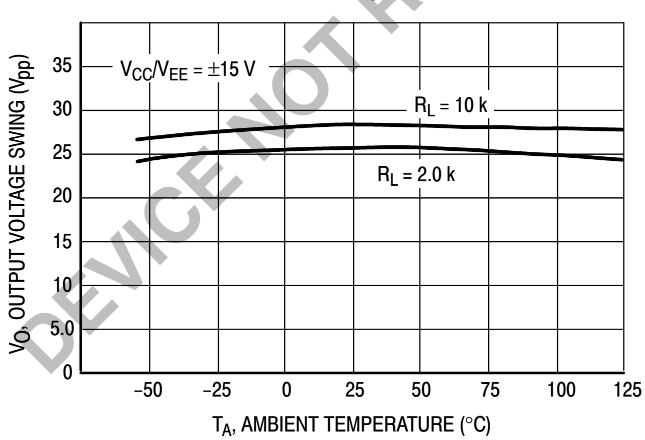


Figure 6. Supply Current per Amplifier versus Temperature

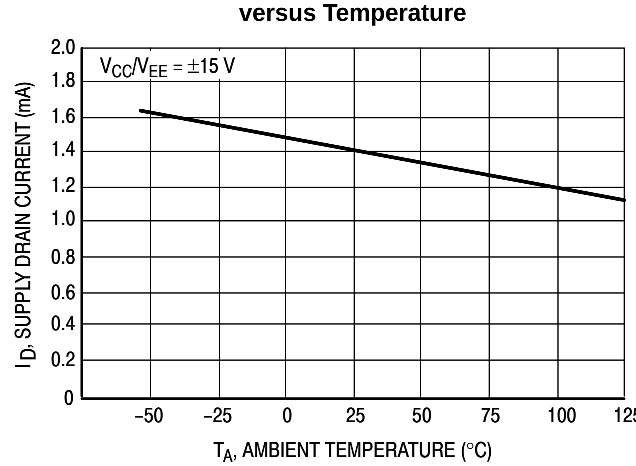


Figure 7. Large–Signal Voltage Gain and Phase Shift versus Frequency

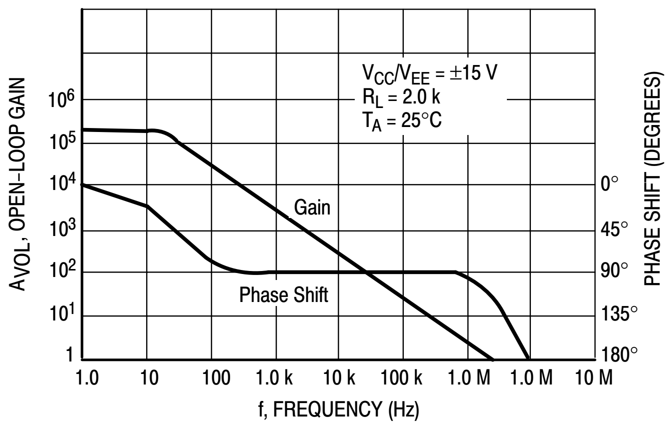


Figure 8. Large–Signal Voltage Gain versus Temperature

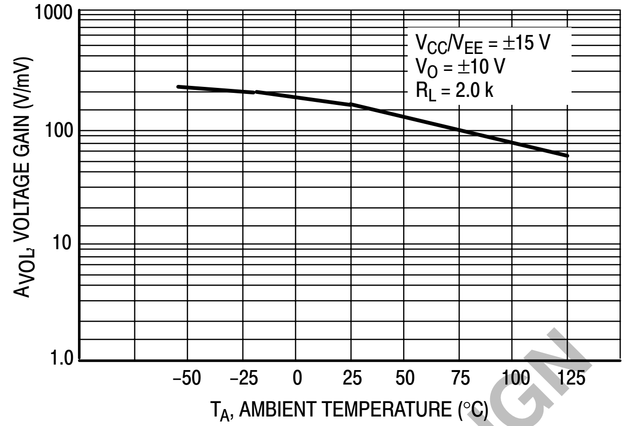


Figure 9. Normalized Slew Rate versus Temperature

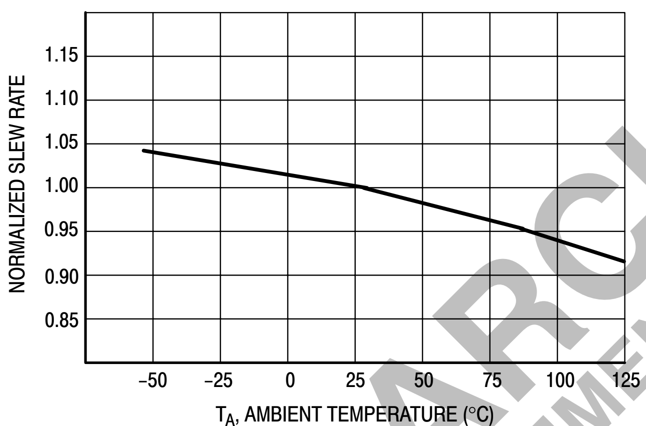


Figure 10. Equivalent Input Noise Voltage versus Frequency

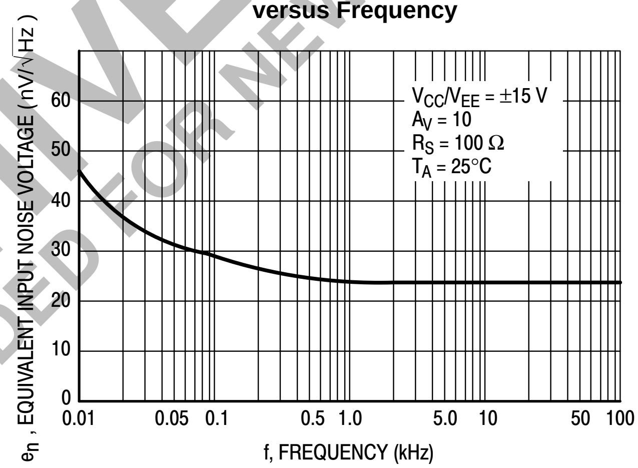
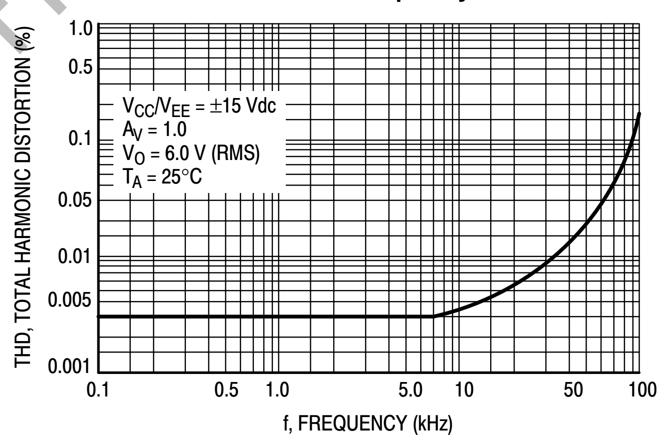


Figure 11. Total Harmonic Distortion versus Frequency



Representative Circuit Schematic
(Each Amplifier)

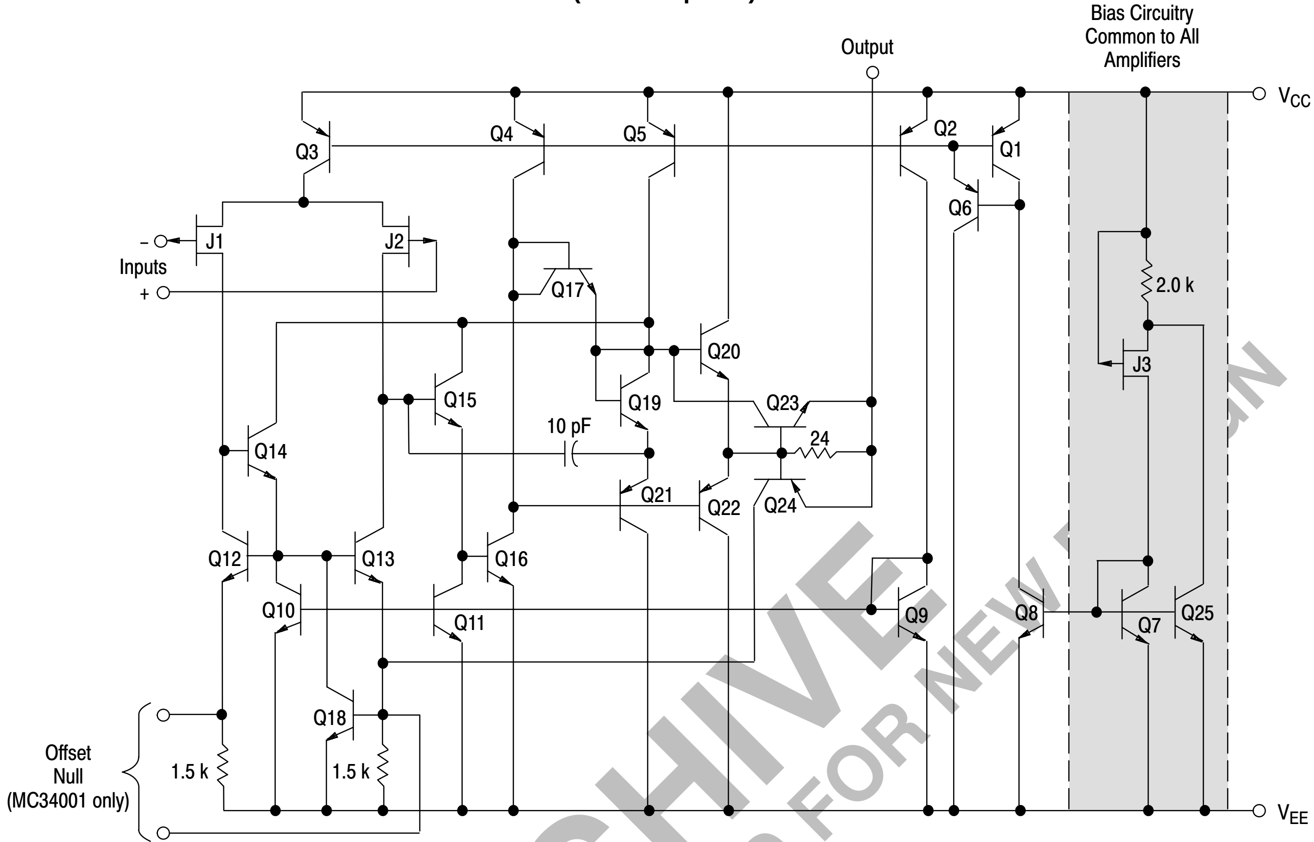
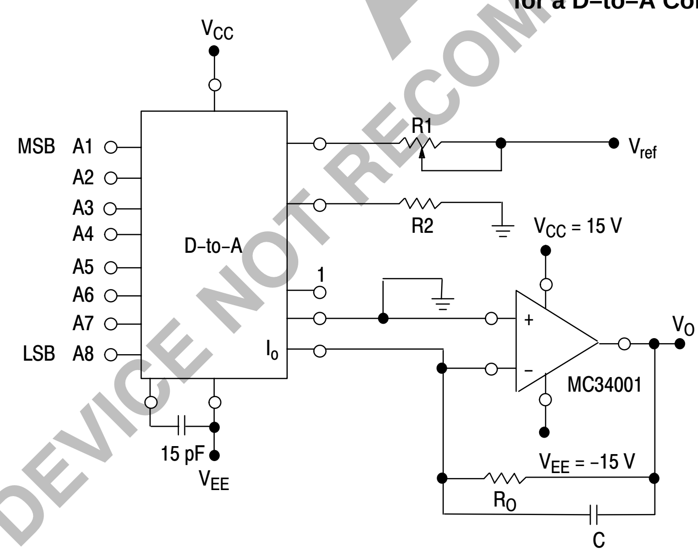


Figure 12. Output Current to Voltage Transformation
for a D–to–A Converter



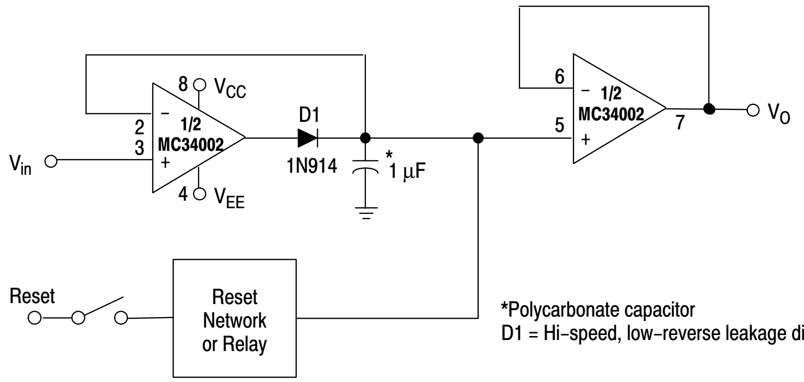
Settling time to within 1/2 LSB is approximately 4.0 μs from the time all bits are switched (C = 68 pF).

The value of C may be selected to minimize overshoot and ringing.

Theoretical V_O

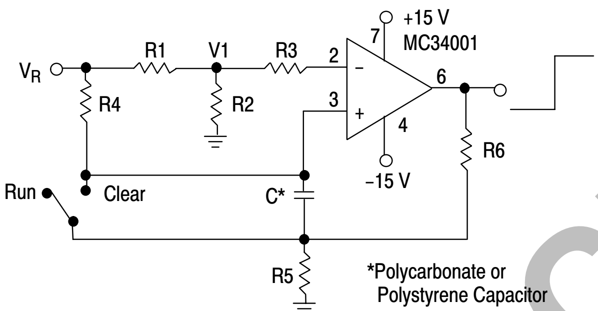
$$V_O = \frac{V_{ref}}{R1}(R_O)\left[\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \frac{A4}{16} + \frac{A5}{32} + \frac{A6}{64} + \frac{A7}{128} + \frac{A8}{256}\right]$$

Figure 13. Positive Peak Detector



*Polycarbonate capacitor
D1 = Hi−speed, low−reverse leakage diode

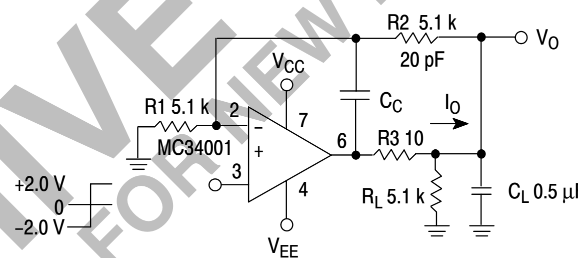
Figure 14. Long Interval RC Timer



Time (t) = R4 Cn ($V_R/V_R - V_I$), $R_3 = R_4$, $R_5 = 0.1\ R_6$
If R1 = R2: t = 0.693 R4C

Design Example: 100 Second Timer
V_R = 10 V   C = 1.0 µF   R3 = R4 = 144 M
R6 = 20 k   R5 = 2.0 k   R1 = R2 = 1.0 k

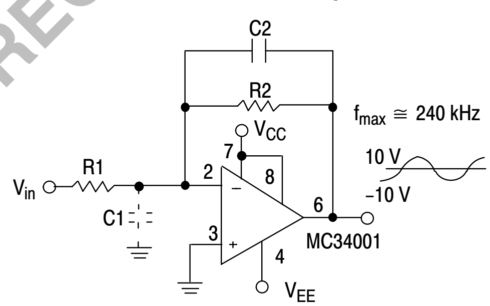
Figure 15. Isolating Large Capacitive Loads



Overshoot < 10%
t_s = 10 µs
When driving large C_L, the V_O slew rate is determined by C_L and $I_{O(max)}$:

$$\frac{\Delta V_O}{\Delta t} = \frac{I_O}{C_L} = \frac{0.02}{0.5}\ \text{V/µs} = 0.04\ \text{V/µs (with } C_L \text{ shown)}$$

Figure 16. Wide BW, Low Noise, Low Drift Amplifier

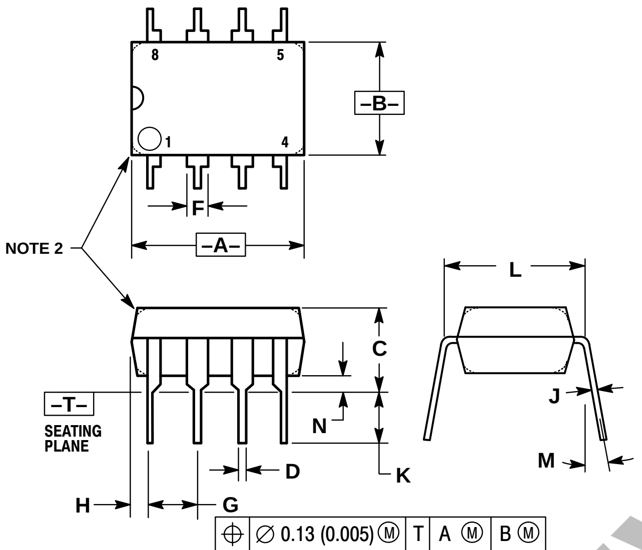


Power BW: $f_{max} = \frac{S_r}{2\pi\ Vp} \cong 240$ kHz

Parasitic input capacitance (C1 ≅ 3.0 pF plus any additional layout capacitance) interacts with feedback elements and creates undesirable high−frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

OUTLINE DIMENSIONS

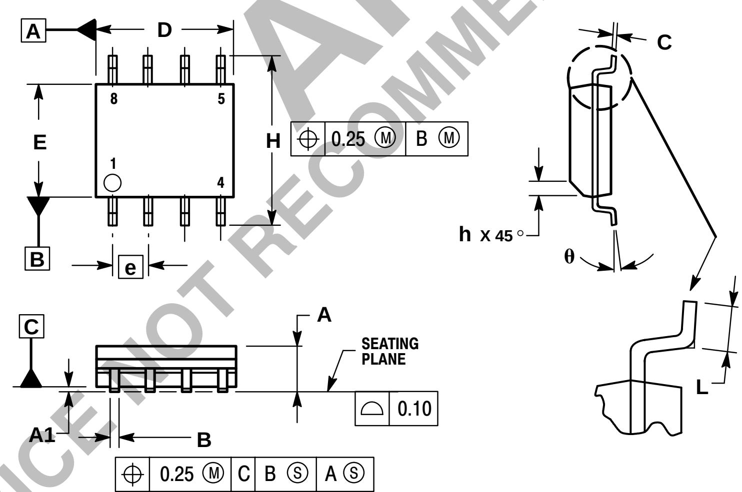
P SUFFIX
PLASTIC PACKAGE
CASE 626–05
ISSUE K



NOTES:
1. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
2. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	–––	10°	–––	10°
N	0.76	1.01	0.030	0.040

D SUFFIX
PLASTIC PACKAGE
CASE 751–05
(SO–8)
ISSUE R

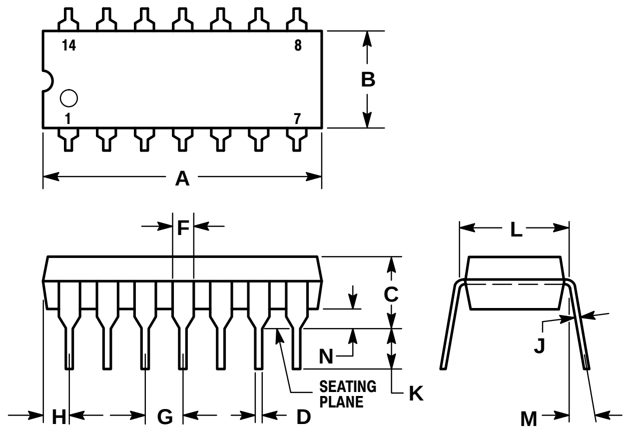


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.18	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

OUTLINE DIMENSIONS

P SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0°	10°	0°	10°
N	0.015	0.039	0.39	1.01

NOTES

NOTES

PUBLICATION ORDERING INFORMATION

Literature Fulfillment:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
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Phone: 81–3–5740–2700
Email: r14525@onsemi.com

ON Semiconductor Website: http://onsemi.com

For additional information, please contact your local Sales Representative.