TOSHIBA

SILICON STACKED GATE CMOS

## 32,768 WORD x 8 BIT ONE TIME PROGRAMMABLE READ ONLY MEMORY

Description

The TC54256AP/AF is a 32,768 word x 8 bit one time programmable read only memory molded in a 28-pin plastic package. The TC54256AP/AF's access time is 200ns and it has a low power standby mode which reduces the power dissipation without increasing access time. The electrical characteristics and programming method are the same as for the TC57256AD UV EPROM. Once programmed, the TC54256AP/AF cannot be erased because of the use of a plastic DIP without a transparent window.

Features

- Peripheral circuit   : CMOS
  Memory cell   : NMOS
- Low power dissipation
  - Active   : 30mA/6.7MHz
  - Standby   : 100μA
- Fast access time   : 200ns
- Single 5V power supply
- Fully static operation
- High speed programming mode
- Inputs and outputs TTL compatible
- Pin compatible with ROM TC53257P, TMM23256P, EPROM TMM27256D/AD, TC57256D/AD, One time PROM TMM24256P/AP, and TC54256P
- Package
  - TC54256AP   : DIP28-P-600
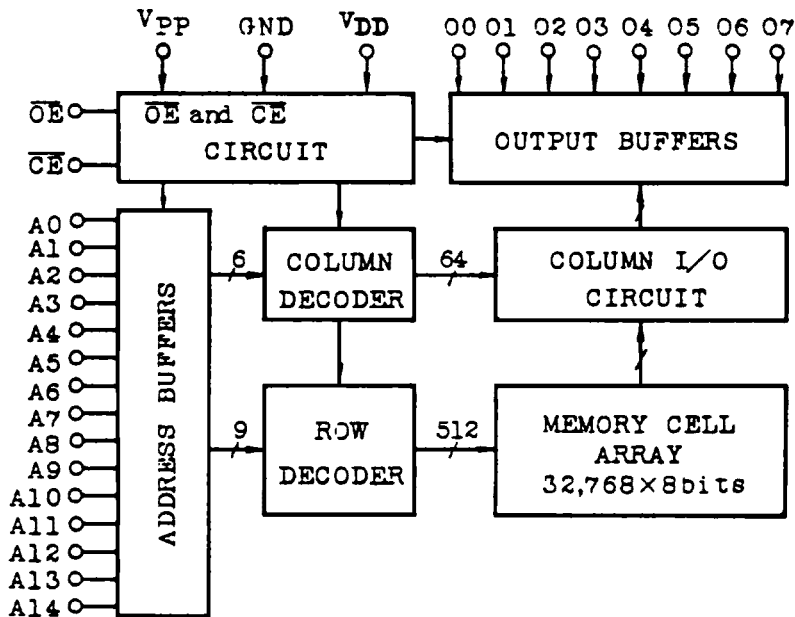 - TC54256AF   : SOP28-P-450

Pin Connection (Top View)
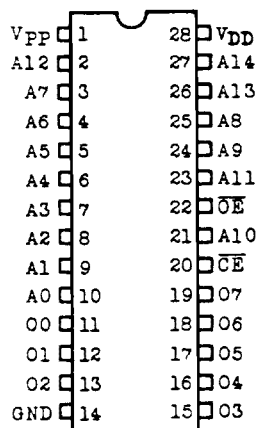
Pin Names

A0 ~ A14	Address Inputs
O0 ~ O7	Outputs (Inputs)
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
V_{PP}	Program Supply Voltage
V_{DD}	Power Supply Voltage (+5V)
GND	Ground

Block Diagram

Operating Mode

	PIN	$\overline{CE}$	$\overline{OE}$	V_{PP}	V_{DD}	00 ~ 07	POWER
MODE		(20)	(22)	(1)	(28)	(11 ~ 13, 15 ~ 19)	
Read		L	L			Data Out	Active
Output Deselect		*	H	5V	5V	High Impedance	
Standby		H	*			High Impedance	Standby
Program		L	H			Data In	
Program Inhibit		H	H	12.5V	6V	High Impedance	Active
Program Verify		*	L			Data Out	

* H or L

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT
V_{DD}	Power Supply Voltage	-0.6 ~ 7.0	
V_{PP}	Program Supply Voltage	-0.6 ~ 14.0	
V_{IN}	Input Voltage	-0.6 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	-0.6 ~ V_{DD} + 0.5	
P_D	Power Dissipation	1.5	W
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
T_{STRG}	Storage Temperature	-65 ~ 125	°C
T_{OPR}	Operating Temperature	-40 ~ 85	

Read Mode

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{DD} + 0.3$	
V_{IL}	Input Low Voltage	-0.3	–	0.8	V
V_{DD}	Power Supply Voltage	4.75	5.00	5.25	
V_{PP}	Program Supply Voltage	$V_{DD} - 0.6$	V_{DD}	$V_{DD} + 0.6$	

DC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±5%)

SYMBOL	PARAMETER	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0V \sim V_{DD}$		–	–	±10	µA
I_{DDO1}	Operating Current	$\overline{CE} = 0V$	f = 6.7MHz	–	–	30	
I_{DDO2}			f = 1MHz	–	–	10	mA
I_{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		–	–	1	
I_{DDS2}		$\overline{CE} = V_{DD} - 0.2V$		–	–	100	µA
V_{OH}	Output High Voltage	$I_{OH} = -400µA$		2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$		–	–	0.4	
I_{PP1}	V_{PP} Current	$V_{PP} = V_{DD}±0.6V$		–	–	±10	µA
I_{LO}	Output Leakage Current	$V_{OUT} = 0.4V \sim V_{DD}$		–	–	±10	

AC Characteristics (Ta = -40 ~ 85°C, V_{DD} = 5V±5%, V_{PP} = $V_{DD}±0.6V$)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	MAX.	UNIT
t_{ACC}	Address Access Time	$\overline{CE} = \overline{OE} = V_{IL}$	–	200	
t_{CE}	$\overline{CE}$ to Output Valid	$\overline{OE} = V_{IL}$	–	200	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IL}$	–	70	
t_{DF1}	$\overline{CE}$ to Output in High-Z	$\overline{OE} = V_{IL}$	0	60	ns
t_{DF2}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IL}$	0	60	
t_{OH}	Output Data Hold Time	$\overline{CE} = \overline{OE} = V_{IL}$	0	–	

AC Test Conditions

Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

Capacitance* (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	$V_{IN} = 0V$	–	4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$	–	8	12	

*This parameter is periodically sampled and is not 100% tested.

Timing Waveforms (Read)
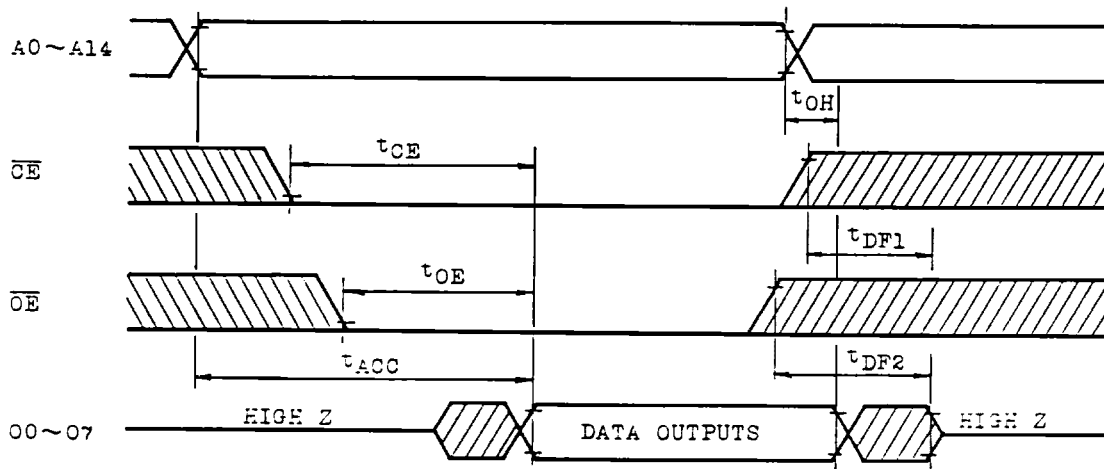
Program Mode

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.2	–	$V_{DD} + 1.0$	
V_{IL}	Input Low Voltage	-0.3	–	0.8	V
V_{DD}	Power Supply Voltage	5.75	6.0	6.25	
V_{PP}	Program Supply Voltage	12.0	12.5	13.0	

DC Characteristics (Ta = 25±5°C, V_{DD} = 6V±0.25V, V_{PP} = 12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{IN} = 0 \sim V_{DD}$	–	–	±10	μA
V_{OH}	Output High Voltage	$I_{OH} = -400\mu A$	2.4	–	–	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1mA$	–	–	0.4	
I_{DD}	V_{DD} Supply Current	–	–	–	40	mA
I_{PP2}	V_{PP} Supply Current	$V_{PP} = 13.0V$	–	–	50	
V_{ID}	A9 Auto Select Voltage	–	11.5	12.0	12.5	V

AC Programming Characteristics (Ta = 25±5°C, V_{DD} = 6V±0.25V, V_{PP} = 12.5V±0.5V)

SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
t_{AS}	Address Setup Time	–	2	–	–	μs
t_{AH}	Address Hold Time	–	2	–	–	
t_{CES}	$\overline{CE}$ Setup Time	–	0	–	–	ns
t_{CEH}	$\overline{CE}$ Hold Time	–	0	–	–	
t_{OES}	$\overline{OE}$ Setup Time	–	2	–	–	
t_{DS}	Data Setup Time	–	2	–	–	
t_{DH}	Data Hold Time	–	2	–	–	μs
t_{VPS}	V_{PP} Setup Time	–	2	–	–	
t_{VDS}	V_{DD} Setup Time	–	2	–	–	
t_{PW}	Initial Program Pulse Width	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$	0.95	1	1.05	ms
t_{OPW}	Overprogram Pulse Width	Note 1	2.85	3	78.75	
t_{OE}	$\overline{OE}$ to Output Valid	$\overline{CE} = V_{IH}$	–	–	150	ns
t_{DFP}	$\overline{OE}$ to Output in High-Z	$\overline{CE} = V_{IH}$	–	–	130	

Note 1: The length of the overprogram pulse may vary as a function of the counter value X.

AC Test Conditions

Input Pulse Levels	2.4V/0.45V
Input Pulse Rise and Fall Times	10ns max.
Input Timing Measurement Reference Levels	2.2V/0.8V
Output Timing Measurement Reference Levels	2.0V/0.8V
Output Load	1 TTL Gate and C_L = 100 pF

Timing Waveforms (Program)

$V_{DD} = 6V \pm 0.25V$, $V_{PP} = 12.5V \pm 0.5V$
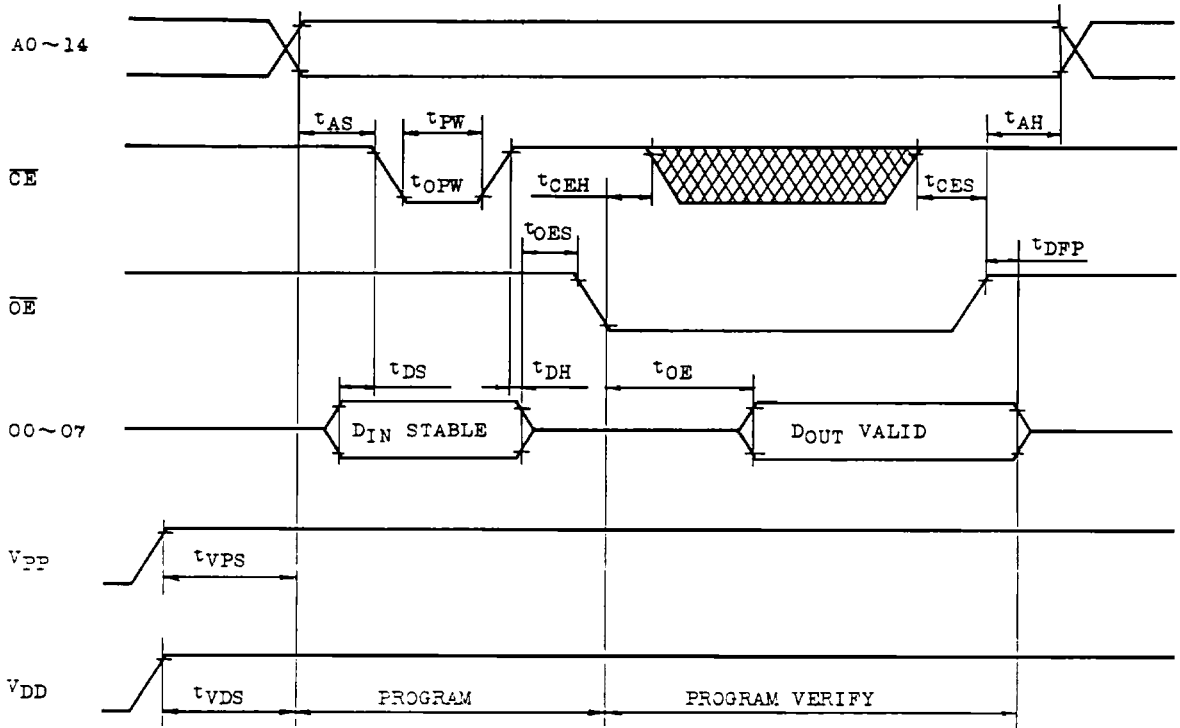
Notes:

1. V_{DD} must be applied simultaneously or before V_{PP} and cut off simultaneously or after V_{PP}

2. Removing the device from a programming socket and replacing the device in the socket while $V_{PP} = 12.5V$ may cause permanent damage to the device.

3. The V_{PP} supply voltage is permitted to be up to 14V for programming. Voltages over 14V should not be applied to the V_{PP} terminal. When the programming voltage is applied to the V_{PP} terminal, the overshoot voltage should not exceed 14V.

Operation Information

The TC54256AP/AF's six operating modes are listed in the following table. Mode selection is achieved by applying TTL level signals to appropriate inputs.

MODE	PIN NAMES (NUMBER)	$\overline{CE}$ (20)	$\overline{OE}$ (22)	V_{PP} (1)	V_{DD} (28)	OO ~ O7 (11 ~ 13, 15 ~ 19)	POWER
Read Operation (Ta = -40 ~ 85°C)	Read	L	L	5V	5V	Data Out	Active
	Output Deselect	*	H			High Impedance	
	Standby	H	*			High Impedance	Standby
Program Operation (Ta = 25±5°C)	Program	L	H	12.5V	6V	Data In	Active
	Program Inhibit	H	H			High Impedance	
	Program Verify	*	L			Data Out	

Notes: H = V_{IH}, L = V_{IL}, * = V_{IH} or V_{IL}

Read Mode

The TC54256AP/AF has two control inputs. The chip enable ($\overline{CE}$) input controls the operating power and should be used for device selection while the output enable ($\overline{OE}$) input controls the output buffers. Assuming that $\overline{CE} = \overline{OE} = V_{IL}$, once the address has stabilized, output data will be valid after the address access time has elapsed.

The $\overline{CE}$ to output valid time (t_{CE}) is equal to the address access time (t_{ACC}).

Assuming that $\overline{CE} = V_{IL}$ and that the address has been stable for at least t_{ACC}, then output data will be valid after t_{OE} from the falling edge of $\overline{OE}$.

Output Deselect Mode

If $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$, the outputs will be in a high impedance state.

Therefore, two or more devices can be connected together on a common bus if the output of only one device is enabled. When $\overline{CE}$ is used for device selection, all deselected devices are in the low power standby mode.

Standby Mode

The TC54256AP/AF has a low power standby mode controlled by the $\overline{CE}$ signal.

By applying a MOS high level voltage (V_{DD}) to the $\overline{CE}$ input, the TC54256AP/AF is placed in the standby mode which reduces the operating current to 100µA and puts the outputs in a high impedance state, independent of the $\overline{OE}$ input.

Program Mode

When the TC54256AP/AF is initially received by customers, all bits of the device are in the "1" state, which is the erased state. Therefore, the object of the program operation is to introduce "0" data into the desired bit locations.

The TC54256AP/AF is in the programming mode when V_{PP} = 12.5V, $\overline{CE} = V_{IL}$, and $\overline{OE} = V_{IH}$.

The TC54256AP/AF can be programmed at any address location at any time - either individually, sequentially, or at random.

Program Verify Mode

The verify mode is used to check that the desired data has been correctly programmed. The verify mode is activated when $\overline{OE} = V_{IL}$.

Program Inhibit Mode

When the programming voltage (+12.5V) is applied to the V_{PP} terminal, a high level $\overline{CE}$ input inhibits the TC54256AP/AF from being programmed.

The programming of two or more TC54256AP/AFs in parallel with different data is easily accomplished. All inputs except for $\overline{CE}$ and $\overline{OE}$ may be commonly connected, then a TTL low level program pulse is applied to the $\overline{CE}$ of the desired device only while a TTL high level signal is applied to the $\overline{CE}$ of the other devices.

High Speed Programming Mode

The device is set up in high speed programming mode when the programming voltage (+12.5V) is applied to the V_{PP} terminal with V_{DD} = 6V.

Programming is achieved by applying a single 1ms TTL low level pulse to the $\overline{CE}$ input after addresses and data are stable. Then the programmed data is verified by using the program verify mode. If the programmed data is not correct, another program pulse of 1ms is applied and then the programmed data is verified. This should be repeated until the data has programmed correctly (max. 25 times).

After correctly programming the selected address, an additional program pulse with a width of 3 times more than that needed for initial programming is applied. When programming has been completed, the data in all addresses should be verified with V_{DD} = V_{PP} = 5V.

High Speed Programming Mode

Flow Chart

```
                              START

                         ADDRESS =
                        START ADDRESS

                          V_DD = 6V

                         V_PP = 12.5V


                         DATA = FF? ──YES──┐
                             │NO           │
                           X = 0           │
                             │             │
                    PROGRAM: 1ms PULSE     │
                             │             │
                         X = X + 1         │
                             │             │
                        X > 25? ──YES──┐   │
                           │NO         │   │
              NG──── VERIFY            │   │
                        │OK            │   │
   ADDRESS =    OVERPROGRAM 3X PULSES OF 1ms │
   NEXT ADDRESS OR ONE PULSE OF 3X ms DURATION│
                        │             │   │
                      VERIFY ──NG──┐  │   │
                        │OK ◄──────┼──┘   │
                        │          │      │
          NO──── LAST          ◄───┘      │
                 ADDRESS?                 │
                        │YES              │
                    V_DD = 5.0V           │
                    V_PP = 5.0V           │
                        │                 │
                     VERIFY ──NG──► FAIL  │
                   ALL BYTES              │
                        │OK               │
                      PASS                │
```
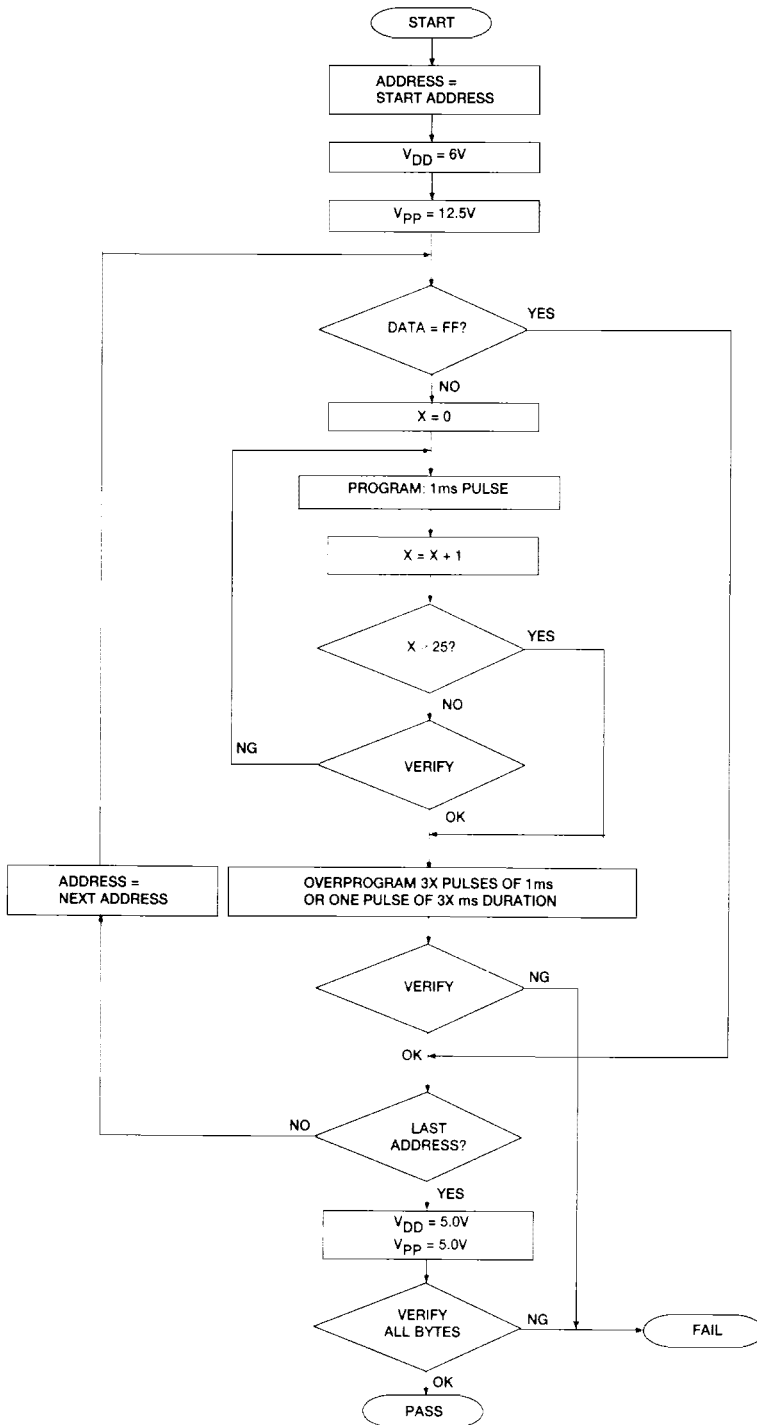
Electric Signature Mode

The electric signature mode allows one to read out a code from the TC54256AP/AF which identifies its manufacturer and device type.

The programming equipment may read out the manufacturer code and device code from the TC54256AP/AF by using this mode before programming and automatically set the programming voltage (V_{PP}) and algorithm.

The electric signature mode is set up when 12V is applied to address line A9 and the rest of the address lines are set to V_{IL} during a read operation. Data output under these conditions is the manufacturer code. The device code is output when address A0 is set to V_{IH}. These two codes possess an odd parity with the parity bit being the MSB (O7). The following table shows the electric signature of the TC54256AP/AF.

PINS SIGNATURE	A0 (10)	07 (19)	06 (18)	05 (17)	04 (16)	03 (15)	02 (13)	01 (12)	00 (11)	HEX. DATA
Manufacturer Code	V_{IL}	1	0	0	1	1	0	0	0	98
Device Code	V_{IH}	1	1	0	0	0	1	0	0	C4

Notes: A9 = 12V±0.5V
A1 ~ A8, A10 ~ A14. $\overline{CE}$. $\overline{OE}$ = V_{IL}

TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC.