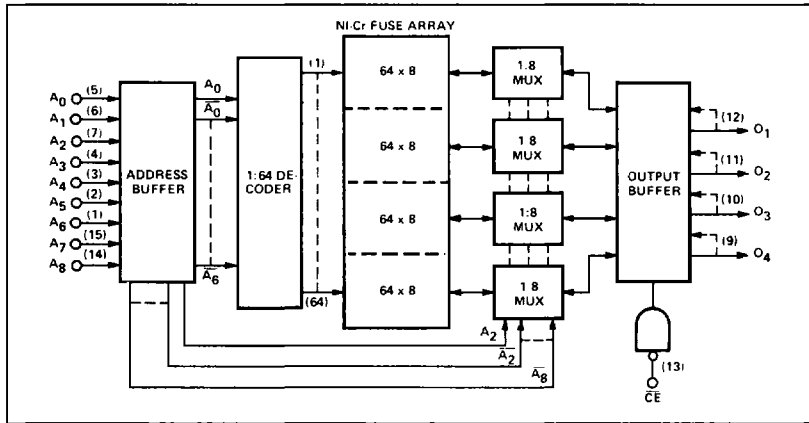
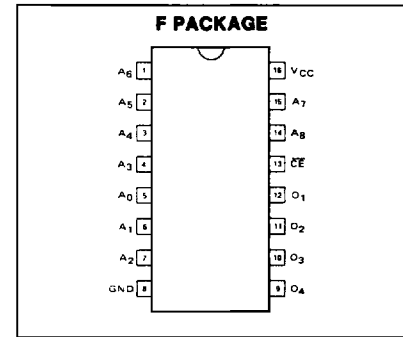


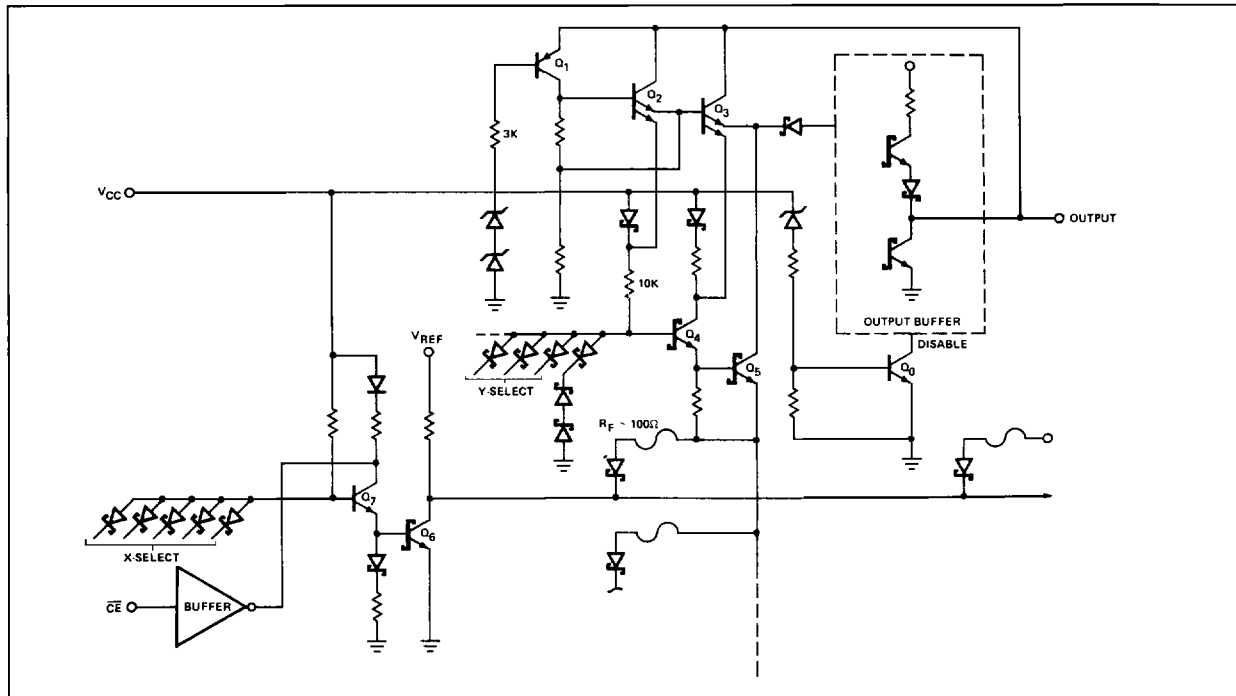
**BLOCK DIAGRAM**



**PIN CONFIGURATION**



**TYPICAL FUSING PATH**

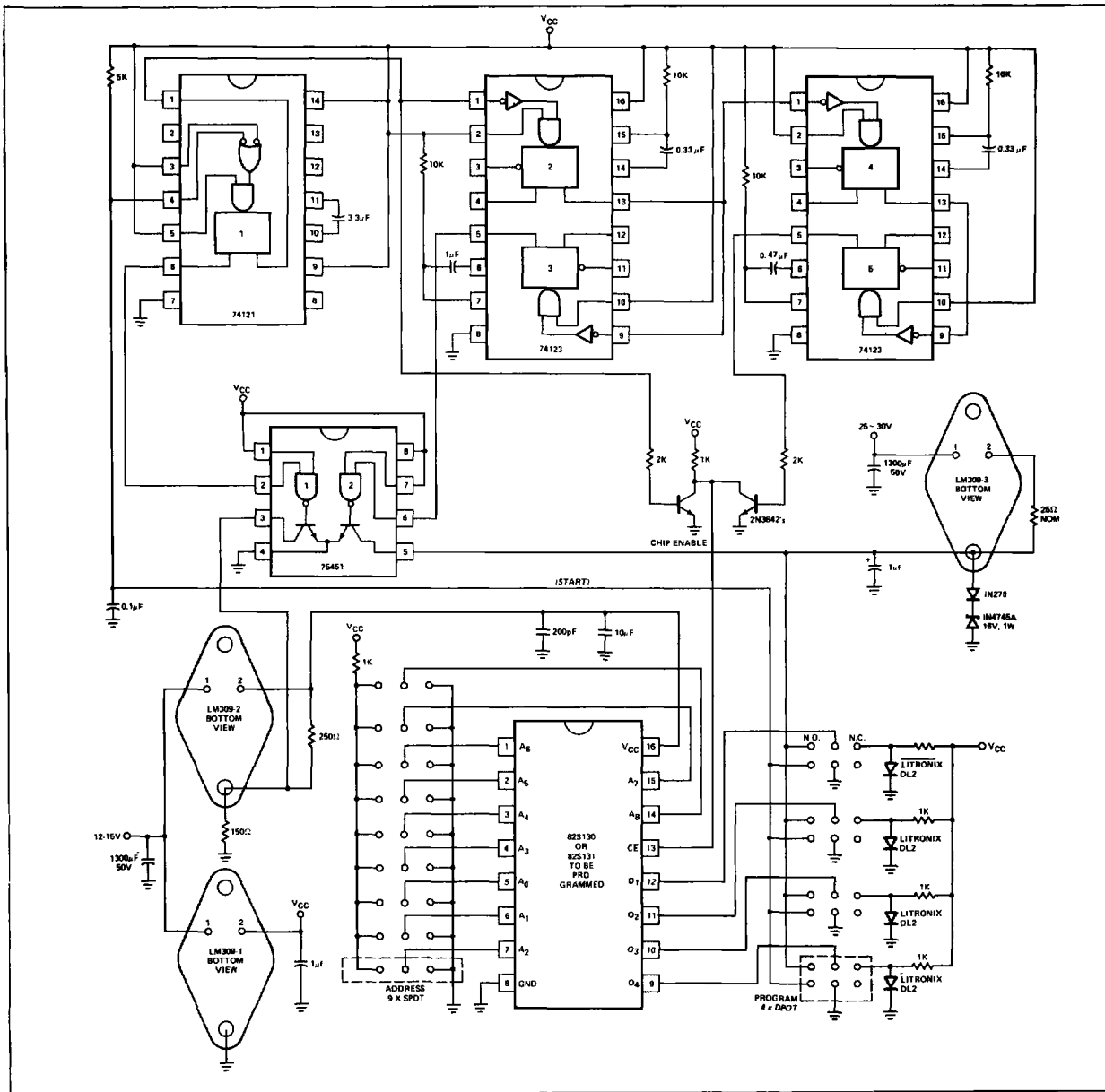


**AC ELECTRICAL CHARACTERISTICS** S82S130/131  $-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ ,  $4.5 \leq V_{CC} \leq 5.5\text{V}$   
 N82S130/131  $0^{\circ}\text{C} \leq T_A \leq +75^{\circ}\text{C}$ ,  $4.75 \leq V_{CC} \leq 5.25\text{V}$

PARAMETER	TEST CONDITIONS1	S82S130/131			N82S130/131			UNIT
		MIN	TYP2	MAX	MIN	TYP2	MAX	
<b>Propagation Delay</b>								
T <sub>AA</sub>	Address to Output	C <sub>L</sub> = 30pF	40	70		40	50	ns
T <sub>CD</sub>	Chip Disable to Output	R <sub>1</sub> = 270Ω	20	30		20	30	ns
T <sub>CE</sub>	Chip Enable to Output	R <sub>2</sub> = 600Ω	20	30		20	30	ns

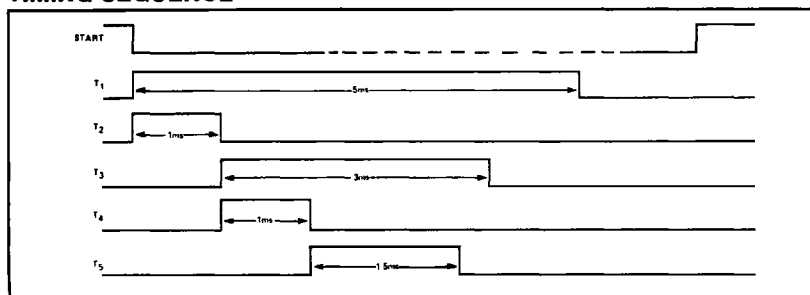
- NOTES:  
 1. Positive current is defined as into the terminal referenced.  
 2. Typical values are at V<sub>CC</sub> = 5.0V, T<sub>A</sub> = +25°C.

MANUAL PROGRAMMER



MEMORIES

TIMING SEQUENCE



**PROGRAMMING SPECIFICATIONS** (Testing of these limits may cause programming of device.)  $T_A = +25^\circ\text{C}$ 

PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
		MIN	TYP	MAX		
<b>Power Supply Voltage</b>						
$V_{CCP}^1$	To Program	$I_{CCP} = 350 \pm 50\text{mA}$ (Transient or steady state)	8.5	8.75	9.0	V
$V_{CCH}$	Upper Verify Limit		5.3	5.5	5.7	V
$V_{CCL}$	Lower Verify Limit		4.3	4.5	4.7	V
$V_S^3$	Verify Threshold		0.9	1.0	1.1	V
$I_{CCP}$	Programming Supply Current	$V_{CCP} = +8.75 \pm .25\text{V}$	300	350	400	mA
<b>Input Voltage</b>						
$V_{IH}$	Logical "1"		2.4		5.5	V
$V_{IL}$	Logical "0"		0	0.4	0.8	V
<b>Input Current</b>						
$I_{IH}$	Logical "1"	$V_{IH} = +5.5\text{V}$			50	$\mu\text{A}$
$I_{IL}$	Logical "0"	$V_{IL} = +0.4\text{V}$			-500	$\mu\text{A}$
$V_{OUT}^2$	Output Programming Voltage	$I_{OUT} = 200 \pm 20\text{mA}$ (Transient or steady state) $V_{OUT} = +17 \pm 1\text{V}$	16.0	17.0	18.0	V
$I_{OUT}$	Output Programming Current		180	200	220	mA
$T_R$	Output Pulse Rise Time		10		50	$\mu\text{s}$
$t_P$	$\overline{\text{CE}}$ Programming Pulse Width		1		2	ms
$t_D$	Pulse Sequence Delay		10			$\mu\text{s}$
$T_{PR}^5$	Programming Time	$V_{CC} = V_{CCP}$			2.5	sec
$T_{PS}$	Programming Pause	$V_{CC} = 0\text{V}$	5			sec
$\frac{T_{PR}^4}{T_{PR} + T_{PS}}$	Programming Duty Cycle				33	%

**PROGRAMMING PROCEDURE**

1. Terminate all device outputs with a  $10\text{k}\Omega$  resistor to  $V_{CC}$ .
2. Select the Address to be programmed, and raise  $V_{CC}$  to  $V_{CCP} = 8.75 \pm .25\text{V}$ .
3. After  $10\mu\text{s}$  delay, apply  $V_{OUT} = +17 \pm 1\text{V}$  to the output to be programmed. Program one output at the time.
4. After  $10\mu\text{s}$  delay, pulse the  $\overline{\text{CE}}$  input to logic "0" for 1 to 2 ms.
5. After  $10\mu\text{s}$  delay, remove  $+17\text{V}$  from the programmed output.
6. To verify programming, after  $10\mu\text{s}$  delay, lower  $V_{CC}$  to  $V_{CCH} = +5.5 \pm .2\text{V}$ , and apply a logic "0" level to the CE input. The programmed output should remain in the "1" state. Again, lower  $V_{CC}$  to  $V_{CCL} = +4.5 \pm .2\text{V}$ , and verify that the programmed output remains in the "1" state.
7. Raise  $V_{CC}$  to  $V_{CCP} = 8.75 \pm .25\text{V}$ , and repeat steps 3 through 6 to program other bits at the same address.
8. After  $10\mu\text{s}$  delay, repeat steps 2 through 7 to program all other address locations.

**NOTES:**

1. Bypass  $V_{CC}$  to GND with a  $0.01\mu\text{F}$  capacitor to reduce voltage spikes.
2. Care should be taken to insure the  $+17 \pm 1\text{V}$  output voltage is maintained during the entire fusing cycle. The recommended supply is a constant current source clamped at the specified voltage limit.
3.  $V_S$  is the sensing threshold of the PROM output voltage for a programmed bit. It normally constitutes the reference voltage applied to a comparator circuit to verify a successful fusing attempt.
4. Continuous fusing for an unlimited time is also allowed, provided that a 33% duty cycle is maintained. This may be accomplished by following each Program-Verify cycle with a Rest period ( $V_{CC} = 0\text{V}$ ) of 4ms.
5. On the first programming attempt (from cold start) a maximum limit of 5 sec. is allowed. In most cases, depending on the truth table, this will decrease total programming time.