Signetics

82HS187
82HS187A
8K-Bit TTL Bipolar PROM

Preliminary Specification

Bipolar Memory Products

DESCRIPTION

The 82HS187 is a programmable read only memory containing D-type, master slave data registers. The 82HS187 contains 1024 words of 8 bits each. The unprogrammed state is with all outputs at a High level and can be selectively programmed to a Low level by following the Signetics Generic II programming method. The output structure is Three-state for ease in connection to bus organized systems. The combination of on-chip registers and Three-state outputs will substantially reduce cost and size of pipelined microprogrammed systems and other designs where accessed PROM data is temporarily stored in a register.

All outputs will go into the Third state or Hi-Z condition whenever the asynchronous chip enable ($\overline{G}$) is High. The outputs are enabled when ($\overline{GS}$) is brought Low before the rising edge of the clock and ($\overline{G}$) is held Low. The ($\overline{GS}$) flip-flop is designed to power up in the third state or Hi-Z condition with the application of V_{CC}.
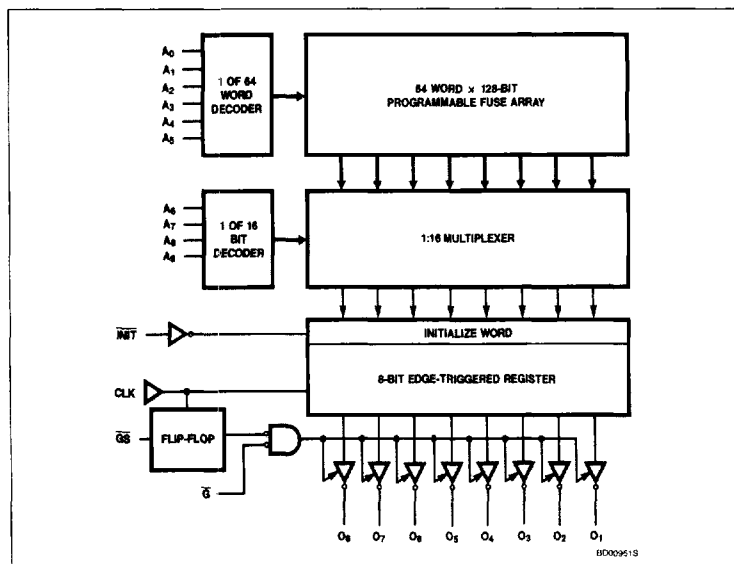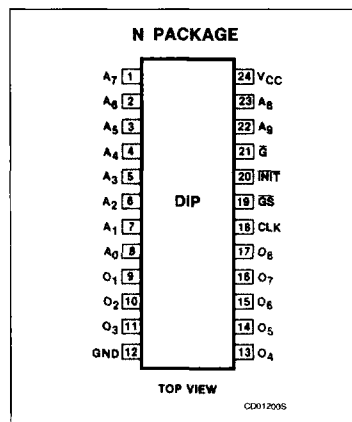
The 82HS187 also features an initialize function $\overline{INIT}$. The initialize function provides the user with an extra word of programmable memory which is accessed with single pin control by applying a Low on $\overline{INIT}$. The initialize function is asynchronous and is loaded into the output register and will appear at the outputs upon an application of a Low on $\overline{INIT}$ if the outputs are enabled and will control the state of the data registers independent of all other inputs. The unprogrammed state of the $\overline{INIT}$ is all ones.

Data is read from the PROM by first applying an address to inputs A_0 to A_9. During the set-up time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (Low to High transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

BLOCK DIAGRAM

PIN CONFIGURATION

N PACKAGE

	DIP	
A_7 [1]		[24] V_{CC}
A_6 [2]		[23] A_8
A_5 [3]		[22] A_9
A_4 [4]		[21] $\overline{G}$
A_3 [5]		[20] $\overline{INIT}$
A_2 [6]		[19] $\overline{GS}$
A_1 [7]		[18] CLK
A_0 [8]		[17] O_8
O_1 [9]		[16] O_7
O_2 [10]		[15] O_6
O_3 [11]		[14] O_5
GND [12]		[13] O_4

TOP VIEW

CD01200S

FEATURES

- **On-chip edge triggered registers**
- **Programmable register with asynchronous Initialize function**
- **24-pin 300 mil wide DIP package**
- **Read cycle "Address set-up plus clock to output delay"**
  - **N82HS187: 55ns max**
  - **N82HS187A: 45ns max**
- **Outputs: Three-state**
- **Unprogrammed outputs are High level**
- **Synchronous and asynchronous enables for word expansion**

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ORDERING CODE

DESCRIPTION	ORDER CODES
Plastic Dual Inline 300mil wide 24-pin	N82HS187 N • N82HS187A N
Plastic Leaded Chip Carrier 450mil sq 28-pin	N82HS187 A • N82HS187A A

ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	V_{dc}
V_{IN}	Input voltage	+5.5	V_{dc}
V_O	Output voltage Off-state	+5.5	V_{dc}
T_A T_{STG}	Temperature range Operating Storage	0 to +75 −65 to +150	°C

DC ELECTRICAL CHARACTERISTICS $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER	TEST CONDITIONS[1, 2]	LIMITS			UNIT
		Min	Typ[5]	Max	
Input voltage[2] V_{IL} Low V_{IH} High V_{IC} Clamp	$I_{IN} = -12mA$	2.0	−0.8	0.8 −1.2	V
Output voltage[2] V_{OL} Low V_{OH} High	$\overline{G}$, $\overline{GS}$ = Low $I_{OUT} = 16mA$ $I_{OUT} = -2mA$	2.4		0.5	V
Input current[1] I_{IL} Low I_{IH} High	$V_{IN} = 0.45V$ $V_{IN} = 5.5V$			−100 40	μA
Output current[1] I_{OZ} Hi-Z State I_{OS} Short circuit[3]	$\overline{G}$ = High, $V_{OUT} = 5.5V$ $\overline{G}$ = High, $V_{OUT} = 0.5V$ $\overline{G}$, $\overline{GS}$ = Low, $V_{OUT} = 0V$ High Stored	−15		40 −40 −70	μA mA
Supply current I_{CC}	$V_{CC} = 5.25V$		125	175	mA
Capacitance C_{IN} Input C_{OUT} Output	$\overline{G}$ = High, $V_{CC} = 5.0V$ $V_{IN} = 2.0V$ $V_{OUT} = 2.0V$		5 8		pF

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AC ELECTRICAL CHARACTERISTICS $R_1 = 270\Omega$, $R_2 = 600\Omega$, $C_L = 30pF$, $0°C \leqslant T_A \leqslant +75°C$, $4.75V \leqslant V_{CC} \leqslant 5.25V$

PARAMETER[4]		TO	FROM	N82HS187			N82HS187A			UNIT
				Min	Typ[5]	Max	Min	Typ	Max	
t_{CSA}	Set-up	CK	Address	35			30			ns
t_{CHA}	Hold			0			0			
t_{OC}	Delay	Output	CK			20	0		15	ns
t_{WC}	Width		CK	20	25		15	20		ns
t_{CSGS}	Set-up	CK	$\overline{GS}$	15			10			ns
t_{CHGS}	Hold			5			5			
t_{OIN}	Delay	Output	$\overline{INIT}$		12	30			25	ns
t_{CIN}	Recovery	CK	$\overline{INIT}$	20	9		15			ns
t_{WIN}	Width		$\overline{INIT}$	25			20			ns
t_{OG}	Delay	Output	$\overline{G}$		11	25			20	ns
t_{OZC}[6]	Delay	Output	CK		18	25			20	ns
t_{OZG}[6]	Delay	Output	$\overline{G}$		14	25			20	ns

NOTES:
1. Positive current is defined as into the terminal referenced.
2. All voltages with respect to network ground.
3. Duration of short circuit should not exceed 1 second.
4. Tested at an address cycle time of 1μs.
5. Typical values are at $V_{CC} = 5V$, $T_A = 25°C$.
6. Measured at a delta of 0.5V from Logic Level with $R_1 = 750\Omega$, $R_2 = 750\Omega$ and $C_L = 5pF$.

TEST LOAD CIRCUIT

All inputs: $t_r = t_f = 5ns$ (10% to 90%).
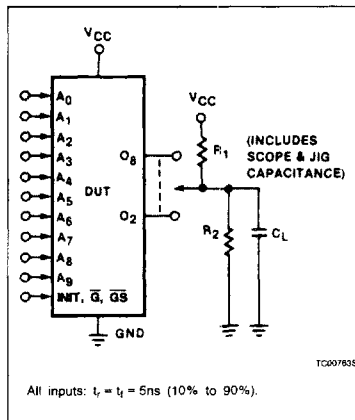
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VOLTAGE WAVEFORMS

NOTE:
All AC parameters are measured at 1.5V unless otherwise specified.

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