SYNCHRONOUS DRAM MODULE

MT4LSD(T)232U

FEATURES

* JEDEC pinout in a 100-pin, dual in-line memory module (DIMM)
* 8MB (2 Meg x 32)
* Utilizes 100 MHz SDRAM components
* Single +3.3V ±0.3V power supply
* Fully synchronous; all signals registered on positive edge of system clock
* Internal pipelined operation; column address can be changed every clock cycle
* Dual internal banks for hiding row access/precharge
* Programmable burst lengths; 1, 2, 4, 8 or full page
* Auto Precharge and Auto Refresh modes
* 64ms, 4,096-cycle refresh
* All inputs, outputs and clocks LVTTL-compatible
* Serial presence-detect (SPD)
* One-clock WRITE recovery (^{t}WR) version, two-clock (^{t}WR) not supported

OPTIONS — MARKING

* Components
  SOJ — D
  TSOP — DT
* Package
  100-pin DIMM (gold) — G
* Timing
  10ns cycle (≤100 MHz clock rate) — -10

KEY SDRAM COMPONENT TIMING PARAMETERS

SPEED GRADE	CLOCK FREQUENCY	ACCESS TIME		SETUP TIME	HOLD TIME
		*CL = 2	*CL = 3		
-10	100 MHz	9ns	7.5ns	3ns	1ns

*CL = CAS (READ) Latency

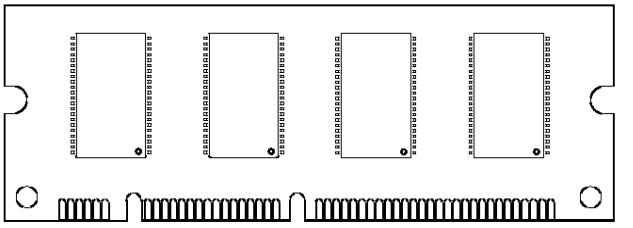
PART NUMBERS

PART NUMBER	CONFIGURATION	DEVICE PACKAGE
MT4LSD232UG-10_	2 Meg x 32	SOJ
MT4LSDT232UG-10_	2 Meg x 32	TSOP

Note: All part numbers end with a two-place code (not shown) designating component and PCB revisions. Consult factory for current revision codes. Example: MT4LSDT232UG-10C1.

PIN ASSIGNMENT (Front View)

100-Pin DIMM



PIN	FRONT	PIN	FRONT	PIN	BACK	PIN	BACK
1	Vss	26	Vss	51	Vss	76	Vss
2	DQ0	27	CKE0	52	DQ8	77	NC (CKE1)
3	DQ1	28	WE#	53	DQ9	78	NC
4	DQ2	29	S0#	54	DQ10	79	NC (S1#)
5	DQ3	30	S2#	55	DQ11	80	NC (S3#)
6	Vcc	31	Vcc	56	Vcc	81	Vcc
7	DQ4	32	NC	57	DQ12	82	NC
8	DQ5	33	NC	58	DQ13	83	NC
9	DQ6	34	NC	59	DQ14	84	NC
10	DQ7	35	NC	60	DQ15	85	NC
11	DQMB0#	36	Vss	61	DQMB1#	86	Vss
12	Vss	37	DQMB2#	62	Vss	87	DQMB3#
13	A0	38	DQ16	63	A1	88	DQ24
14	A2	39	DQ17	64	A3	89	DQ25
15	A4	40	DQ18	65	A5	90	DQ26
16	A6	41	DQ19	66	A7	91	DQ27
17	A8	42	Vcc	67	A9	92	Vcc
18	A10/AP	43	DQ20	68	BA0	93	DQ28
19	NC	44	DQ21	69	NC	94	DQ29
20	NC	45	DQ22	70	NC	95	DQ30
21	Vcc	46	DQ23	71	Vcc	96	DQ31
22	DU	47	Vss	72	RAS#	97	Vss
23	RFU	48	SDA	73	CAS#	98	SA0
24	RFU	49	SCL	74	RFU	99	SA1
25	CK0	50	Vcc	75	NC (CK1)	100	SA2

NOTE: Symbols in parentheses are not used on this module but may be used for other modules in this product family. They are for reference only.

GENERAL DESCRIPTION

The MT4LSD(T)232U is a high-speed CMOS, dynamic random-access 8MB solid-state memory organized in a x32 configuration. This module is configured as a dual bank with a synchronous interface (all signals are registered on the positive edge of the clock signal CK0). READ and WRITE accesses to the SDRAM module are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVE command which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA0 selects the bank; A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The module provides for programmable READ or WRITE burst terminate option. An auto precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence. The module uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures, but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the precharge cycles and provide seamless, high-speed random access operation.

The module is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided along with a power-saving power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAM modules offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic column-address generation, the ability to interleave between internal banks in order to hide precharge time and the capability to randomly change column addresses on each clock cycle during a burst access. For more information regarding the SDRAM operation, refer to the 16Mb SDRAM data sheet.

SERIAL PRESENCE-DETECT OPERATION

This module incorporates serial presence-detect (SPD). The SPD function is implemented using a 2,048 bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various DRAM organization and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device (DIMM) occur via a standard IIC bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA(2:0), which provide eight unique DIMM/EEPROM addresses.

SPD CLOCK AND DATA CONVENTIONS

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions (Figures 1 and 2).

SPD START CONDITION

All commands are preceded by the start condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SPD device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

SPD STOP CONDITION

All communications are terminated by a stop condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the SPD device into standby power mode.

SPD ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data (Figure 3).

The SPD device will always respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a WRITE operation have been selected, the SPD device will respond with an acknowledge after the receipt of each subsequent eight-bit word. In the read mode the SPD device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the stop condition to return to standby power mode.

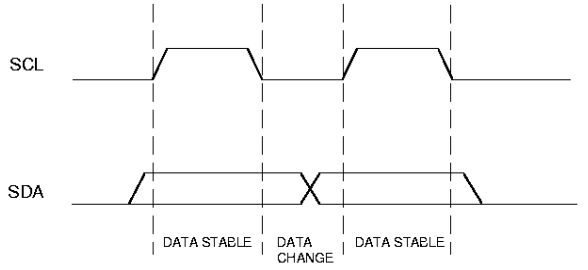


Figure 1
DATA VALIDITY

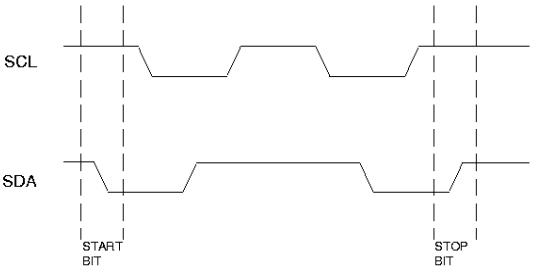


Figure 2
DEFINITION OF START AND STOP

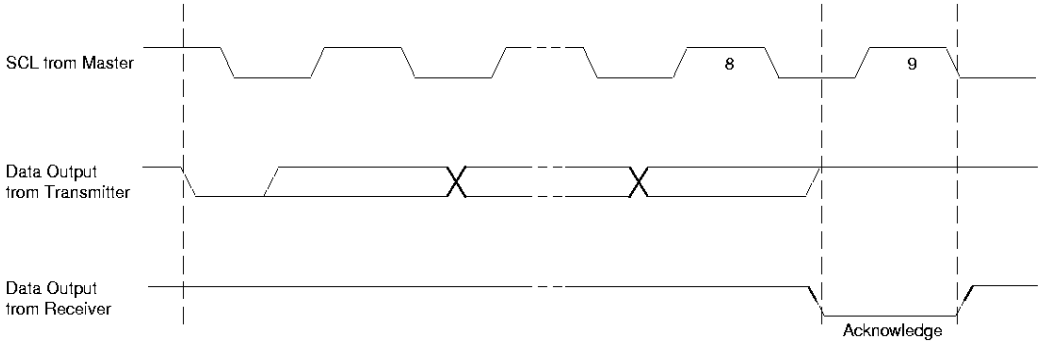
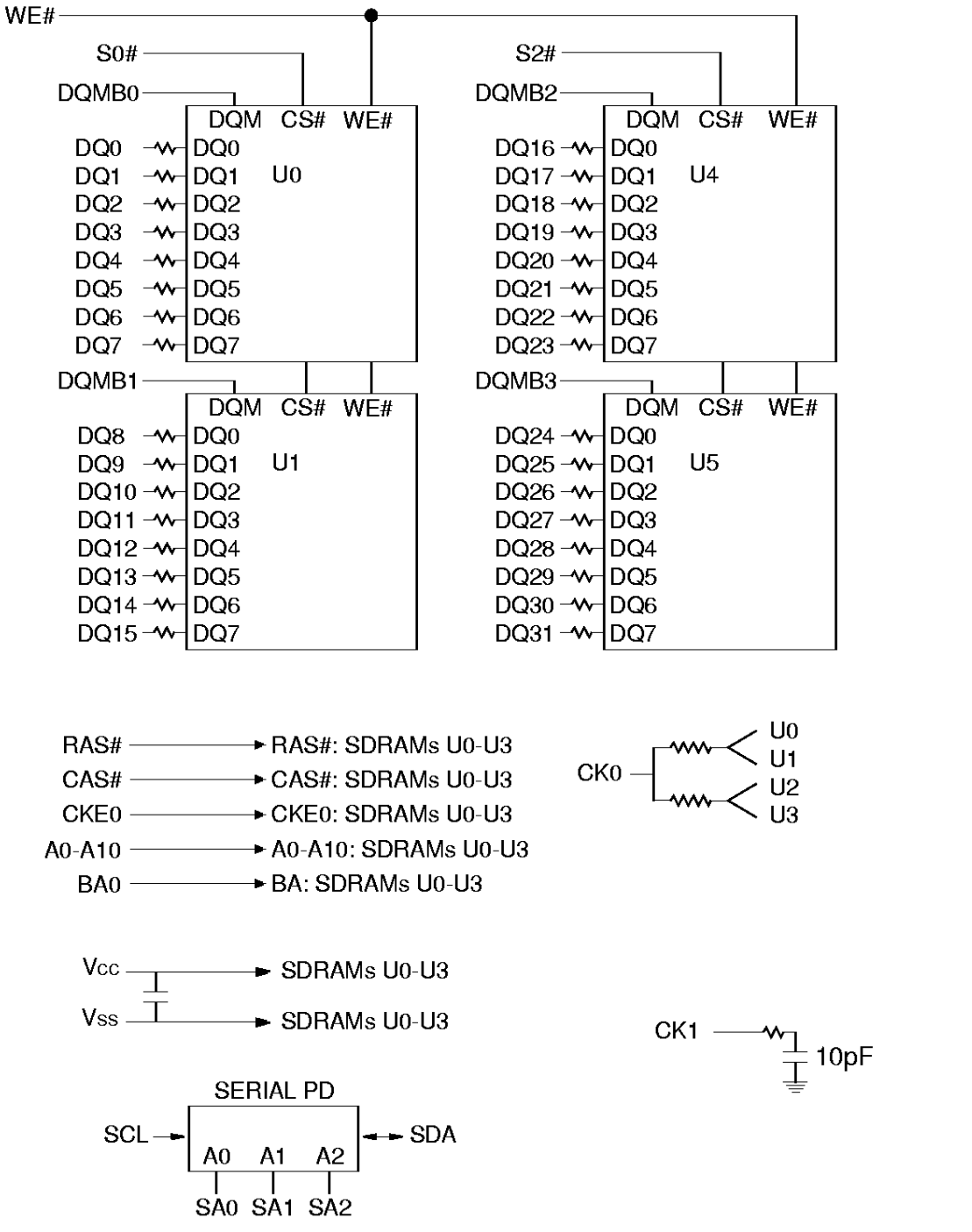


Figure 3
ACKNOWLEDGE RESPONSE FROM RECEIVER

FUNCTIONAL BLOCK DIAGRAM
MT4LSD(T)232U (8MB)



NOTE: ALL RESISTOR VALUES ARE 10 OHMS. U0-U3 = MT48LC2M8A1 SDRAMs

PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
28, 72, 73	WE#, RAS#, CAS#	Input	Command Inputs: WE#, RAS# and CAS# (along with S0#-S3#) define the command being entered.
25	CK0	Input	Clock: CK0 is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CK. CK also increments the internal burst counter and controls the output registers.
27	CKE0	Input	Clock Enable: CKE0 activates (HIGH) and deactivates (LOW) the CK0 signal. Deactivating the clock provides POWER-DOWN and SELF REFRESH operation (all banks idle), or CLOCK SUSPEND operation (burst access in progress). CKE0 is synchronous except after the device enters power-down and self refresh modes, where CKE0 becomes asynchronous until after exiting the same mode. The input buffers, including CK0, are disabled during power-down and self refresh modes, providing low standby power.
29, 30	S0#, S2#	Input	Chip Select: S0# and S2# enable (registered LOW) and disable (registered HIGH) the command decoder. All commands are masked when S0# or S2# are registered HIGH. S0# and S2# are considered part of the command code.
11, 37, 61, 87	DQMB0-DQMB3	Input/ Output	Input/Output Mask: DQMB is an input mask signal for WRITE accesses and an output enable signal for READ accesses. Input data is masked when DQMB is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (after a two-clock latency) when DQMB is sampled HIGH during a READ cycle.
68	BA0	Input	Bank Address: BA0 defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA0 is also used to program the 12th bit of the mode register.
13-18, 63-67	A0-A10/AP	Input	Address Inputs: A0-A10 are sampled during the ACTIVE command (row address A0-A10) and READ/WRITE command (column address A0-A8 with A10 defining auto precharge) to select one location out of the 1Mb available in the respective bank. A10 is sampled during a PRECHARGE command to determine if both banks are to be precharged (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE REGISTER command.
2-5, 7-10, 38-41, 43-46, 52-55, 57-60, 88-91, 93-96	DQ0-DQ31	Input/ Output	Data I/O: Data bus.
6, 21, 31, 42, 50, 56, 71, 81, 92	Vcc	Supply	Power Supply: +3.3V ±0.3V

PIN DESCRIPTIONS (continued)

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
1, 12, 26, 36, 47, 51, 62, 76, 86, 97	Vss	Supply	Ground
48	SDA	Input/Output	Serial Presence-Detect Data: SDA is a bidirectional pin used to transfer addresses and data into and data out of the presence-detect portion of the module.
49	SCL	Input	Serial Clock for Presence-Detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
98-100	SA0-SA2	Input	Presence-Detect Address Inputs: These pins are used to configure the presence-detect device.
23, 24, 74	RFU	—	Reserved for Future Use: These pins should be left unconnected.
22	DU	—	Don't Use: This pin is not connected on this module but is an assigned pin on the compatible DRAM version.

SERIAL PRESENCE-DETECT MATRIX

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
0	NUMBER OF BYTES USED BY MICRON	128		1	0	0	0	0	0	0	0	80
1	TOTAL NUMBER OF SPD MEMORY BYTES	256		0	0	0	0	1	0	0	0	0
2	MEMORY TYPE	SDRAM		0	0	0	0	0	1	0	0	04
3	NUMBER OF ROW ADDRESSES	11		0	0	0	0	1	0	1	1	0B
4	NUMBER OF COLUMN ADDRESSES	9		0	0	0	0	1	0	0	1	09
5	NUMBER OF BANKS	1		0	0	0	0	0	0	0	1	01
6	MODULE DATA WIDTH	32		0	0	1	0	0	0	0	0	20
7	MODULE DATA WIDTH (continued)	0		0	0	0	0	0	0	0	0	00
8	MODULE VOLTAGE INTERFACE LEVELS	LVTTL		0	0	0	0	0	0	0	1	01
9	SDRAM CYCLE TIME (HIGHEST CAS# LATENCY)	10	^{t}CK	1	0	1	0	0	0	0	0	A0
10	SDRAM ACCESS FROM CLOCK (HIGHEST CAS# LATENCY)	7.5	^{t}AC	0	1	1	1	0	1	0	1	75
11	MODULE CONFIGURATION TYPE	NONPARITY		0	0	0	0	0	0	0	0	00
12	REFRESH RATE/TYPE	15.6µs/SELF		1	0	0	0	0	0	0	0	80
13	SDRAM WIDTH (PRIMARY SDRAM)	8		0	0	0	0	1	0	0	0	08
14	ERROR CHECKING SDRAM DATA WIDTH	NONE		0	0	0	0	0	0	0	0	00
15	MIN. CLOCK DELAY FROM BACK-TO-BACK RANDOM COLUMN ADDRESSES	1	^{t}CCD	0	0	0	0	0	0	0	1	01
16	BURST LENGTHS SUPPORTED	1, 2, 4, 8, PAGE		1	0	0	0	1	1	1	1	8F
17	NUMBER OF BANKS ON SDRAM DEVICE	2		0	0	0	0	0	0	1	0	02
18	CAS# LATENCIES SUPPORTED	1, 2, 3		0	0	0	0	0	1	1	1	07
19	CS# LATENCY	0		0	0	0	0	0	0	0	1	01
20	WE# LATENCY	0		0	0	0	0	0	0	0	1	01
21	SDRAM MODULE ATTRIBUTES	NONBUFFERED		0	0	0	0	0	0	0	0	00
22	SDRAM DEVICE ATTRIBUTES: GENERAL	0E		0	0	0	0	1	1	1	0	0E
23	SDRAM CYCLE TIME (2ND HIGHEST CAS LATENCY)	15	^{t}CK	1	1	1	1	0	0	0	0	F0
24	SDRAM ACCESS FROM CLK (2ND HIGHEST CAS LATENCY)	9	^{t}AC	1	0	0	1	0	0	0	0	90
25	SDRAM CYCLE TIME (3RD HIGHEST CAS LATENCY)	30	^{t}CK	0	1	1	1	1	0	0	0	78
26	SDRAM ACCESS FROM CLK (3RD HIGHEST CAS LATENCY)	27	^{t}AC	0	1	1	0	1	1	0	0	6C
27	MINIMUM ROW PRECHARGE TIME	30	^{t}RP	0	0	0	1	1	1	1	0	1E
28	MINIMUM ROW ACTIVE TO ROW ACTIVE	20	^{t}RRD	0	0	0	1	0	1	0	0	14
29	MINIMUM RAS# TO CAS# DELAY	30	^{t}RCD	0	0	0	1	1	1	1	0	1E
30	MINIMUM RAS# PULSE WIDTH	60	^{t}RAS	0	0	1	1	1	1	0	0	3C
31	MODULE BANK DENSITY	8MB		0	0	0	0	0	0	1	0	02
32	COMMAND/ADDRESS SETUP	3	^{t}AS, ^{t}CMS	0	0	1	1	0	0	0	0	30
33	COMMAND/ADDRESS HOLD	1	^{t}AH, ^{t}CMH	0	0	0	1	0	0	0	0	10
34	DATA SIGNAL INPUT SETUP	3	^{t}DS	0	0	1	1	0	0	0	0	30
35	DATA SIGNAL INPUT HOLD	1	^{t}DH	0	0	0	1	0	0	0	0	10
36-61	RESERVED BYTES	-		-	-	-	-	-	-	-	-	--

NOTE: 1. "**1**"/"0": Serial Data, "driven to HIGH"/"driven to LOW."

SERIAL PRESENCE-DETECT (contined)

BYTE	DESCRIPTION	ENTRY (VERSION)	SYMBOL	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	HEX
62	SPD REVISION	REV. 2		0	0	0	0	0	0	1	0	02
63	CHECKSUM FOR BYTES 0-62			0	1	1	1	1	1	0	0	7C
64	MANUFACTURER'S JEDEC ID CODE	MICRON		0	0	1	0	1	1	0	0	2C
65-71	MANUFACTURER'S JEDEC CODE (CONT.)			1	1	1	1	1	1	1	1	FF
72	MANUFACTURING LOCATION			0	0	0	0	0	0	0	1	01
				0	0	0	0	0	0	1	0	02
				0	0	0	0	0	0	1	1	03
				0	0	0	0	0	1	0	0	04
				0	0	0	0	0	1	0	1	05
				0	0	0	0	0	1	1	0	06
73-90	MODULE PART NUMBER (ASCII)			x	x	x	x	x	x	x	x	xx
91	PCB REVSION CODE	A		0	0	0	0	0	0	0	1	01
		B		0	0	0	0	0	0	1	0	02
		C		0	0	0	0	0	0	1	1	03
		D		0	0	0	0	0	1	0	0	04
92	REVISION CODE (CONT.)	0		0	0	0	0	0	0	0	0	00
93	YEAR OF MANUFACTURE IN BCD			x	x	x	x	x	x	x	x	xx
94	WEEK OF MANUFACTURE IN BCD			x	x	x	x	x	x	x	x	xx
95-98	MODULE SERIAL NUMBER			x	x	x	x	x	x	x	x	xx
99-127	MANUFACTURE SPECIFIC DATA (RSVD)			-	-	-	-	-	-	-	-	--

COMMANDS

Truth Table 1 provides a quick reference of available commands.

TRUTH TABLE 1 – Commands and DQMB Operation

(Notes: 1)

NAME (FUNCTION)	CS#	RAS#	CAS#	WE#	DQMB	ADDR	DQs	NOTES
COMMAND INHIBIT (NOP)	H	X	X	X	X	X	X	
NO OPERATION (NOP)	L	H	H	H	X	X	X	
ACTIVE (Select bank and activate row)	L	L	H	H	X	Bank/Row	X	3
READ (Select bank and column, and start READ burst)	L	H	L	H	X	Bank/Col	X	4
WRITE (Select bank and column, and start WRITE burst)	L	H	L	L	X	Bank/Col	VALID	4
BURST TERMINATE	L	H	H	L	X	X	Active	
PRECHARGE (Deactivate row in bank or banks)	L	L	H	L	X	Code	X	5
AUTO REFRESH or SELF REFRESH (enter self refresh mode)	L	L	L	H	X	X	X	6, 7
LOAD MODE REGISTER	L	L	L	L	X	Op-code	X	2
Write enable/output enable	-	-	-	-	L	-	Active	8
Write inhibit/output High-Z	-	-	-	-	H	-	High-Z	8

NOTE:
1. CKE is HIGH for all commands shown except SELF REFRESH.
2. A0 through A10 and BA0 define the op-code written to the mode register.
3. A0 through A10 provide row address and BA0 determines which bank is made active (BA0 LOW = Bank 0 and BA0 HIGH = Bank 1).
4. A0 through A8 provide column address; A10 HIGH enables the auto precharge feature (nonpersistent) while A10 LOW disables the auto precharge feature; BA0 determines which bank is being read from or written to (BA0 LOW = Bank 0 and BA0 HIGH = Bank 1).
5. A10 LOW: BA0 determines bank being precharged (BA0 LOW = Bank 0 and BA0 HIGH = Bank 1). A10 HIGH: both banks precharged and BA0 is a "don't care."
6. This command is AUTO REFRESH if CKE is HIGH, SELF REFRESH if CKE is LOW.
7. Internal refresh counter controls row addressing; all inputs and I/Os are "don't care" except for CKE.
8. Activates or deactivates the DQs during WRITEs (zero-clock delay) and READs (two-clock delay).

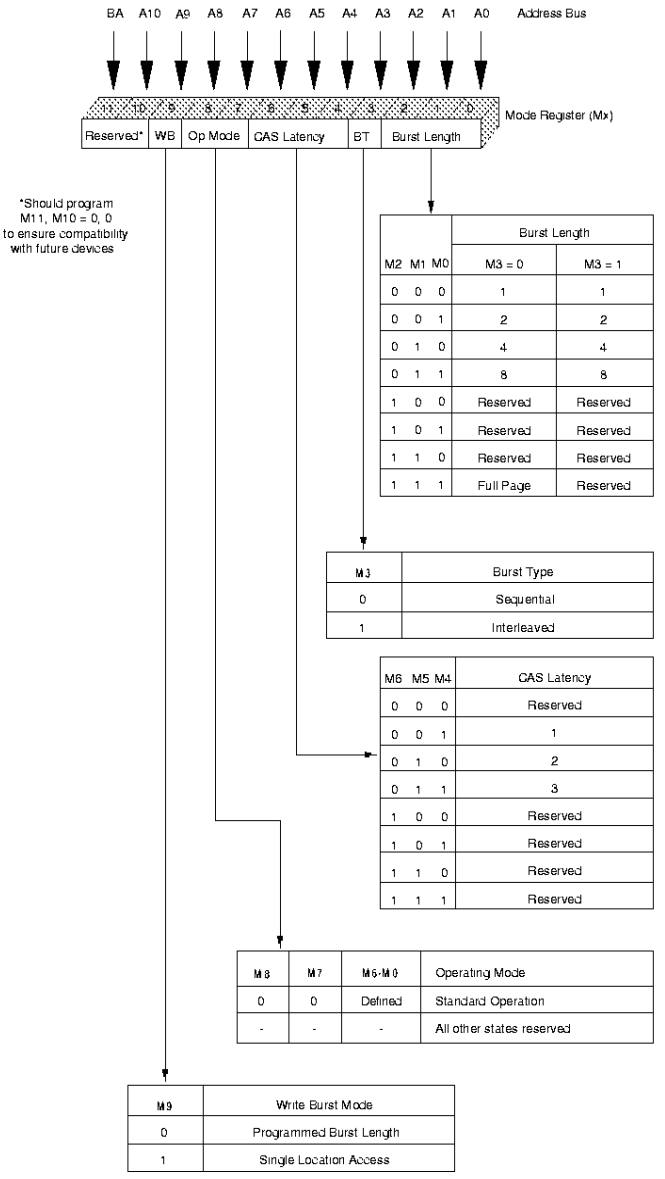


Figure 1
MODE REGISTER DEFINITION

Table 1
BURST DEFINITION

Burst Length	Starting Column Address	Order of Accesses within a Burst	
		Type = Sequential	Type = Interleaved
2	A0		
	0	0-1	0-1
	1	1-0	1-0
4	A1 A0		
	0 0	0-1-2-3	0-1-2-3
	0 1	1-2-3-0	1-0-3-2
	1 0	2-3-0-1	2-3-0-1
	1 1	3-0-1-2	3-2-1-0
8	A2 A1 A0		
	0 0 0	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7
	0 0 1	1-2-3-4-5-6-7-0	1-0-3-2-5-4-7-6
	0 1 0	2-3-4-5-6-7-0-1	2-3-0-1-6-7-4-5
	0 1 1	3-4-5-6-7-0-1-2	3-2-1-0-7-6-5-4
	1 0 0	4-5-6-7-0-1-2-3	4-5-6-7-0-1-2-3
	1 0 1	5-6-7-0-1-2-3-4	5-4-7-6-1-0-3-2
	1 1 0	6-7-0-1-2-3-4-5	6-7-4-5-2-3-0-1
	1 1 1	7-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0
Full Page (512)	n = A0-A8 (location 0-511)	Cn, Cn + 1, Cn + 2 Cn + 3, Cn + 4... ...Cn - 1, Cn...	Not Supported

NOTE:
1. For a burst length of two, A1-A8 select the block-of-two burst; A0 selects the starting column within the block.
2. For a burst length of four, A2-A8 select the block-of-four burst; A0-A1 select the starting column within the block.
3. For a burst length of eight, A3-A8 select the block-of-eight burst; A0-A2 select the starting column within the block.
4. For a full-page burst, the full row is selected, and A0-A8 select the starting column.
5. Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.
6. For a burst length of one, A0-A8 select the unique column to be accessed, and mode register bit M3 is ignored.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} Supply Relative to V_{SS} ..... -1V to +4.6V
Voltage on Inputs, NC or I/O Pins
Relative to V_{SS} ..... -1V to +4.6V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +125°C
Power Dissipation 4W
Short Circuit Output Current 50mA

*Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(Notes: 1, 6) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION		SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V_{CC}	3	3.6	V	
Input High (Logic 1) Voltage: All inputs		V_{IH}	2	V_{CC} + 0.3	V	
Input Low (Logic 0) Voltage: All inputs		V_{IL}	-0.3	0.8	V	
INPUT LEAKAGE CURRENT: Any input 0V ≤ V_{IN} ≤ V_{CC}	RAS#, CAS#, A0-A10, BA0, WE#, CK0, CKE0	I_{I1}	-20	20	µA	
(All other pins not under test = 0V)	S0#, S2#	I_{I2}	-10	10	µA	
OUTPUT LEAKAGE CURRENT: DQs are disabled; 0V ≤ V_{OUT} ≤ V_{CC}	DQ0-DQ31, DQMB0-DQMB3	I_{OZ}	-5	5	µA	
OUTPUT LEVELS: Output High Voltage (I_{OUT} = -2mA)		V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 2mA)		V_{OL}		0.4	V	

Icc OPERATING CONDITIONS AND MAXIMUM LIMITS

(Notes: 1, 6, 11, 13) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	SIZE	MAX -10	UNITS	NOTES
OPERATING CURRENT: Active mode; Burst = 2; READ or WRITE; $^tRC \geq {}^tRC$ (MIN); CAS latency = 3	I_{CC1}	8MB	360	mA	3,18,19
STANDBY CURRENT: Power-down mode; ^tCK = 15ns; CKE ≤ V_{IL} (MAX); All banks idle	I_{CC2}	8MB	8	mA	
STANDBY CURRENT: CS# ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); ^tCK = 15ns; All banks idle	I_{CC3}	8MB	120	mA	12, 19
STANDBY CURRENT: CS# ≥ V_{IH} (MIN); CKE ≥ V_{IH} (MIN); ^tCK = 15ns; All banks active after ^tRCD met; No accesses in progress	I_{CC4}	8MB	160	mA	12, 19
OPERATING CURRENT: Burst mode; Continuous burst; READ or WRITE; ^tCK = 15ns; All banks active; CAS latency = 3	I_{CC5}	8MB	340	mA	3,18,19
AUTO REFRESH CURRENT: $^tRC \geq {}^tRC$ (MIN); CAS latency = 3	I_{CC6}	8MB	340	mA	3,18,19
SELF REFRESH CURRENT: CKE ≤ 0.2V	I_{CC7}	8MB	8	mA	4

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A10, BA0, RAS#, CAS#, WE#, CK0, CKE0	C_{I1}	26	pF	2
Input Capacitance: S0#, S2#	C_{I2}	14	pF	2
Input Capacitance: DQMB0#-DQMB7#	C_{I3}	8	pF	2
Input Capacitance: SCL, SA0-SA2	C_{I4}	6	pF	2
Input/Output Capacitance: DQ0-DQ31, SDA	C_{IO}	9	pF	2

SDRAM COMPONENT* AC ELECTRICAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 11)

AC CHARACTERISTICS			-10			
PARAMETER	CAS LATENCY	SYMBOL	MIN	MAX	UNITS	NOTES
Access time from CLK (positive edge)	3	^tAC		7.5	ns	
	2	^tAC		9	ns	
	1	^tAC		27	ns	
Address hold time		^tAH	1		ns	
Address setup time		^tAS	3		ns	
CLK high-level width		^tCH	3.5		ns	
CLK low-level width		^tCL	3.5		ns	
Clock cycle time	3	^tCK	10		ns	
	2	^tCK	15		ns	
	1	^tCK	30		ns	
CKE hold time		^tCKH	1		ns	
CKE setup time		^tCKS	3		ns	
CS#, RAS#, CAS#, WE#, DQM hold time		^tCMH	1		ns	
CS#, RAS#, CAS#, WE#, DQM setup time		^tCMS	3		ns	
Data-in hold time		^tDH	1		ns	
Data-in setup time		^tDS	3		ns	
Data-out high-impedance time	3	^tHZ		8	ns	10
	2	^tHZ		10	ns	10
	1	^tHZ		15	ns	10
Data-out low-impedance time		^tLZ	2		ns	
Data-out hold time		^tOH	3		ns	
ACTIVE to PRECHARGE command period		^tRAS	60	120K	ns	
AUTO REFRESH and ACTIVE to ACTIVE command period		^tRC	90		ns	
ACTIVE to READ or WRITE delay		^tRCD	30		ns	
Refresh period (4,096 cycles)		^tREF		64	ms	7
PRECHARGE command period		^tRP	30		ns	
ACTIVE bank A to ACTIVE bank B command period		^tRRD	20		ns	
Transition time		^tT	0.3	10	ns	
WRITE recovery time		^tWR	1		^tCK	23
Exit SELF REFRESH to ACTIVE command		^tXSR	96		ns	20

*Specifications for the SDRAM components used on the module.

AC FUNCTIONAL CHARACTERISTICS

(Notes: 5, 6, 7, 8, 9, 11)

PARAMETER	CAS LATENCY	SYMBOL	-10	UNITS	NOTES
READ/WRITE command to READ/WRITE command		^{t}CCD	1	^{t}CK	17
CKE to clock disable or power-down entry mode		^{t}CKED	1	^{t}CK	14
CKE to clock enable or power-down exit setup mode		^{t}PED	1	^{t}CK	14
DQM to input data delay		^{t}DQD	0	^{t}CK	17
DQM to data mask during WRITEs		^{t}DQM	0	^{t}CK	17
DQM to data high-impedance during READs		^{t}DQZ	2	^{t}CK	17
WRITE command to input data delay		^{t}DWD	0	^{t}CK	17
Data-in to ACTIVATE command		^{t}DAL	3	^{t}CK	15
Data-in to precharge		^{t}DPL	1	^{t}CK	16,23
Last data-in to BURST STOP command		^{t}BDL	0	^{t}CK	17
Last data-in to new READ/WRITE command		^{t}CDL	1	^{t}CK	17
Last data-in to PRECHARGE command		^{t}RDL	1	^{t}CK	17,23
LOAD MODE REGISTER command to command		^{t}MRD	2	^{t}CK	17
Data-out to high-impedance from PRECHARGE command	3	^{t}ROH	3	^{t}CK	17
	2	^{t}ROH	2	^{t}CK	17
	1	^{t}ROH	1	^{t}CK	17

SERIAL PRESENCE-DETECT EEPROM DC OPERATING CONDITIONS

(Notes: 1) (V_{CC} = +3.3V ±0.3V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	3	3.6	V	
Input High (Logic 1) Voltage: All inputs	V_{IH}	V_{CC} × 0.7	V_{CC} + 0.5	V	
Input Low (Logic 0) Voltage: All inputs	V_{IL}	-1	V_{CC} × 0.3	V	
OUTPUT LOW VOLTAGE: I_{OUT} = 3mA	V_{OL}		0.4	V	
INPUT LEAKAGE CURRENT: V_{IN} = GND to V_{CC}	I_{LI}		10	µA	
OUTPUT LEAKAGE CURRENT: V_{OUT} = GND to V_{CC}	I_{LO}		10	µA	
STANDBY CURRENT: SCL = SDA = V_{CC} - 0.3V; All other inputs = GND or 3.3V +10%	I_{SB}		30	µA	
POWER SUPPLY CURRENT: SCL clock frequency = 100 KHz	I_{CC}		2	mA	

SERIAL PRESENCE-DETECT EEPROM AC ELECTRICAL CHARACTERISTICS

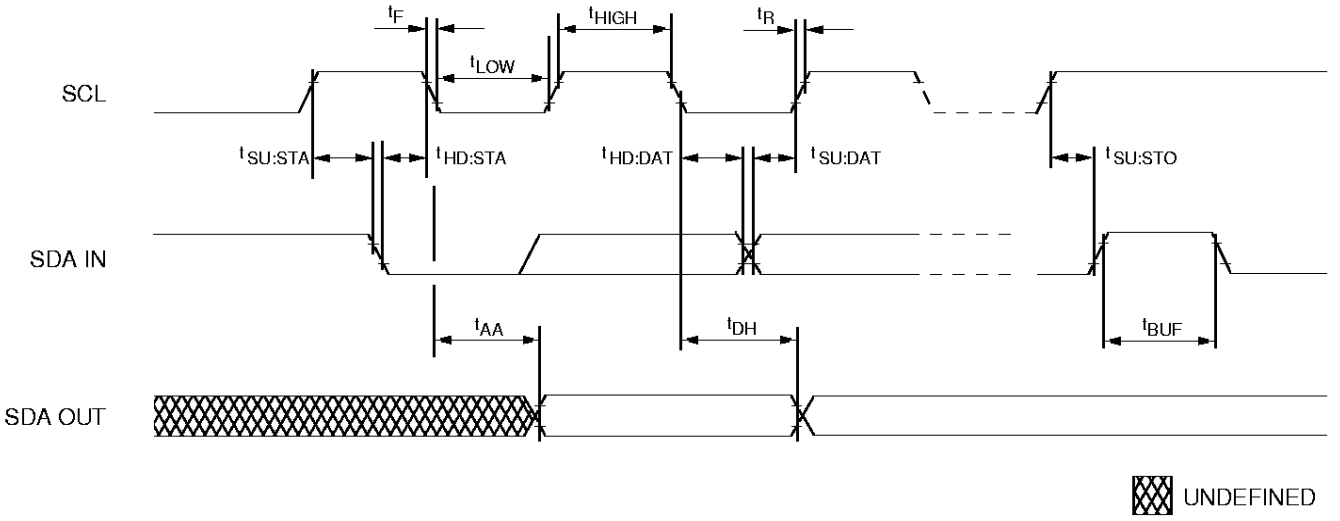
(Notes: 1) (V_{CC} = +3.3V ±0.3V)

AC CHARACTERISTICS					
PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
SCL LOW to SDA data-out valid	^tAA	0.3	3.5	µs	
Time the bus must be free before a new transition can start	^tBUF	4.7		µs	
Data-out hold time	^tDH	300		ns	
SDA and SCL fall time	^tF		300	ns	
Data-in hold time	$^tHD:DAT$	0		µs	
Start condition hold time	$^tHD:STA$	4		µs	
Clock HIGH period	^tHIGH	4		µs	
Noise suppression time constant at SCL, SDA inputs	^tI		100	ns	
Clock LOW period	^tLOW	4.7		µs	
SDA and SCL rise time	^tR		1	µs	
SCL clock frequency	^tSCL		100	KHz	
Data-in setup time	$^tSU:DAT$	250		ns	
Start condition setup time	$^tSU:STA$	4.7		µs	
Stop condition setup time	$^tSU:STO$	4.7		µs	
WRITE cycle time	^tWRC		10	ms	22

NOTES

1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = +3.3V ±0.3V; f = 1 MHz.
3. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
4. Enables on-chip refresh and address counters.
5. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \leq T_A \leq 70°C$) is ensured.
6. An initial pause of 100µs is required after power-up, followed by two AUTO REFRESH commands before proper device operation is ensured. The two AUTO REFRESH command wake-ups should be repeated any time the ^{t}REF refresh requirement is exceeded.
7. AC characteristics assume ^{t}T = 1ns.
8. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
9. Outputs measured at 1.4V with equivalent load:
10. ^{t}HZ defines the time at which the output achieves the open circuit condition; it is not a reference to V_{OH} or V_{OL}. The last valid data element will meet ^{t}OH before going High-Z.
11. AC timing tests have V_{IL} = 0V and V_{IH} = 3V with timing referenced to 1.4V crossover point.
12. Other input signals are allowed to transition no more than once in any 30ns period and are otherwise at valid V_{IH} or V_{IL} levels.
13. I_{CC} specifications are tested after the device is properly initialized.
14. Timing actually specified by ^{t}CKS; clock(s) specified as a reference only at minimum cycle rate.
15. Timing actually specified by ^{t}WR plus ^{t}RP; clock(s) specified as a reference only at minimum cycle rate.
16. Timing actually specified by ^{t}WR.
17. Clocks required specified by JEDEC functionality and not dependent on any timing parameter.
18. The I_{CC} current will decrease as the CAS latency is reduced. This is due to the fact that the maximum cycle rate is slower as the CAS latency is reduced.
19. Address transitions average one transition every 30ns.
20. CLK must be toggled a minimum of two times during this period.
21. Based on ^{t}CK = 100 MHz for -10.
22. The SPD EEPROM WRITE cycle time (^{t}WRC) is the time from a valid stop condition of a WRITE sequence to the end of the EEPROM internal erase/program cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistor, and the EEPROM does not respond to its slave address.
23. It is recommended that the DRAM controller use two clocks for ^{t}WR to support future design requirements.

SPD EEPROM

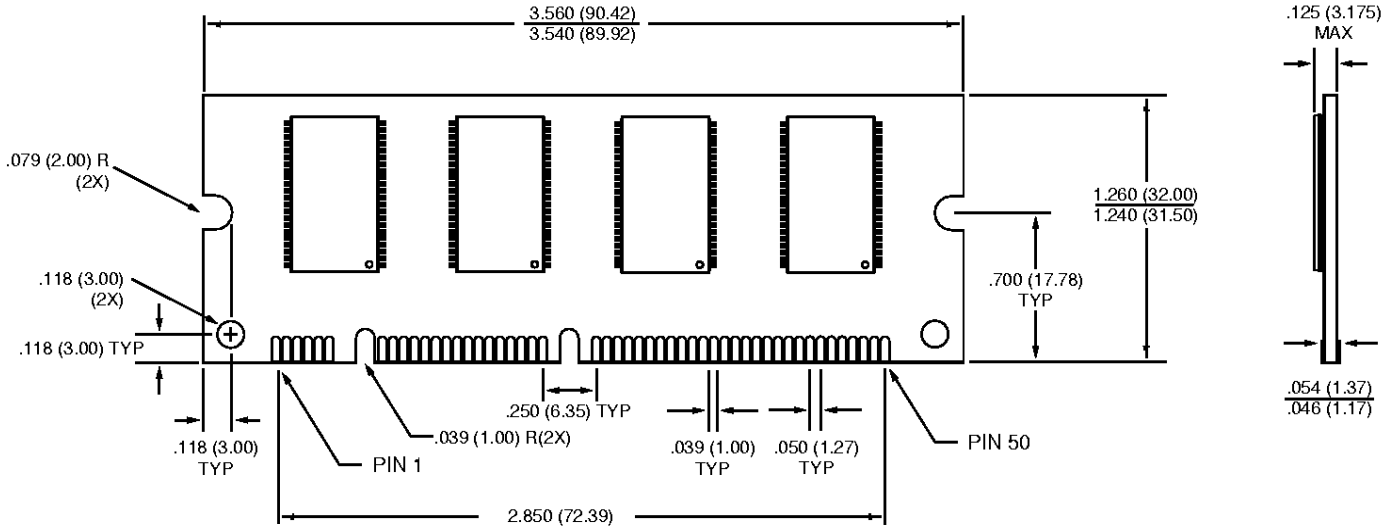


SERIAL PRESENCE-DETECT EEPROM TIMING PARAMETERS

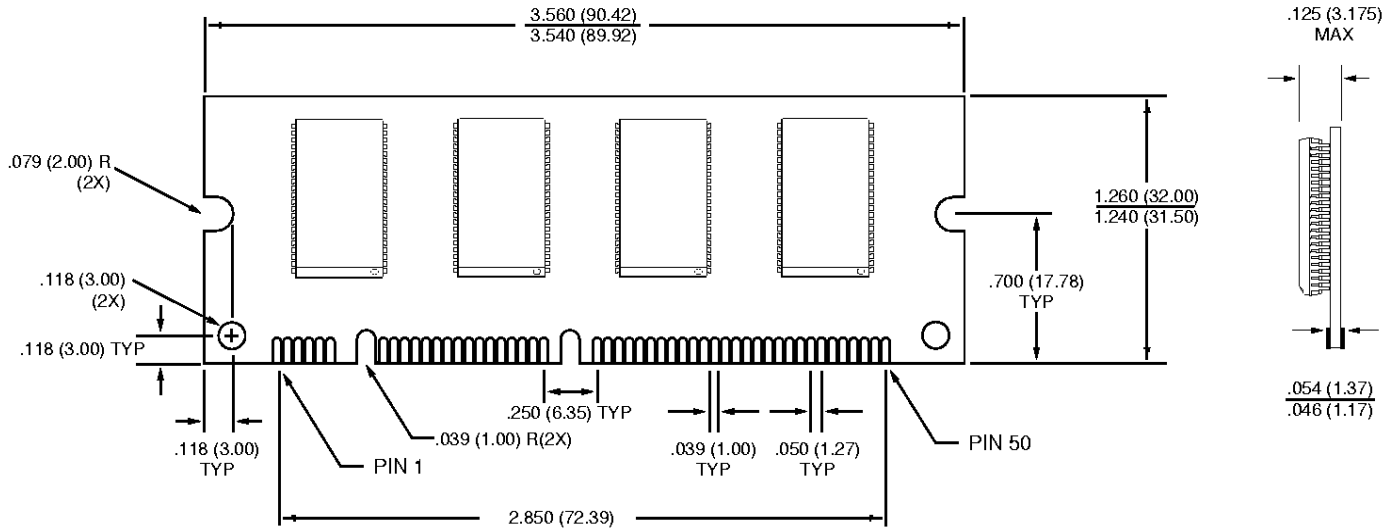
SYMBOL	MIN	MAX	UNITS
tAA	0.3	3.5	µs
tBUF	4.7		µs
tDH	300		ns
tF		300	ns
tHD:DAT	0		µs
tHD:STA	4		µs

SYMBOL	MIN	MAX	UNITS
tHIGH	4		µs
tLOW	4.7		µs
tR		1	µs
tSU:DAT	250		ns
tSU:STA	4.7		µs
tSU:STO	4.7		µs

100-PIN DIMM
(MT4LSDT232UG)



100-PIN DIMM
(MT4LSD232UG)



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