

ISD3800
Digital ChipCorder
with
Digital Audio Interface

TABLE OF CONTENTS

| | | |
|-------|--|----|
| 1 | GENERAL DESCRIPTION | 3 |
| 2 | FEATURES | 3 |
| 3 | BLOCK DIAGRAM | 5 |
| 4 | PINOUT CONFIGURATION | 6 |
| 4.1 | 48L-LQFP | 6 |
| 5 | PIN DESCRIPTION..... | 7 |
| 6 | ELECTRICAL CHARACTERISTICS | 11 |
| 6.1 | OPERATING CONDITIONS | 11 |
| 6.2 | DC PARAMETERS | 12 |
| 6.3 | AC PARAMETERS | 13 |
| 6.3.1 | <i>Inputs</i> | 13 |
| 6.3.2 | <i>Outputs</i> | 14 |
| 6.3.3 | <i>SPI Timing</i> | 17 |
| 6.3.4 | <i>I²S Timing</i> | 18 |
| 7 | APPLICATION DIAGRAM..... | 20 |
| 8 | PACKAGE SPECIFICATION | 22 |
| 8.1 | 48 LEAD LQFP(7x7x1.4MM FOOTPRINT 2.0MM)..... | 22 |
| 9 | ORDERING INFORMATION..... | 23 |
| 10 | REVISION HISTORY..... | 24 |

1 GENERAL DESCRIPTION

The ISD3800 is a digital ChipCorder® featuring digital compression, comprehensive memory management, and integrated analog/digital audio signal paths. The ISD3800 utilizes serial flash memory to provide non-volatile audio playback for a two-chip solution. The ISD3800 provides an I²S digital audio interface, faster digital programming, higher sampling frequency, and a signal path with SNR 80dB.

The ISD3800 can take digital audio data via I²S or SPI interface. When I²S input is selected, it will replace the analog audio inputs and will support sample rates of 32, 44.1 or 48 kHz depending upon clock configuration. When SPI interface is chosen, the sample rate of the audio data sent must be one of the ISD3800 supported sample rates.

The ISD3800 has inbuilt analog audio inputs, analog audio line driver, and speaker driver output.

The analog audio input, Aux-in, has a fixed gain configured by SPI command. Aux-in can directly feed-through to the analog outputs; it can also mix with the DAC output and then feed-through to the analog outputs.

Analog outputs are available in two forms: (1) Aux-out is an analog single-ended voltage output; (2) Class-AB BTL (bridge-tied-load) is an analog differential voltage output. Class-AB BTL delivers 1-watt output power at $V_{CCSPK} = 5V$.

Class-D PWM direct-drive is also available, which delivers 1-watt output power at $V_{CCSPK} = 5V$.

2 FEATURES

- External Memory:
 - The ISD3800 supports the following flash:

| Manufacturer | Winbond | | Numonyx | | | MXIC |
|--------------|----------|----------|----------|----------|----------|-----------|
| Family | 25X | 25Q | 25P | 25PX | 25PE | 25L / 25V |
| JEDEC ID | EF 30 1X | EF 40 1X | 20 20 1X | 20 71 1X | 20 80 1X | C2 20 1X |

- The addressing ability of ISD3800 is up to 128Mbit, which is 64-minute playback time based on 8kHz/4bit ADPCM.
- Inbuilt 3V voltage regulator to provide power source to the external flash memory
- Fast Digital Programming
 - Programming rate can go up to 1Mbits/second mainly limited by the flash memory write rate.
- Memory Management
 - Store pre-recorded audio (Voice Prompts) using high quality digital compression
 - Use a simple index-based command for playback
 - Execute pre-programmed macro scripts (Voice Macros) designed to control the configuration of the device and play back Voice Prompts sequences.
- Sample Rate
 - Seven sampling frequencies are available for a given master sample rate. For example, the sampling frequencies of 4, 5.3, 6.4, 8, 12.8, 16 and 32kHz are available when the device is clocked at a 32kHz master sample rate.
 - For I²S operation, 32, 44.1 and 48kHz master sample rates are available with playback sampling frequencies scaling accordingly.
- Compression Algorithms
 - For Pre-Recorded Voice Prompts
 - μ -Law: 6, 7 or 8 bits per sample

- Differential μ -Law: 6, 7 or 8 bits per sample
- PCM: 8, 10 or 12 bits per sample
- Enhanced ADPCM: 2, 3, 4 or 5 bits per sample
- Variable-bit-rate optimized compression. This allows best possible compression given a metric of SNR and background noise levels.
- Oscillator
 - Internal oscillator with internal reference: 2.048 MHz
 - Internal oscillator with external resistor: 2.048 MHz with $R_{osc} = 80\text{kohm}$
 - External crystal or clock input
 - Crystals support standard audio sampling rates of 2.048, 4.096, 8.192, 12.288 and 11.2896MHz
 - I²S bit clock input
- Inputs
 - Aux-in: Analog input with 2-bit gain control configured by SPI command
- Outputs
 - PWM: Class-D speaker driver to directly drive an 8 Ω speaker or buzzer
 - Deliver 1-watt output power at $V_{CCSPK} = 5\text{V}$
 - Aux-out: an analog single-ended voltage output
 - Class-AB BTL: an analog differential voltage output
 - Deliver 1-watt output power at $V_{CCSPK} = 5\text{V}$
 - Class-AB BTL can directly drive an 8 Ω speaker or buzzer
 - Class-AB BTL can drive an 8 Ω speaker or buzzer via an external amplifier
- I/Os
 - SPI interface: MISO, MOSI, SCLK, SSB for commands and digital audio data
 - I²S interface: I²S_CLK, I²S_WS, I²S_SDI, I²S_SDO for digital audio data
 - 8 GPIO pins:
 - 4 GPIO pins share with I²S
 - 4 GPIO pins share with SPI Interface
 - GPIO pins can trigger Voice Macro for a pushbutton application
- 8-bit Volume Control set by SPI command for flexible mixing
- Operating Voltage: 2.7 ~ 5.5V
- Standby Current: 1uA typical
- Package:
 - Green 48L-LQFP
- Temperature Options:
 - Industrial: -40°C to 85°C

3 BLOCK DIAGRAM

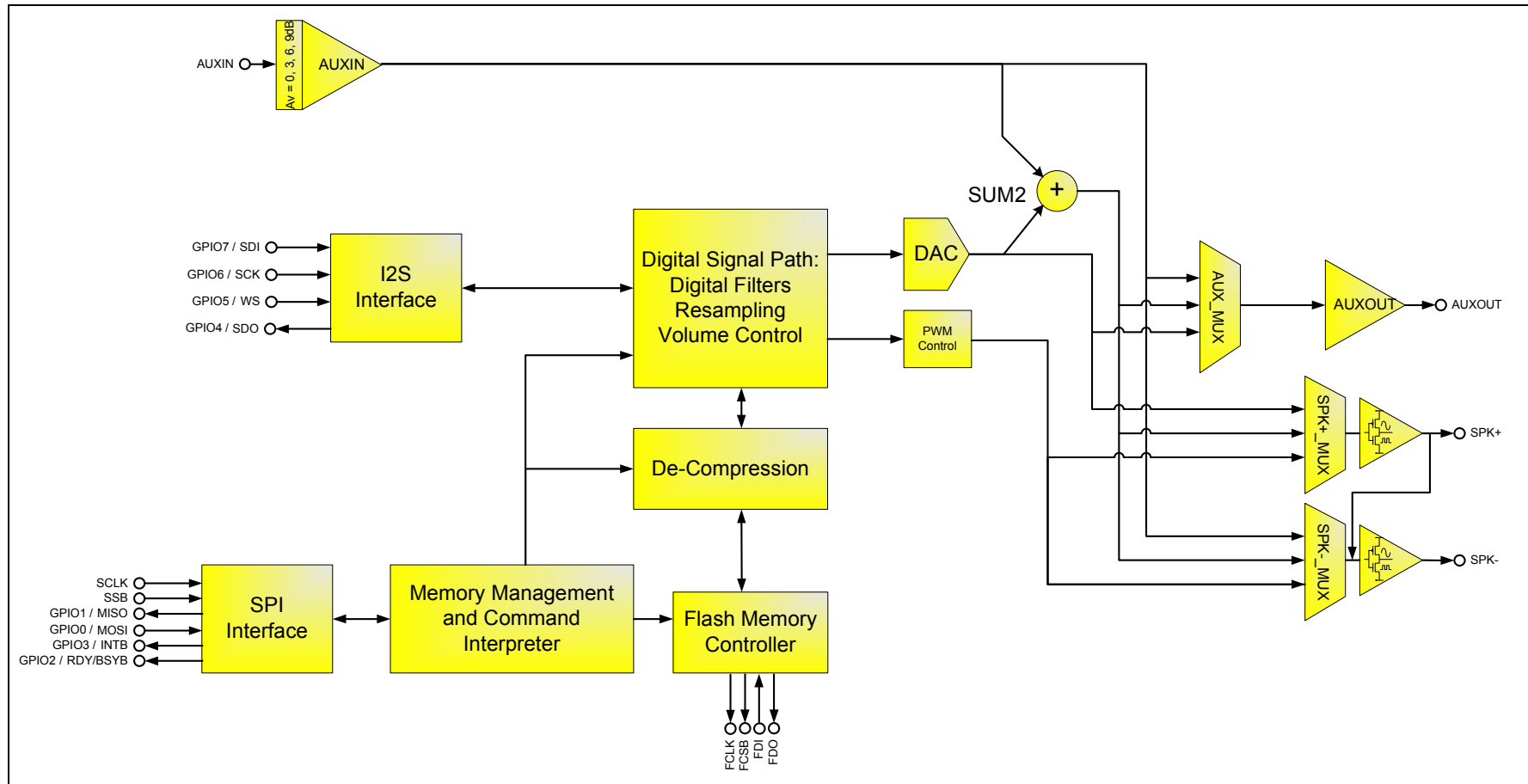


Figure 3-1 ISD3800 Block Diagram

4 PINOUT CONFIGURATION

4.1 48L-LQFP

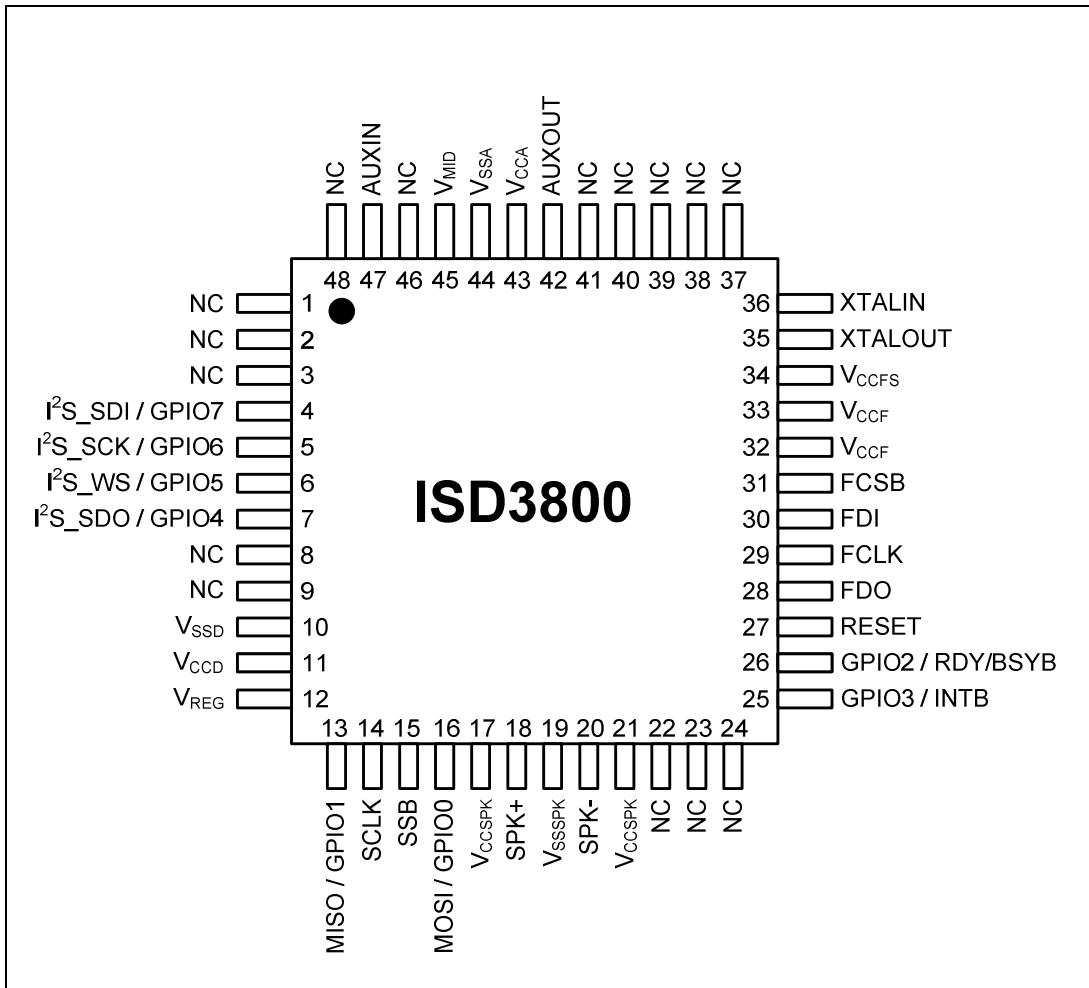


Figure 4-1 ISD3800 48-Lead LQFP Pin Configuration.

5 PIN DESCRIPTION

| Pin Number 48L- LQFP | Pin Name | I/O | Function |
|----------------------------|---------------------------------|-----|---|
| 1 | NC | | This pin should be left unconnected. |
| 2 | NC | | This pin should be left unconnected. |
| 3 | NC | | This pin should be left unconnected. |
| 4 | GPIO7 / I ² S_SDI | I/O | A GPIO pin. By default this pin is a pull-high input. Can be configured as Serial Data Input of the I ² S interface. |
| 5 | GPIO6 / I ² S_SCK | I/O | A GPIO pin. By default this pin is a pull-high input. Can be configured as Clock input in slave mode or clock output in master mode. This pin can be configured as an external clock buffer if I ² S is not used. |
| 6 | GPIO5 / I ² S_WS | I/O | A GPIO pin. By default this pin is a pull-high input. Can be configured as Word Select (WS) input in slave mode or WS output in master mode. |
| 7 | GPIO4 / I ² S_SDO | I/O | A GPIO pin. By default this pin is a pull-high input. Can be configured as Serial Data Output of the I ² S Interface. |
| 8 | NC | | This pin should be left unconnected. |
| 9 | NC | | This pin should be left unconnected. |
| 10 | V _{SSD} | I | Digital Ground. |
| 11 | V _{CCD} | I | Digital power supply. |
| 12 | V _{REG} | O | A 1.8V regulator to supply the internal logic. A minimum 1uF capacitor with low ESR<0.5OHM should be connected to this pin for supply decoupling and stability. |
| 13 | MISO / GPIO1 | O | Master-In-Slave-Out. Serial output from the ISD3800 to the host. This pin is in tri-state when SSB=1. Can be configured as GPIO1. |
| 14 | SCLK | I | Serial Clock input to the ISD3800 from the host. |
| 15 | SSB | I | Slave Select input to the ISD3800 from the host. When SSB is low device is selected and responds to commands on the SPI interface. |
| 16 | MOSI / GPIO0 | I | Master-Out-Slave-In. Serial input to the ISD3800 from the host. Can be configured as GPIO0. |

| Pin Number 48L- LQFP | Pin Name | I/O | Function |
|----------------------------|---------------------|-----|--|
| 17 | V _{CCSPK} | I | In PWM mode: Digital Power for the PWM Driver. Deliver 1-watt output power at V _{CCSPK} = 5V. Or, In Class-AB mode: Analog Power for the Class-AB output. Class-AB BTL delivers 1-watt output power at V _{CCSPK} = 5V. |
| 18 | SPK+ | O | PWM driver positive output. This SPK+ output, together with SPK- pin, provide a differential output to drive 8Ω speaker or buzzer. During power down this pin is in tri-state. Or, can be configured as Class-AB BTL which, together with SPK- pin, provides a differential voltage output. Or, can be configured as a Class-AB single-ended output. |
| 19 | V _{SSSPK} | I | In PWM mode: Digital Ground for the PWM Driver. Or, In Class-AB mode: Analog Ground for the Class-AB output. |
| 20 | SPK- | O | PWM driver negative output. This SPK- output, together with SPK+ pin, provides a differential output to drive 8Ω speaker or buzzer. During power down this pin is tri-state. Or, can be configured as Class-AB BTL which, together with SPK+ pin, provides a differential voltage output. Or, can be configured as a Class-AB single-ended output. |
| 21 | V _{CCSPK} | I | In PWM mode: Digital Power for the PWM Driver. Deliver 1-watt output power at V _{CCSPK} = 5V. Or, In Class-AB mode: Analog Power for the Class-AB output. Class-AB BTL delivers 1-watt output power at V _{CCSPK} = 5V. |
| 22 | NC | | This pin should be left unconnected. |
| 23 | NC | | This pin should be left unconnected. |
| 24 | NC | | This pin should be left unconnected. |
| 25 | INTB / GPIO3 | O | Active low interrupt request pin. This pin is an open-drain output. Can be configured as GPIO3. |
| 26 | RDY/BSYB / GPIO2 | O | An output pin to report the status of data transfer on the SPI interface. "High" indicates that ISD3800 is ready to accept new SPI commands or data. Can be configured as GPIO2. |
| 27 | RESET | I | Applying power to this pin will reset the chip. (A high pulse of 50ms or more will reset the chip.) |

| Pin Number 48L- LQFP | Pin Name | I/O | Function |
|----------------------------|-------------------|-----|--|
| 28 | FDO | O | Serial data output of the external serial flash interface. Connects to data input (DI) of external serial flash. |
| 29 | FCLK | O | Serial data CLK of the external serial flash interface. |
| 30 | FDI | I | Serial data input to external serial flash interface. Connects to data output (DO) of external flash memory. |
| 31 | FCSB | O | Chip Select Bar of the external serial flash interface. |
| 32 | V _{CCF} | O | Digital power supply for the external flash memory. A minimum 1uF capacitor with low ESR<0.5OHM should be connected to this pin for supply decoupling and stability. Refer to the application diagram. |
| 33 | V _{CCF} | O | Digital power supply for the external flash memory. A minimum 1uF capacitor with low ESR<0.5OHM should be connected to this pin for supply decoupling and stability. Refer to the application diagram. |
| 34 | V _{CCFS} | I | Digital power supply for the inbuilt voltage regulator for the external flash memory. A 0.1uF capacitor should be connected to this pin for supply decoupling and stability. Refer to the application diagram. |
| 35 | XTALOUT | O | Crystal interface output pin. |
| 36 | XTALIN | I | The CLK_CFG register determines one of the following three configurations: (1) A crystal or resonator connected between the XTALOUT and XTALIN pins. (2) A resistor connected to GND as a reference current to the internal oscillator and left the XTALOUT unconnected. (3) An external clock input to the device and left the XTALOUT unconnected. |
| 37 | NC | | This pin should be left unconnected. |
| 38 | NC | | This pin should be left unconnected. |
| 39 | NC | | This pin should be left unconnected. |
| 40 | NC | | This pin should be left unconnected. |
| 41 | NC | | This pin should be left unconnected. |
| 42 | Aux-out | O | Aux Out. This pin is an analog voltage output. If AUXOUT is not used, this pin should be left unconnected. |
| 43 | V _{CCA} | I | Analog power supply pin. |
| 44 | V _{SSA} | I | Analog ground pin. |
| 45 | V _{MID} | O | Middle voltage reference for the swing of analog/digital audio outputs. A 4.7uF capacitor should be connected to this pin for supply decoupling and stability. |
| 46 | NC | | This pin should be left unconnected. |

| Pin Number 48L- LQFP | Pin Name | I/O | Function |
|----------------------------|----------|-----|---|
| 47 | Aux-in | I | Auxiliary input with the gain set by SPI command If Aux-in is not used, this pin should be left unconnected. |
| 48 | NC | | This pin should be left unconnected. |

6 ELECTRICAL CHARACTERISTICS

6.1 OPERATING CONDITIONS

OPERATING CONDITIONS (INDUSTRIAL PACKAGED PARTS)

| CONDITIONS | VALUES |
|---|-----------------|
| Operating temperature range (Case temperature) | -40°C to +85°C |
| Digital Supply voltage (V_{CCD}) ^[1] | +2.7V to +5.5V |
| Digital Ground voltage (V_{SSD}) ^[2] | 0V |
| Analog Supply voltage (V_{CCA}) ^[3] | +2.7V to +5.5V |
| Analog Ground voltage (V_{SSA}) ^[2] | 0V |
| Speaker Supply voltage (V_{CCSPK}) ^[3] | +2.7V to +5.5V |
| Speaker Ground voltage (V_{SSSPK}) ^[2] | 0V |
| Flash Source Supply voltage (V_{CCFS}) ^[4] – to regulate V_{CCF} | +2.7V to +5.5V |
| Flash Source Supply voltage (V_{CCFS}) ^[4] – tied to V_{CCF} | +2.25V to +3.6V |
| Flash Supply voltage - (V_{CCF}) ^[4] – regulated from V_{CCFS} | +2.4V to +3.0V |
| Flash Supply voltage - (V_{CCF}) ^[4] – tied to V_{CCFS} | +2.25V to +3.6V |

NOTES:

^[1] V_{CCD} 2.7 ~ 5.5V; No restrictions with respect to V_{CCA} and V_{CCSPK} .

^[2] $V_{SSD} = V_{SSA} = V_{SSSPK}$

^[3] In Class-AB mode: V_{CCSPK} must equal V_{CCA} . Otherwise: $V_{CCSPK} \geq V_{CCA}$.

^[4] If V_{CCFS} is guaranteed to be below 3.6V (or upper flash supply limit), then V_{CCF} should be tied to V_{CCFS} .

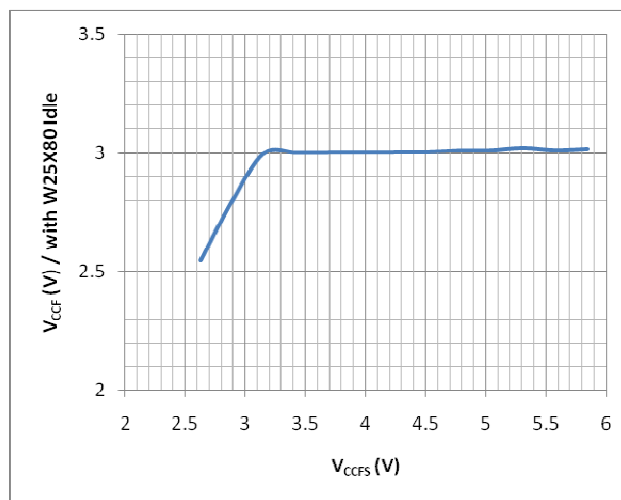


Figure 6-1 V_{CCF} vs. V_{CCFS} – V_{CCF} is regulated internally from V_{CCFS} ^[4]

6.2 DC PARAMETERS

| PARAMETER | SYMBOL | MIN | TYP [1] | MAX | UNIT S | CONDITIONS |
|---|--------------------|----------------------|--------------------|----------------------|-----------|---|
| Digital Supply Voltage | V_{CCD} | 2.7 | | 5.5 | V | |
| Analog Supply Voltage | V_{CCA} | 2.7 | | 5.5 | V | |
| Speaker Supply Voltage | V_{CCSPK} | 2.7 | | 5.5 | V | |
| Flash Source Supply Voltage | V_{CCFS} | 2.7 | | 5.5 | V | to regulate V_{CCF} |
| | | 2.25 | | 3.6 | | tied to V_{CCF} |
| Flash Supply Voltage (refer to Figure 6-1) | V_{CCF} | | V_{CCFS} -0.3 | | V | regulated from V_{CCFS} $V_{CCFS} = 2.7 \sim 3.3V$ |
| | | | 3.0 | | | regulated from V_{CCFS} $V_{CCFS} = 3.3 \sim 5.5V$ |
| | | 2.25 | | 3.6 | | tied to V_{CCFS} |
| Input Low Voltage | V_{IL} | $V_{SSD}-0.3$ | | $0.3 \times V_{CCD}$ | V | |
| Input High Voltage | V_{IH} | $0.7 \times V_{CCD}$ | | V_{CCD} | V | |
| Output Low Voltage | V_{OL} | $V_{SSD}-0.3$ | | $0.3 \times V_{CCD}$ | V | $I_{OL} = 1mA$ |
| Output High Voltage | V_{OH} | $0.7 \times V_{CCD}$ | | V_{CCD} | V | $I_{OH} = -1mA$ |
| INTB Output Low Voltage | V_{OH1} | | | 0.4 | V | |
| Playback Current | $I_{DD_Playback}$ | | | 30 | mA | |
| Standby Current | I_{SB} | | 1 | 10 | μA | |
| Input Leakage Current | I_{IL} | | ± 1 | | μA | Force V_{CCD} |

Notes: ^[1] Conditions $V_{CCD}=V_{CCA}=V_{CCSPK}=V_{CCFS}=3V$, $T_A=25^\circ C$ unless otherwise stated

6.3 AC PARAMETERS

6.3.1 Inputs

AUX-IN:

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 5V$, MCLK = 16.384MHz, $T_A = +25^{\circ}C$, 1kHz signal

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|--|---------------|---|--------|----------------------|--------|--|
| Auxiliary Analog Inputs (AUXIN) | | | | | | |
| Full scale input signal ¹ | | Gain = 0dB | | 1.0 0 | | Vrms dBV |
| AUX Programmable gain | | | 0 | | 9 | dB |
| AUX programmable gain step size | | Guaranteed Monotonic | | 3 | | dB |
| Input resistance | | Aux direct-to-out path, only Input gain = +9.0dB Input gain = +6.0dB Input gain = +3.0dB Input gain = 0dB | | 21 27 33 40 | | k Ω k Ω k Ω k Ω |
| Aux-in Gain Accuracy | $A_{AUX(GA)}$ | | -0.5dB | | +0.5dB | dB |

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 3.3V$, MCLK = 16.384MHz, $T_A = +25^{\circ}C$, 1kHz signal

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|--|---------------|---|--------|----------------------|--------|--|
| Auxiliary Analog Inputs (AUXIN) | | | | | | |
| Full scale input signal ¹ | | Gain = 0dB | | 1.0 0 | | Vrms dBV |
| AUX Programmable gain | | | 0 | | 9 | dB |
| AUX programmable gain step size | | Guaranteed Monotonic | | 3 | | dB |
| Input resistance | R_{aux_in} | Aux direct-to-out path, only Input gain = +9.0dB Input gain = +6.0dB Input gain = +3.0dB Input gain = 0dB | | 21 27 33 40 | | k Ω k Ω k Ω k Ω |
| Aux-in Gain Accuracy | $A_{AUX(GA)}$ | | -0.5dB | | +0.5dB | dB |

6.3.2 Outputs

Aux-out

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 5V$, MCLK = 16.384MHz, $T_A = +25^{\circ}C$, 1kHz signal

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|--------|---|-----|-----------------|-----|-----------|
| Digital to Analog Converter (DAC) driving AUXOUT with 5kΩ / 100pF load | | | | | | |
| Full-scale output | | Gain paths all at 0dB gain | | $V_{CCA} / 3.3$ | | V_{rms} |
| Signal-to-noise ratio | SNR | A-weighted | | 85 | | dB |
| Total harmonic distortion ² | THD+N | $R_L = 5k\Omega$; full-scale signal A-weighted | | -80 | | dB |

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 3.3V$, MCLK = 16.384MHz, $T_A = +25^{\circ}C$, 1kHz signal

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|--------|---|-----|-----------------|-----|-----------|
| Digital to Analog Converter (DAC) driving AUXOUT with 5kΩ / 100pF load | | | | | | |
| Full-scale output | | Gain paths all at 0dB gain | | $V_{CCA} / 3.3$ | | V_{rms} |
| Signal-to-noise ratio | SNR | A-weighted | | 80 | | dB |
| Total harmonic distortion ² | THD+N | $R_L = 5k\Omega$; full-scale signal A-weighted | | -77 | | dB |

PWM OUTPUT

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 5V$, $MCLK = 16.384MHz$, $T_A = +25^{\circ}C$, 1kHz signal

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|-----------|--|-----|-----|-----|-------|
| Speaker PWM Output (SPK_PLUS / SPK_MINUS with 8Ω bridge-tied-load) | | | | | | |
| Signal-to-noise ratio ³ | SNR | A-weighted + Class D Filter | | 65 | | dB |
| Total harmonic distortion ² | THD | $P_o = 1W$, A-weighted + Class D Filter | | -40 | | dB |
| Efficiency | E_{PWM} | 8Ω bridge-tied-load $P_{out} > 0.2W$ | | 85 | | % |

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 3.3V$, $MCLK = 16.384MHz$, $T_A = +25^{\circ}C$, 1kHz signal

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|-----------|---|-----|-----|-----|-------|
| Speaker PWM Output (SPK_PLUS / SPK_MINUS with 8Ω bridge-tied-load) | | | | | | |
| Signal-to-noise ratio ³ | SNR | A-weighted + Class D Filter | | 65 | | dB |
| Total harmonic distortion ² | THD | A-weighted + Class D Filter | | -40 | | dB |
| Efficiency | E_{PWM} | 8Ω bridge-tied-load $P_{out} > 0.2W$ | | 80 | | % |

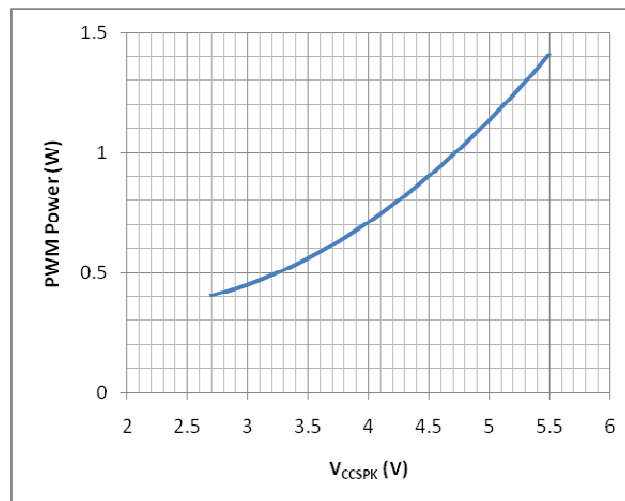


Figure 6-2 PWM Power vs. V_{CCSPK}

CLASS-AB BTL OUTPUT

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 5V$, $MCLK = 16.384MHz$, $T_A = +25^{\circ}C$, 1kHz signal

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|--|----------|---|-----------------|-----|-----|-----------|
| Speaker CLASS-AB BTL Output (SPK_PLUS / SPK_MINUS with 8Ω bridge-tied-load) | | | | | | |
| Full scale output | | Gain paths all at 0dB gain | $V_{CCA} / 3.3$ | | | V_{rms} |
| Signal-to-noise ratio | SNR | A-weighted | | 90 | | dB |
| Total harmonic distortion ² | THD | $P_o = 1W$, A-weighted | | -60 | | dB |
| Efficiency | E_{AB} | 8Ω bridge-tied-load $P_{out} > 0.7W$ | | 50 | | % |

Conditions: $V_{CCD} = 3.3V$, $V_{CCA} = V_{CCSPK} = 3.3V$, $MCLK = 16.384MHz$, $T_A = +25^{\circ}C$, 1kHz signal

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|--|----------|---|-----------------|-----|-----|-----------|
| Speaker CLASS-AB BTL Output (SPK_PLUS / SPK_MINUS with 8Ω bridge-tied-load) | | | | | | |
| Full scale output | | Gain paths all at 0dB gain | $V_{CCA} / 3.3$ | | | V_{rms} |
| Signal-to-noise ratio | SNR | A-weighted | | 84 | | dB |
| Total harmonic distortion ² | THD | A-weighted | | -60 | | dB |
| Efficiency | E_{AB} | 8Ω bridge-tied-load $P_{out} > 0.4W$ | | 50 | | % |

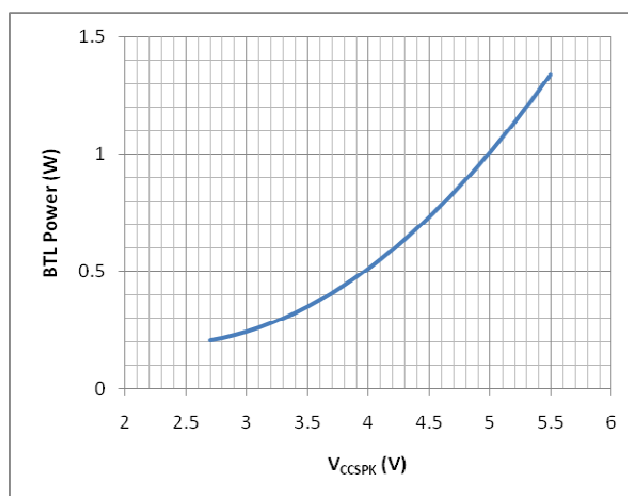


Figure 6-3 Class-AB BTL Power vs. V_{CCSPK}

Notes

1. Full Scale is relative to the magnitude of V_{CCA} and can be calculated as $FS = V_{CCA}/3.3$.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. SNR measured with a -100dbFS signal at input.

6.3.3 SPI Timing

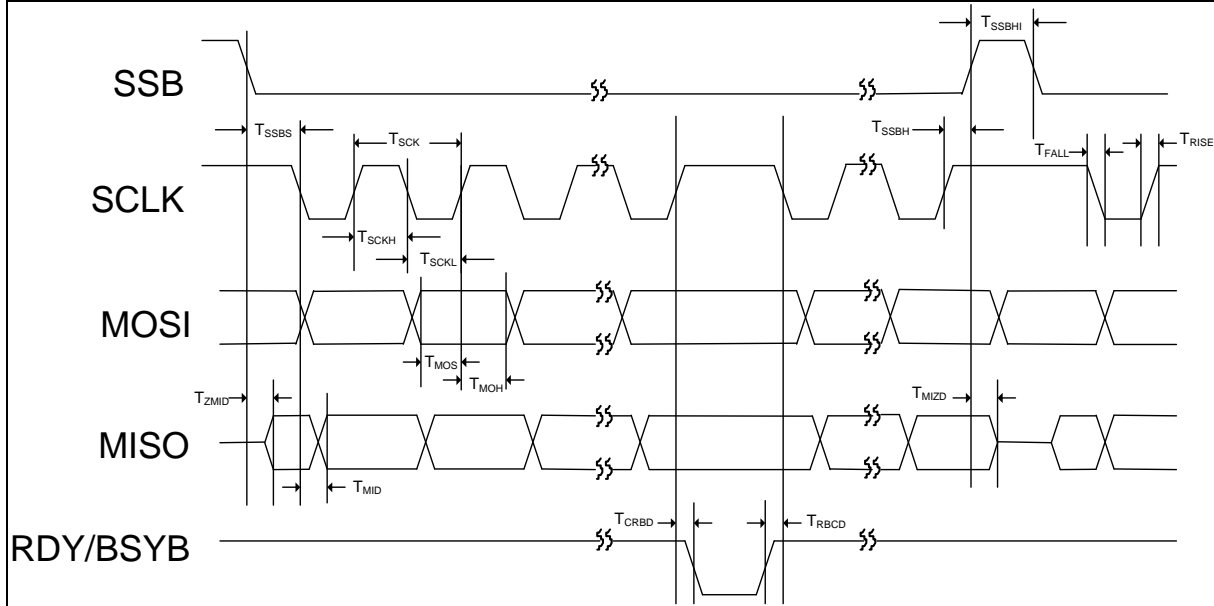


Figure 6-4 SPI Timing

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|--------------------|--|------|-----|------|------|
| T _{SCK} | SCLK Cycle Time | 60 | --- | --- | ns |
| T _{SCKH} | SCLK High Pulse Width | 25 | --- | --- | ns |
| T _{SCKL} | SCLK Low Pulse Width | 25 | --- | --- | ns |
| T _{RISE} | Rise Time for All Digital Signals | --- | --- | 10 | ns |
| T _{FALL} | Fall Time for All Digital Signals | --- | --- | 10 | ns |
| T _{SSBS} | SSB Falling Edge to 1 st SCLK Falling Edge Setup Time | 30 | --- | --- | ns |
| T _{SSBH} | Last SCLK Rising Edge to SSB Rising Edge Hold Time | 30ns | --- | 50us | --- |
| T _{SSBHI} | SSB High Time between SSB Lows | 20 | --- | --- | ns |
| T _{MOS} | MOSI to SCLK Rising Edge Setup Time | 15 | --- | --- | ns |
| T _{MOH} | SCLK Rising Edge to MOSI Hold Time | 15 | --- | --- | ns |
| T _{ZMID} | Delay Time from SSB Falling Edge to MISO Active | -- | -- | 12 | ns |
| T _{MIZD} | Delay Time from SSB Rising Edge to MISO Tri-state | -- | -- | 12 | ns |

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------------|---|-----|-----|-----|------|
| T_{MID} | Delay Time from SCLK Falling Edge to MISO | --- | --- | 12 | ns |
| T_{CRBD} | Delay Time from SCLK Rising Edge to RDY/BSYB Falling Edge | -- | -- | 12 | ns |
| T_{RBCD} | Delay Time from RDY/BSYB Rising Edge to SCLK Falling Edge | 0 | -- | -- | ns |

6.3.4 I²S Timing

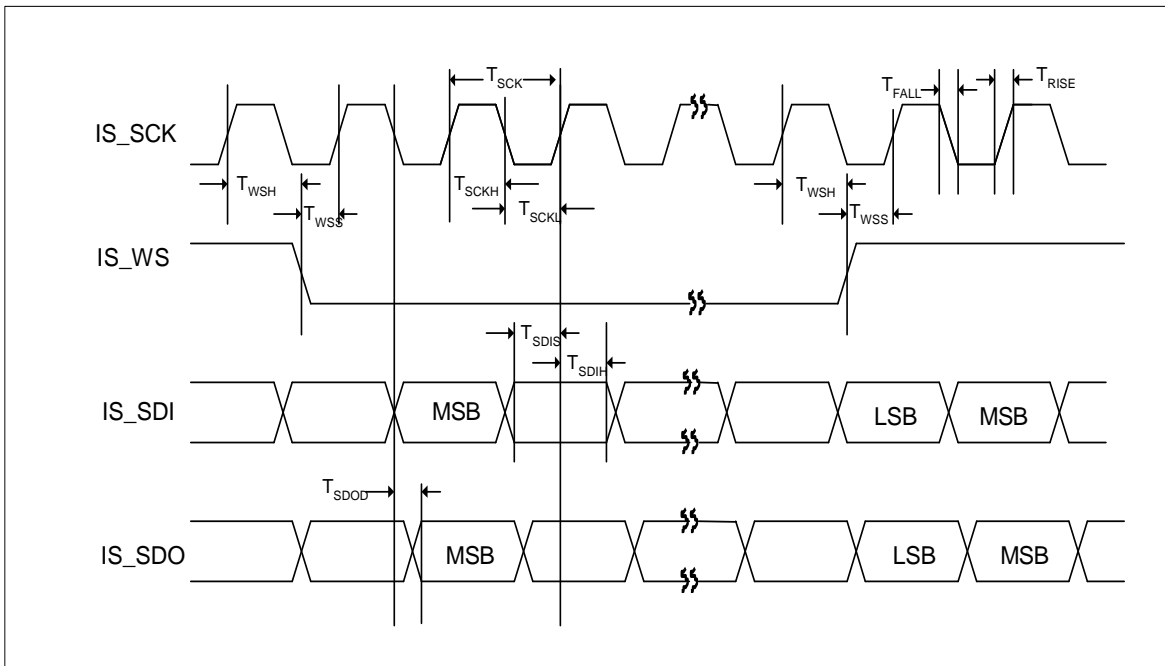


Figure 6-5 I²S Timing

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|------------|-----------------------------------|-----|-----|-----|------|
| T_{SCK} | IS_SCK Cycle Time | 60 | --- | --- | ns |
| T_{SCKH} | IS_SCK High Pulse Width | 25 | --- | --- | ns |
| T_{SCKL} | IS_SCK Low Pulse Width | 25 | --- | --- | ns |
| T_{RISE} | Rise Time for All Digital Signals | --- | --- | 10 | ns |
| T_{FALL} | Fall Time for All Digital Signals | --- | --- | 10 | ns |

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|-------------------|--|-----|-----|-----|------|
| T _{WSS} | WS to IS_SCK Rising Edge Setup Time | 20 | --- | --- | ns |
| T _{WSH} | IS_SCK Rising Edge to IS_WS Hold Time | 20 | --- | --- | ns |
| T _{SDIS} | IS_SDI to IS_SCK Rising Edge Setup Time | 15 | --- | --- | ns |
| T _{SDIH} | IS_SCK Rising Edge to IS_SDI Hold Time | 15 | --- | --- | ns |
| T _{SDOD} | Delay Time from IS_SCLK Falling Edge to IS_SDO | --- | --- | 12 | ns |

7 APPLICATION DIAGRAM

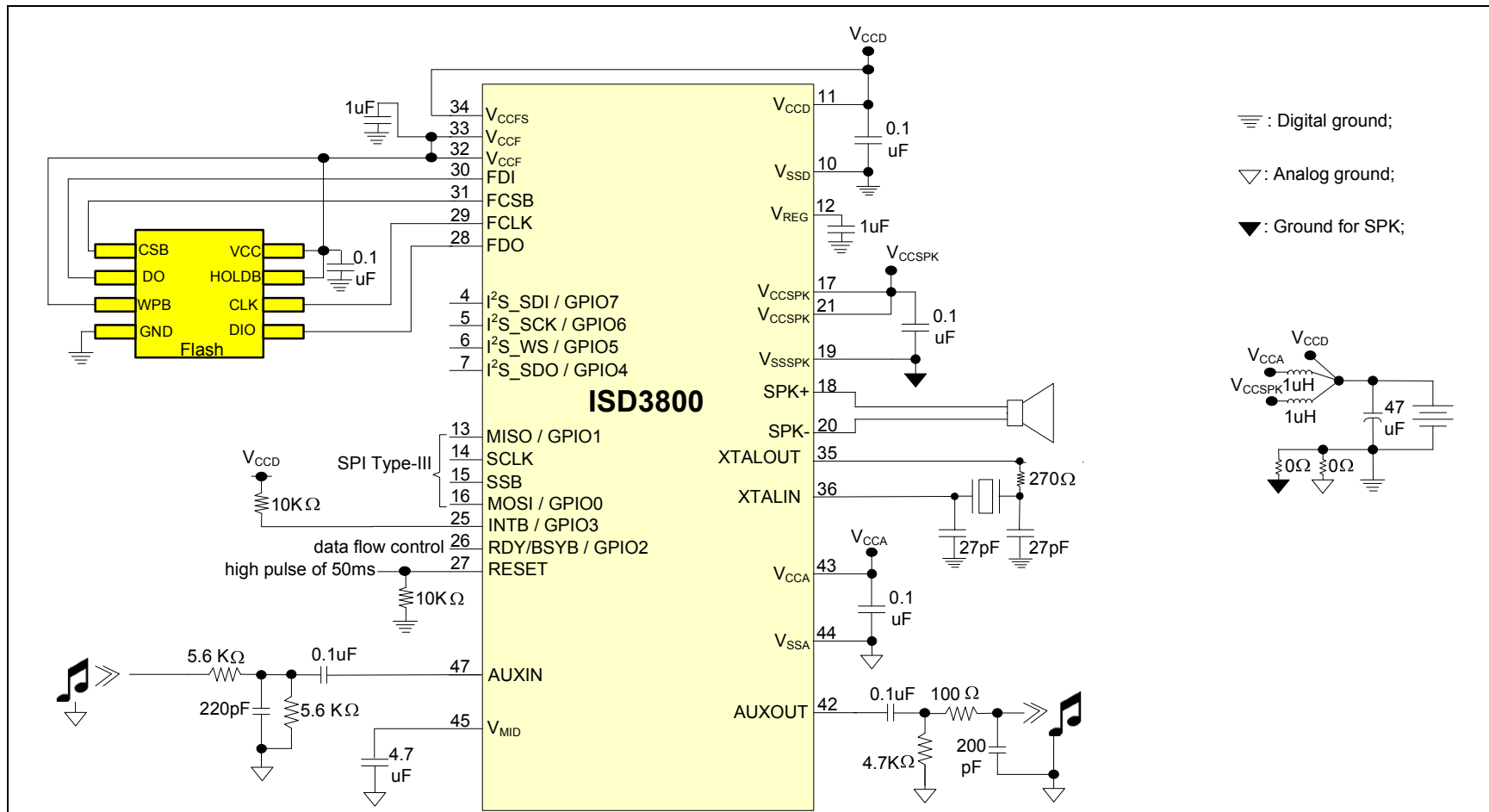


Figure 7-1 ISD3800 Application Diagram – V_{CCF} is regulated internally from V_{CCFS}

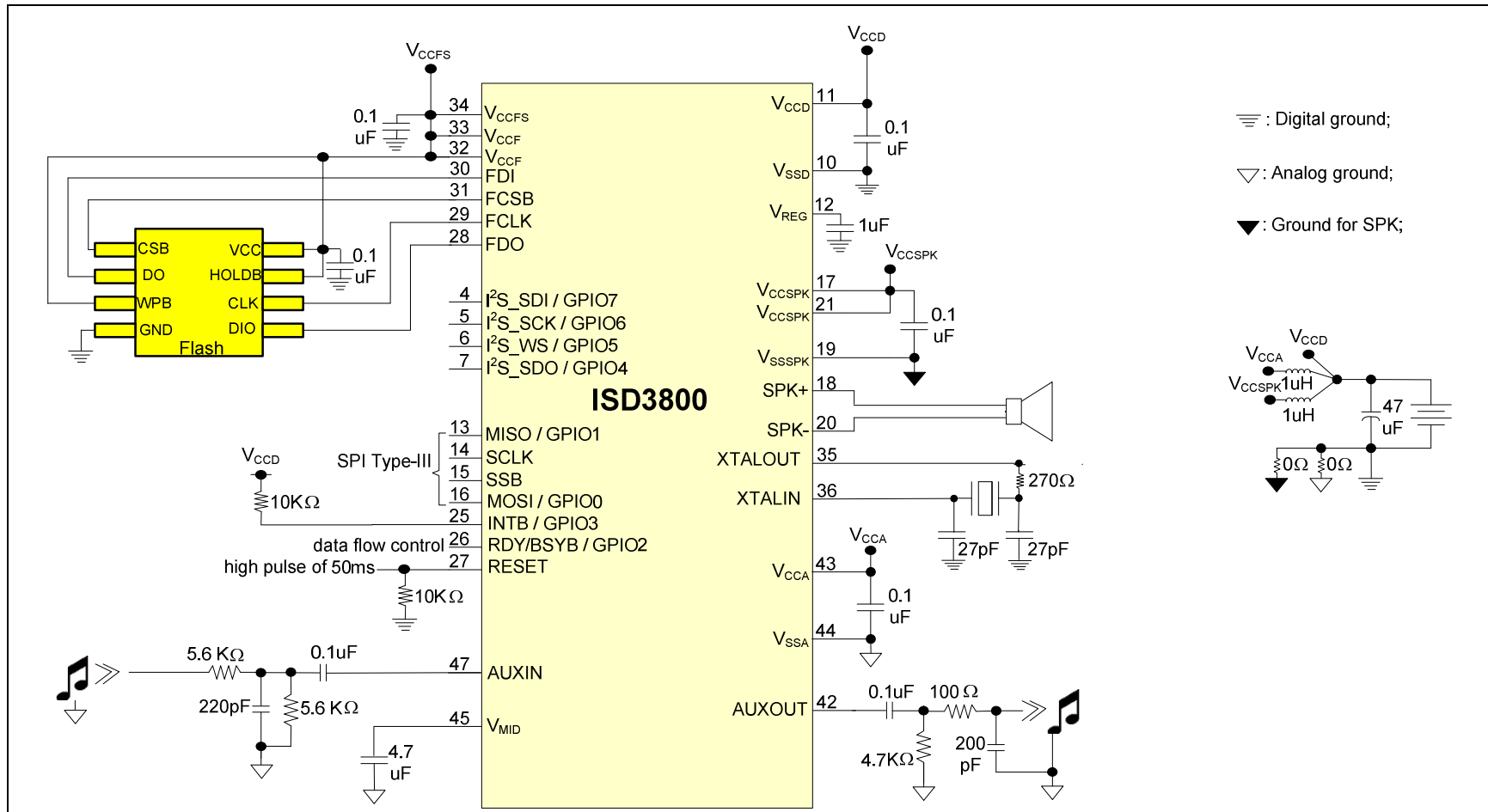
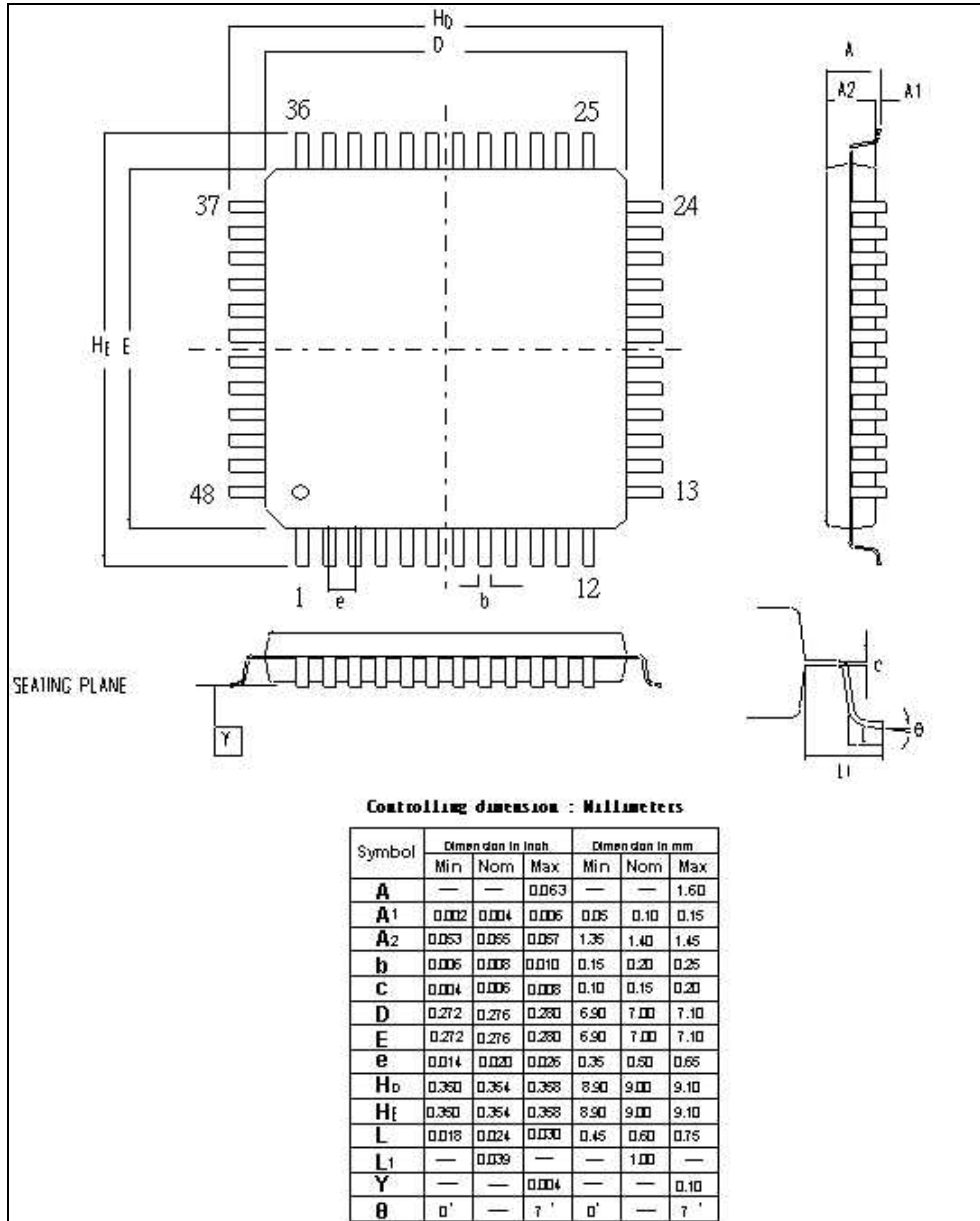


Figure 7-2 ISD3800 Application Diagram – V_{CCF} is tied to V_{CCFS}

The above application examples are for references only. It makes no representation or warranty that such applications shall be suitable for the use specified. Each design has to be optimized in its own system for the best performance on voice quality, current consumption, functionalities and etc.

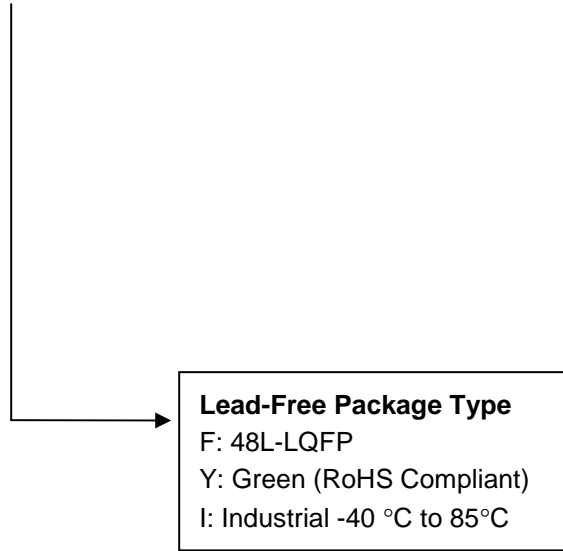
8 PACKAGE SPECIFICATION

8.1 48 LEAD LQFP(7X7X1.4MM FOOTPRINT 2.0MM)



9 ORDERING INFORMATION

I3800 FYI



10 REVISION HISTORY

| Version | Date | Description |
|----------------|--------------|--|
| 0.23 | Aug 3, 2009 | Initially released as the Preliminary Datasheet. |
| 0.26 | Aug 17, 2009 | Update application diagram. |
| 0.27 | Sep 28, 2009 | Update the list of supported Flash Memory. |
| 0.29 | Nov 18, 2009 | Update: <ul style="list-style-type: none">• Block Diagram.• Electrical Characteristics. |
| 0.35 | Feb 8, 2010 | Update block diagram. |
| 0.40 | July 1, 2010 | Update crystal configuration. |
| 0.50 | Aug 12, 2010 | Update PWM spec. |
| 0.60 | Sep 22, 2010 | Update ordering information. |

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Nuvoton customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Nuvoton for any damages resulting from such improper use or sales.

The contents of this document are provided only as a guide for the applications of Nuvoton products. Nuvoton makes no representation or warranties with respect to the accuracy or completeness of the contents of this publication and reserves the right to discontinue or make changes to specifications and product descriptions at any time without notice. No license, whether express or implied, to any intellectual property or other right of Nuvoton or others is granted by this publication. Except as set forth in Nuvoton's Standard Terms and Conditions of Sale, Nuvoton assumes no liability whatsoever and disclaims any express or implied warranty of merchantability, fitness for a particular purpose or infringement of any Intellectual property.

The contents of this document are provided "AS IS", and Nuvoton assumes no liability whatsoever and disclaims any express or implied warranty of merchantability, fitness for a particular purpose or infringement of any Intellectual property. In no event, shall Nuvoton be liable for any damages whatsoever (including, without limitation, damages for loss of profits, business interruption, loss of information) arising out of the use of or inability to use the contents of this documents, even if Nuvoton has been advised of the possibility of such damages.

Application examples and alternative uses of any integrated circuit contained in this publication are for illustration only and Nuvoton makes no representation or warranty that such applications shall be suitable for the use specified.

The 100-year retention and 100K record cycle projections are based upon accelerated reliability tests, as published in the Nuvoton Reliability Report, and are neither warranted nor guaranteed by Nuvoton.

This datasheet and any future addendum to this datasheet is(are) the complete and controlling ISD[®] ChipCorder[®] product specifications. In the event any inconsistencies exist between the information in this and other product documentation, or in the event that other product documentation contains information in addition to the information in this, the information contained herein supersedes and governs such other information in its entirety. This datasheet is subject to change without notice.

Copyright[®] 2005, Nuvoton Technology Corporation. All rights reserved. ChipCorder[®] and ISD[®] are trademarks of Nuvoton Technology Corporation. All other trademarks are properties of their respective owners.

Headquarters

No. 4, Creation Rd. III
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
<http://www.Nuvoton.com.tw/>

Nuvoton Technology Corporation America

2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441797
<http://www.Nuvoton-usa.com/>

Nuvoton Technology (Shanghai) Ltd.

27F, 299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62356988

Taipei Office

9F, No. 480, Pueiguang Rd.
Neihu District
Taipei, 114 Taiwan
TEL: 886-2-81777168
FAX: 886-2-87153579

Nuvoton Technology Corporation Japan

7F Daini-ueno BLDG. 3-7-18
Shinyokohama Kohokuku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Nuvoton Technology (H.K.) Ltd.

Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

Please note that all data and specifications are subject to change without notice.
All the trademarks of products and companies mentioned in this datasheet belong to their respective owners.