BROADCOM® SWP

BCM20793S

Near Field Communications Controller with Integrated EEPROM for Battery-off Mode

GENERAL DESCRIPTION

The Broadcom® BCM20793S is an NFC-compliant, highly integrated, low power, low cost, 40 nm NFC controller combined with an integrated EEPROM for battery-off operation in a single package. The BCM20793S is an update to the BCM20793, which features secure configuration and patch download for applications involving the management and operation of NFC secure elements. The BCM20793S size-optimized architecture is housed in a QFN-34L package that measures 4.0 mm × 4.5 mm × 0.9 mm (nominal), and requires minimal external components. This brings the traditional two-chip NFC controller and EEPROM for battery-off operation into a single package solution to minimize PCB footprint. Refer to the architecture block diagram in Figure 1 on page 2.

The BCM20793S is designed for low-power mobile applications. It is based on over 15 years of Radio Frequency Identification (RFID) and NFC experience. By building onto the BCM20792S, the BCM20793S is designed to be an integral part of all NFC standards-compliant systems. The BCM20793S has the same dual Single Wire Protocol (SWP) secure element interfaces as the BCM20792S, but brings the EEPROM option for battery-off operation to be internal to the package. The BCM20793S is package and pin-compatible with the BCM20794S (which has integral secure element) using minimal external link component changes. The BCM20793S incorporates the PPSE and AID routing functionality for support of multiple applications across multiple secure elements and execution environments.

APPLICATIONS

- Contactless payment
- Mobile handsets
- Simplified connectivity between wireless devices
- Contactless ticketing
- Peer mode transactions
- Smartposter tag reading/writing
- Access control

FEATURES

NFC

- Support for the ISO/IEC 18092, ISO/IEC 21481, ISO/IEC 14443 Types A, B and B', Japanese Industrial Standard (JIS) (X) 6319-4, and ISO/IEC 15693 standards
- No active components requirement for antenna or field-power conditioning
- Individual byte framing
- Hardware-based collision detection and modulation controls
- Reader/Writer (R/W) mode
- Active and Passive Peer (P2P) mode
- Tag/Card Emulation mode:
  - Support for battery-enabled card emulation mode
  - Support for two levels of "residual" battery-assisted card emulation mode
  - Support for completely powered from the field (battery-off) card emulation mode
- Co-packaged CAT24C64 EEPROM:
  - 64 Kb (8 KB) for battery-off personality, persistence, and PPSE/AID routing data storage
- Dual Single Wire Protocol (SWP) interfaces:
  - SWP_0 with platform PMU SIM power switching to UICC SIM card.
  - SWP_1 for embedded secure element or secondary UICC SIM cards
- Supports application tunnelling to secure elements over SWP
- Supports AID routing between host and secure element(s)
- Internal low-power oscillator for periodic wake-up and mode switch operation
- Low-power target detection mode for extremely low average current consumption 'sniff mode'
- NFC Forum NFC Controller Interface (NCI) for host interface

General

- Integral Low-Drop Out (LDO) regulator for direct connection to platform battery
- Clock sourced from platform reference frequency input for minimum BOM (or external XTAL option)
- ARM® Cortex®-M0 with 128 KB ROM and 19 KB RAM
- Supports UART, SPI, and BSC (I^2C-compatible) for host interface
- Multiple low-power modes for flexible power management
- Low-power consumption in all modes and support for field-power mode
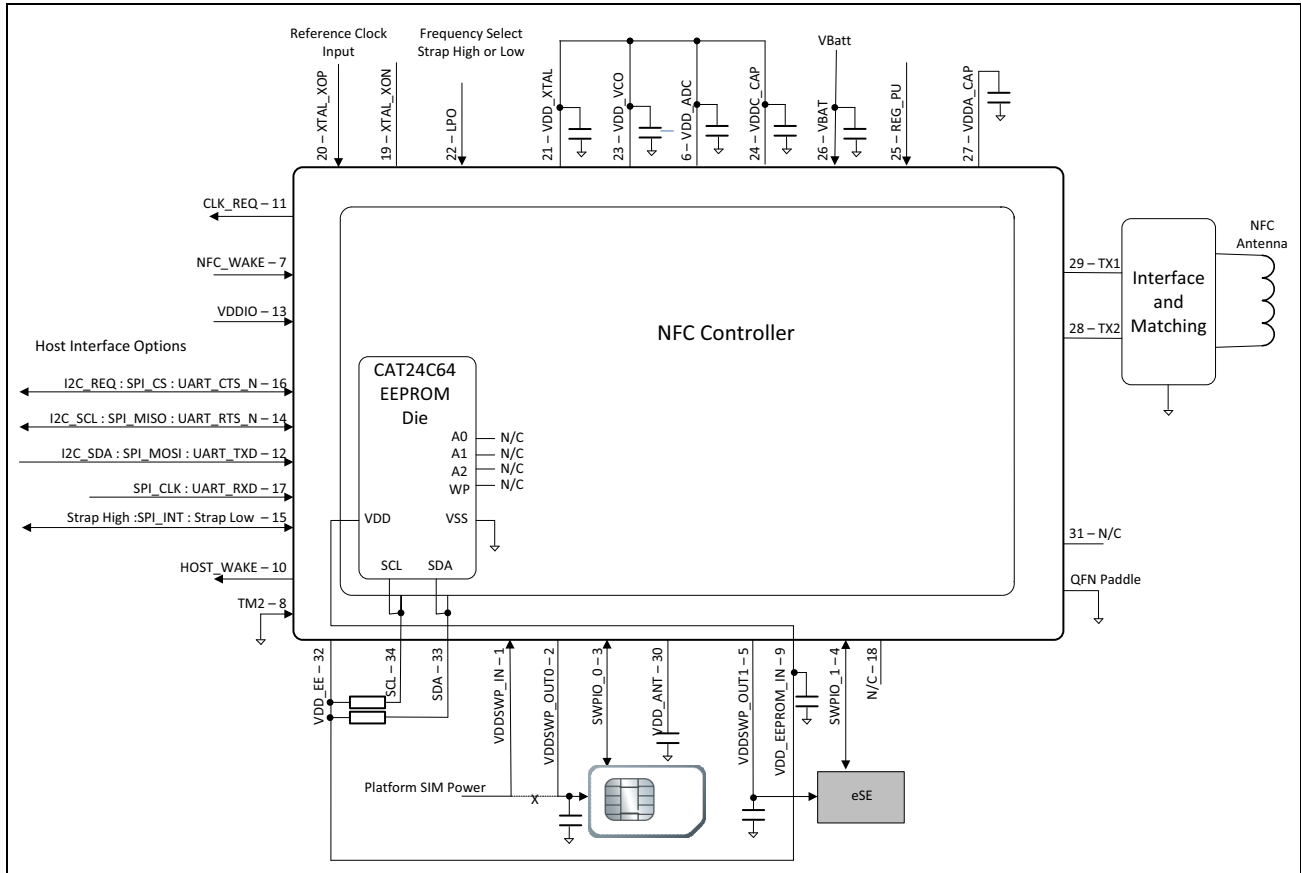- Minimum hardware size and BOM

20793S-DS101-R

Figure 1: Functional Block Diagram

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Revision History

Revision	Date	Change Description
20793S-DS101-R	06/05/12	**Updated:** • Corrected errors related to the Single Wire Protocol (SWP) interface. • Table 5: "Transitions Controlled by the Host," on page 25 and Table 6: "Transitions Controlled Through the VBAT Monitor," on page 27—removed the footnote related to EEPROM requirements.
20793S-DS100-R	05/21/12	Initial release.

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About This Document

Purpose and Audience

This document is for design engineers responsible for adding a BCM20793S NFC controller to mobile devices to enable contactless payment, contactless ticketing, easy pairing of wireless devices (Bluetooth and Wi-Fi), etc. Sections of this document include the NFC subsystem, interfaces, microprocessor and memory unit, and specifications of the BCM20793S.

Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use.

Acronyms and abbreviations in this document are also defined in Appendix A: "Acronyms," on page 60.

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: http://www.broadcom.com/press/glossary.php.

References

The references in this section may be used in conjunction with this document.

> **Note:** Broadcom provides customer access to technical documentation and software through its Customer Support Portal (CSP) and Downloads & Support site (see Technical Support).

For Broadcom documents, replace the "xx" in the document number with the largest number available in the repository to ensure that you have the most current version of the document.

Document (or Item) Name	Number	Source
Broadcom Items		
[1] Current Consumption While Polling	20791-AN1xx-R	Broadcom CSP
Other Items		
[2] Identification cards – Contactless integrated circuit cards – Proximity cards– Part 2: Radio frequency power and signal interface	ISO/IEC 14443-2:2010	www.iso.org/
[3] Identification cards – Contactless integrated circuit(s) cards – Proximity cards – Part 3: Initialization and anticollision	ISO/IEC 14443-3:2001	www.iso.org/
[4] Identification cards – Contactless integrated circuit cards– Proximity cards -- Part 4: Transmission protocol	ISO/IEC 14443-4:2008 (2nd Edition)	www.iso.org/
[5] Identification cards – Contactless integrated circuit cards – Vicinity cards – Part 2: Air interface and initialization	ISO/IEC 15693-2:2006	www.iso.org/

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Document (or Item) Name (Cont.)	Number	Source
[6] *Identification cards – Contactless integrated circuit cards – Vicinity cards – Part 3: Anticollision and transmission protocol*	ISO/IEC 15693-3:2009	www.iso.org/
[7] *Information technology – Telecommunications and information exchange between systems – Near Field Communication – Interface and Protocol (NFCIP-1)*	ISO/IEC 18092:2004	www.iso.org/
[8] *Information technology – Telecommunications and information exchange between systems – Near Field Communication Interface and Protocol -2 (NFCIP-2)*	ISO/IEC 21481:2005	www.iso.org/
[9] *Specification of implementation for integrated circuit(s) cards – Part 4: High Speed proximity cards*	JIS (X) 6319-4	http://www.jisc.go.jp

Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (https://support.broadcom.com). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads & Support site (http://www.broadcom.com/support/).

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Section 1: Introduction

General Description

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The BCM20793S is designed for low-power mobile applications. It is based on over 15 years of Radio Frequency Identification (RFID) and NFC experience. The IP base that comprises the BCM20793S is the first in a family of products that targets the entire NFC ecosystem. Follow-on devices will include multiradio (Bluetooth, Wi-Fi, FM, GPS) combo chips, making the BCM20793S an ideal starting point for mobile customers looking for a clear path to cost and board space reduction.

The BCM20793S is designed to be an integral part of all NFC standards-compliant systems.

The BCM20793S has the same dual Single Wire Protocol (SWP) secure element interfaces as the BCM20792S, but brings the EEPROM option for battery-off operation to be internal to the package. The BCM20793S is package and pin-compatible with the BCM20794S (which has integral secure element) using minimal external link component changes. The BCM20793S incorporates the PPSE and AID routing functionality for support of multiple applications across multiple secure elements and execution environments, and also supports application tunneling to secure elements over SWP.

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Features

NFC Features

- Support for the ISO/IEC 18092, ISO/IEC 21481, ISO/IEC 14443 Types A, B and B', Japanese Industrial Standard (JIS) (X) 6319-4, and ISO/IEC 15693 standards
- No active components requirement for antenna or field-power conditioning
- Individual byte framing
- Hardware-based collision detection and modulation controls
- Reader/Writer (R/W) mode
- Active and Passive Peer (P2P) mode
- Tag/Card Emulation mode:
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  - SWP_0 with platform PMU power switching to UICC SIM card.
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  - Supports application tunnelling to secure elements over SWP
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- Minimum hardware size and BOM

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Applications

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- Access control

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Section 2: NFC Subsystem

Operational Modes

The operational modes as defined by the NFC Forum and are supported by the BCM20793S. The following operational modes, as defined by the NFC Forum and NFC standards are supported by the BCM20793S.

Peer Mode

The BCM20793S, along with its software stack, fully supports Peer mode. In Peer mode, the BCM20793S is capable of acting as both an initiator and a target.

This mode of operation allows for well-formed transmission of application data from one NFC device to another NFC device.

Peer mode utilizes the Link Layer Control Protocol (LLCP) defined by the NFC Forum. The physical layer and portions of the MAC layer standards are defined in NFCIP-1 standard ISO/IEC 18092 (ECMA 340). A Peer mode initiator is responsible for beginning communication with a Peer mode target. The initiator is also responsible for generating the RF field. The BCM20793S supports both Active and Passive Communications modes.

Reader/Writer Mode

In the Reader/Writer mode, the BCM20793S acts as a reader or writer of low-cost NFC Forum-defined contactless tags. There are four tag types that are mandated by the NFC Forum. Broadcom® is the exclusive supplier of Tag Type 1 – which is ideal for simple pairing, business card, and all nonpayment applications. For further information on the BCM20203, the Broadcom Topaz Tag (NFC Forum Tag 1), contact your Broadcom representative.

The BCM20793S is capable of detecting, reading, and writing to any of the NFC Forum-supported tag types.

Card Emulation Mode

In Card Emulation mode, the NFC system issues and responds to commands in the same way as a contactless smart card. The use cases for Card and Tag Emulation mode include payment and ticketing.

The BCM20793S supports full Tag and Card Emulation mode when paired with a suitable Secure Element or host device.

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ISO Standards

The BCM20793S supports several RF and ISO standards at various bit rates, up to and including 424 Kbps. A list of the ISO and JIS standards that are supported by the BCM20793S are listed in Table 1.

Table 1: ISO/IEC 14443 A and B, FeliCa, and NFC Forum Modes

Standard	Reader/Initiator			Tag/Target		
Data Rate (kbps)	106	212	424	106	212	424
ISO/IEC 14443 A	✓	✓	✓	✓	✓	✓
ISO/IEC 14443 B	✓	✓	✓	✓	✓	✓
ISO/IEC 14443 B – Prime				✓	✓	✓
ISO/IEC 18092/ECMA 340 Active	✓	✓	✓	✓	✓	✓
ISO/IEC 18092/ECMA 340 Passive	✓	✓	✓	✓	✓	✓
JIS (X) 6319-4 FeliCa		✓	✓		✓	✓

The BCM20793S also supports reader and tag modes for ISO/IEC 15693[1]. A list of supported bit rates can be found in Table 2.

Table 2: ISO/IEC 15693 Supported Bit Rates

Communications Mode	VICC to VCD				VCD to VICC	
Subcarrier	Single		Dual		N/A	
Data Rate (kbps)	6.62	26.48	6.67	26.69	1.65	26.48
Reader Support	✓	✓	–[a]	–[a]	✓	✓
Tag Support	✓	✓	✓	✓	✓	✓

a. Reader version supports only Single Subcarrier mode.

[1]. The host can define Single or Multiple State Machine capabilities, which can alter ISO/IEC 15693 availability. See "Multiple Technology Support and Automatic Standard Detection" on page 19 for more information.

Radio Modes

The BCM20793S supports several modes of operation to enable the NFC use cases.

Initiator Mode

As the initiator in either R/W or Peer mode, the BCM20793S will generate the field used for communication. The size of the field is subject to the antenna used and the current drive of the BCM20793S. The peak antenna drive current is determined by the effective impedance of the antenna network and the voltage drive setting. The BCM20793S supports some variable drive levels to assist in power management. The antenna drive strength is software configurable with the range dependant on the internal voltage option chosen, as shown in Table 3.

Table 3: Antenna Drive Range

Internal Power Setting	Minimum	Maximum	Steps
Low Supply Reader Mode	35 mA pk	110 mA pk	3 dB
High Supply Reader Mode	70 mA pk	200 mA pk	3 dB

High Supply mode uses an internal analog rail of nominally 2.5V and Low Supply mode uses 1.88V, which can be monitored on the VDDA_CAP pin.

Mode Switch

Tag   Tag   Tag
Antenna coil

To discover the presence of a tag or a Peer mode target while operating in Initiator mode, the BCM20793S supports mode switch polling according to the NFC Forum "Activity" specification. Once set to active polling, the BCM20793S generates a field for a certain sequence of protocols and looks for a response.

For maximum flexibility and optimal power management, the duration that the BCM20793S generates a field at each interval is also firmware configurable. The Mode switch, as defined by the NFC Forum "Activity" specification, consists of a series of discovery periods and is configured according to the NFC Forum NFC Controller Interface (NCI) specification. Currently, NCI specifications highlight two parameters to define the discovery period used by the firmware.

- Listen Duration (acting as a target): May range from 0 ms to 65535 ms in 1 ms increments.
- Total Duration (total of acting as a target and acting as an initiator): May range from 0 ms to 65535 ms in 1 ms increments.

The time available for acting as an initiator is Total Duration – Listen Duration. If the initiator polls do not need all this allocated time, then the BCM20793S may enter a power saving mode.

By configuring these three parameters (technology, interval, and duration) the user can optimize the BCM20793S for their particular use case, and make the appropriate system-level response time- and power-consumption trade-offs. For further details on the power consumption used in polling, see Broadcom application note *Current Consumption While Polling* (see Reference [1] on page 9).

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The BCM20793S implements the NFC Forum-defined mode switch, which the host can use to configure and set the FW in the BCM20793S to periodically wake up and poll for targets of the various technology types.
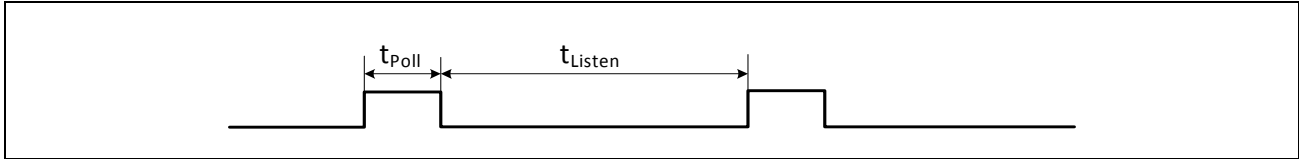
Figure 2: NFC Forum Mode Switch Polling and Listening

A typical poll cycle can be used to attempt to discover targets of NFC-A, NFC-B, and NFC-F. This involves generating the carrier field for approximately 38 ms and sending the REQA, REQB, and POLL_F commands to activate and illicit a response from any tags or peer mode targets that are present.
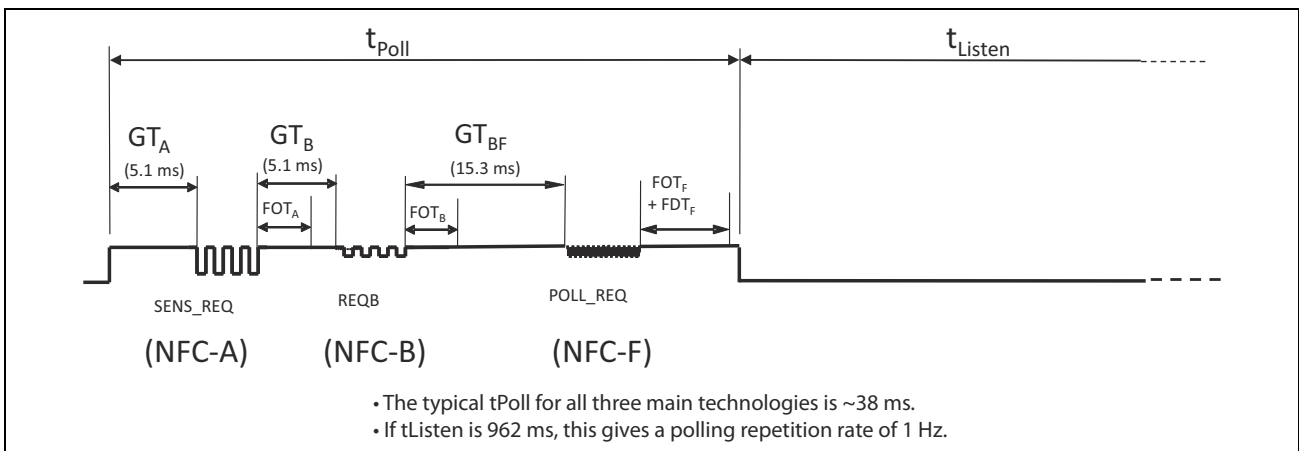
Figure 3: Forum Mode Switch Polling for NFC-A, NFC-B, and NFC-F

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During the time of each poll event, the BCM20793S draws a peak current from the VBAT supply. The level of this peak current depends on the characteristics of the antenna design and the environment of the antenna, as well as internal drive level and gain settings within the BCM20793S configuration.
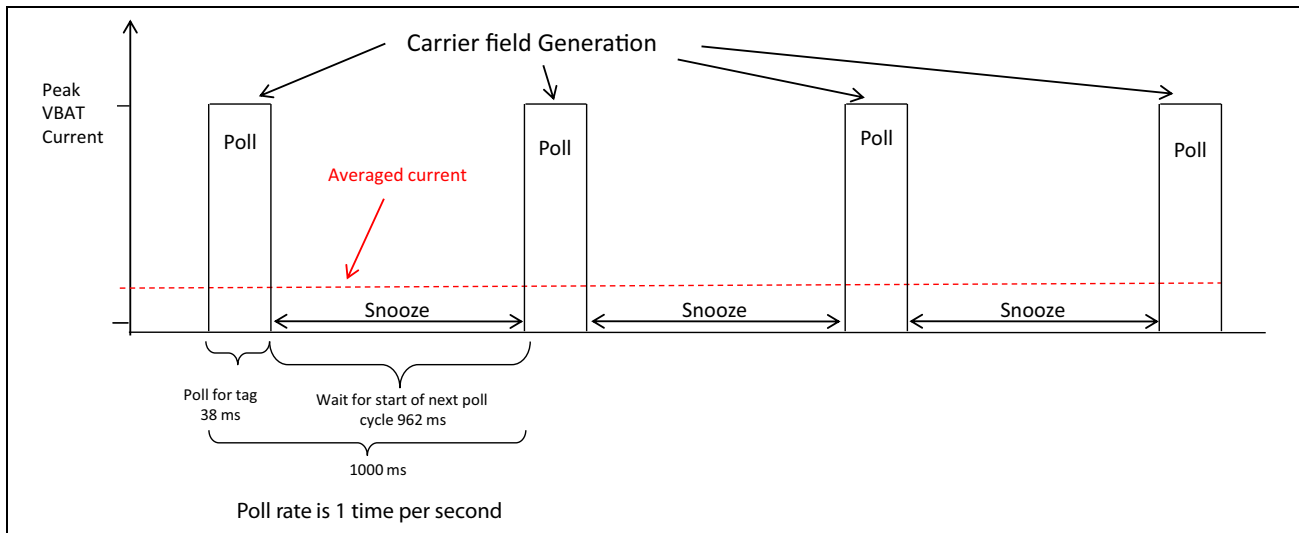
Figure 4: Representation of Averaged Duty-Cycle Current

Low Power Target Detection

The BCM20793S has the ability to use a Low Power Target Detection (LPTD) mode, where a target can be an NFC tag, card, or an NFC device in Listener mode, to save current consumption (see Figure 5 on page 19). In this mode, the device periodically wakes and tries to sense the presence of a tag. It does so without initiating a full A, B, and F poll. If a tag load is detected, then normal A, B, and F polling is initiated. If a load or change in environment is not detected, then the device returns to its snooze state. Broadcom can demonstrate a significant saving using this feature. Contact your local Broadcom representative for additional details.

To fully optimize battery power usage, Broadcom has developed an efficient time/current algorithm for detecting the presence of a target by the BCM20793S.

Instead of the conventional mode switch poll sequence, the BCM20793S can "sniff" for very brief durations to detect the presence of a tuned circuit or disturbance of the environment in the proximity of the NFC antenna. This results in a very much reduced duration of field generation and peak current drain from 38 ms to ~50 µs.

The "sniff" detects the presence of a target, but does not detect which technology type caused the trigger. The LPTD algorithm is always a precursor to a full poll event, which is used to qualify the trigger generated by the LPTD algorithm and discover the technology type just like a standard mode switch full poll event would.

A "false alarm rate" can occur when the LPTD can be triggered by metallic objects, but any trigger will be qualified by a full poll event and therefore can be discounted if it is not a real target.

The control algorithm includes a background calibration, so it auto-adjusts to a background baseline to account for drift and changing conditions.

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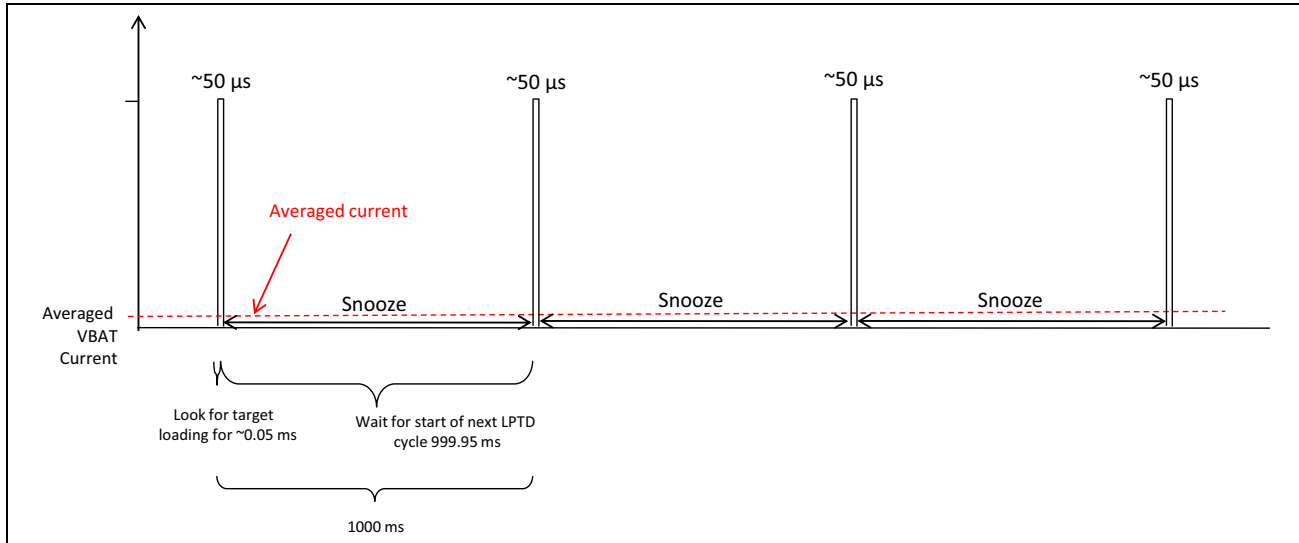
Figure 5: Principle of Low Power Target Detection (LPTD) Mode

Multiple Technology Support and Automatic Standard Detection

The BCM20793S has the ability to act as a Proximity Integrated Circuit Card (PICC) or Vicinity Integrated Circuit Card (VICC) for any of the technologies it supports (ISO/IEC 14443A, ISO/IEC 14443B, ISO/IEC 14443B-Prime, JIS (X) 6319-4, ISO/IEC 15693). The technology used is determined by both software configuration and the nature of the coupling device into the carrier field of which the BCM20793S is introduced.

The BCM20793S automatically detects and identifies, from the field generated by the initiator device, the technology that is requested. It then responds accordingly, assuming it has been configured by software to support a particular application on that given technology.

The BCM20793S has the capability of emulating targets of multiple technologies (A, B, F, ISO/IEC 15693, Calypso) at the same time. An NFC Forum initiator, following the activity specification, identifies all applications supported by targets in the field by polling using A, B, and F technologies. The initiator will then select one of the targets for subsequent communication.

The BCM20793S can emulate targets in two modes, and the mode can be changed over the NCI interface. In both modes, the BCM20793S supports emulation of multiple NFC-F targets.

In the default mode, the BCM20793S listen device maintains a single state machine and responds to the technology (A, B, F, ISO/IEC 15693, Calypso) of the first poll command that matches one of its emulated targets. After responding to this poll command, polls from other technologies are ignored until a carrier is dropped.

In the second mode, the BCM20793S listen device maintains multiple state machines and behaves virtually like multiple devices. This allows the host to have multiple applications listening at the same time, and announcing all of its applications to an NFC Forum initiator and not just the application of the first matching technology. For example, a BCM20793S-enabled device could announce both credit card emulation and LLCP. This is achieved by the BCM20793S responding to all polling commands (A, B, F, ISO/IEC 15693, Calypso) and only restrict itself to a specific technology once it has responded to the first non-polling command (A, B, F) or any ISO/IEC 15693 or Calypso command.

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Power Supply Topology

The BCM20793S integrates multiple LDO regulators and a Power Management Unit (PMU). All regulators are programmable via the PMU. These blocks simplify power supply design for NFC functionality in embedded designs. Main digital and analog regulator outputs are brought out to pins for decoupling.

A single VBAT (2.3V to 5.5V) and VDDIO (1.65V to 3.3V) can be used, with all additional voltages being provided by the regulators in the BCM20793S.

A control signal (REG_PU, regulator power-up) is used to power-up the regulators and take the respective section out of reset. This signal provides a method for the host to override the operational control of the internal LDOs. REG_PU operates on the VDDIO domain.

Applications that do not require control of the internal regulators can strap REG_PU to VDDIO.

Even with REG_UP deasserted, there is a low current always-on digital LDO that is used to keep-alive the state of important register settings within the front-end system. This uses residual power from the host battery to maintain the Card Emulation personality and persistence data.

NFC Power Management

The BCM20793S has been designed with the stringent power consumption requirements of mobile devices in mind. All areas of the chip design are optimized to minimize power consumption. The PMU, in conjunction with the local MCU and firmware, enables and disables internal regulators and circuit blocks depending on the requirements of the operating modes selected. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

The BCM20793S main power states are described as follows:

- Full power mode—All required regulators are enabled and the necessary circuit blocks are energized as required for the NFC operation mode. The BCM20793S and the host device operate in all NFC operating modes (i.e., Peer, Reader/Writer, and Card Emulation). There are various submodes within this level as required to optimize the transient power operation of the BCM20793S host interfaces, the MCU, and NFC subsystems.

- Snooze standby mode—During operation of the NFC Forum Mode Switch, in between the polling events, the BCM20793S enters snooze standby mode, where the analog LDO is off and all main clocks (PLL and crystal oscillator) are shut down to reduce active power to the minimum. Only the LPO clock is running and available for the PMU sequencer. This is used to allow the PMU sequencer to wake up the chip and transition to full-power mode for the next poll event. In snooze mode, all firmware patches and configuration data is retained ready to restart the MCU and the primary power consumed is due to leakage current.

  The carrier detector block is also running from the always-on LDO power domain to detect an external reader during the listen time in between polling events. When an external reader carrier field is detected, then the IC wakes up and enters Card Emulation and Peer Target modes.

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Card Emulation Power Modes

The BCM20793S has flexibility in its power modes to optimize NFC availability in card emulation (CE) mode to the user as the host battery capacity discharges and voltage level declines with time. As an option, this can extend to full Battery-off operation when the battery is deemed to be exhausted or even no longer present. The are two ways that the power levels can be controlled; either the BCM20793S can move between power modes under direct host control, or alternatively, the BCM20793S can be configured with a built-in V_{BATT} monitor circuit that can be pre-programmed by the host to have various pre-set voltage thresholds, such that when the battery voltage drops, the BCM20793S can automatically select and transition between the power level modes after the host is no longer available.

The BCM20793S can operate in CE mode with up to four sequential levels of battery power:

• CE Level 4 Power State
• CE Level 3 Power State
• CE Level 2 Power State
• CE Level 1 Power State

CE Level 4 Power State

Level 4 is the full battery voltage mode when the device operates in card emulation mode only and where the BCM20793S can be put into a very low power standby state, but still have the ability to alert the host for any CE transactions. It is lower current than the snooze standby state because the SoC is powered down, but boot time is a little slower compared to the snooze standby state, so the hardware must handle the initial part of the CE transaction.

CE Level 3 Power State

Level 3 is the residual power mode when the device operates in card emulation mode only. The operating power for the BCM20793S and Secure Element(s) is derived from the residual capacity of the battery supply. The preset tag personality and persistence data is retained in the NFC front-end registers, ready for immediate use.

CE Level 2 Power State

Level 2 is the partially field-powered mode when the device only operates in card emulation modes. All power required for the BCM20793S (and the designated Secure Element) is derived from energy harvested from the illuminating field. Residual power from the battery is only used for a very low current drain necessary to keep register data ready for immediate use.

CE Level 1 Power State

Level 1 is the fully field-powered mode where the device operates in card emulation mode only. This operating level will make use of the internal serial EEPROM. When the device is illuminated by a field and the BCM20793S harvests sufficient energy, the BCM20793S can retrieve the necessary personality and persistence data ready to respond to the reader/writer. The appropriate Secure Element is supplied with power from the BCM20793S, and the transaction can proceed to completion.

Devices without the battery-off personality storage medium may briefly enter Level 1, but the unsuccessful attempt to restore the personality and persistence data will abort communication.

Figure 6 shows how CE levels are mapped onto GSMA-recommended handset battery power regions.
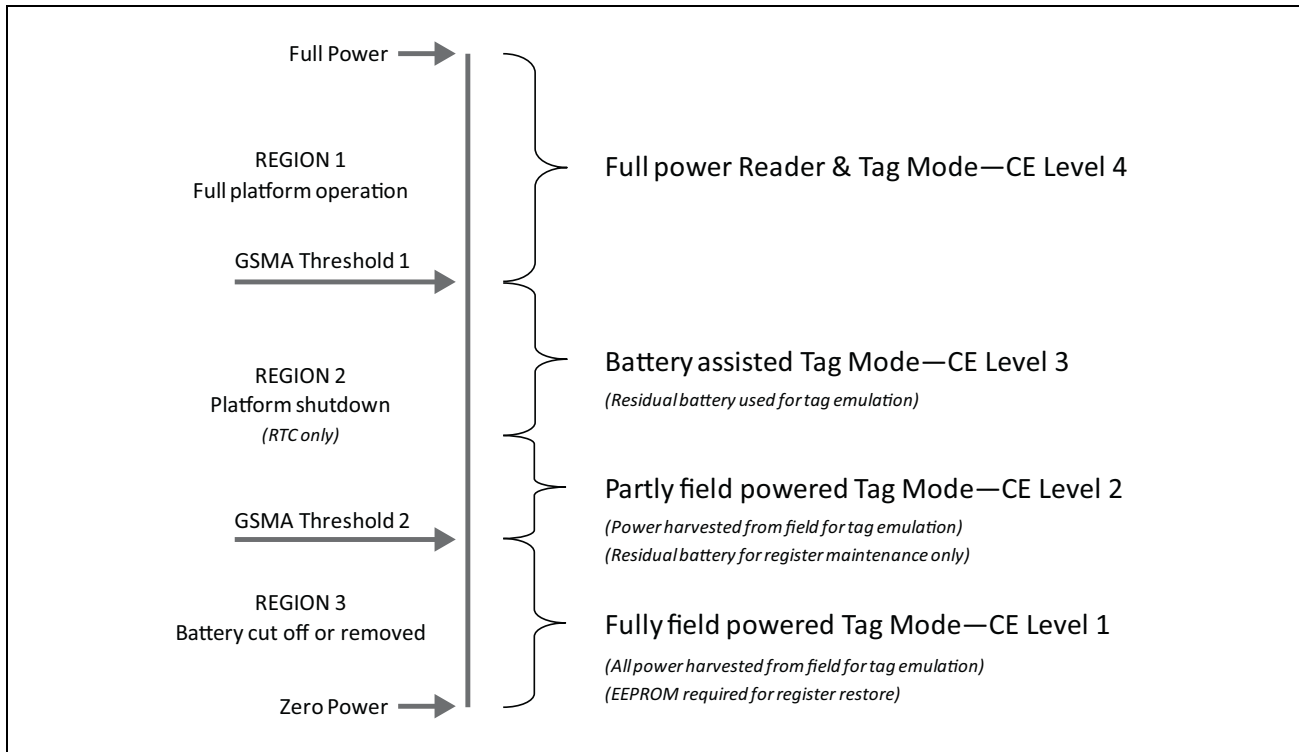
Figure 6: Mapping CE Levels

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CE Power Levels

Figure 7 shows how CE power levels can be controlled automatically by the internal VBAT monitor.
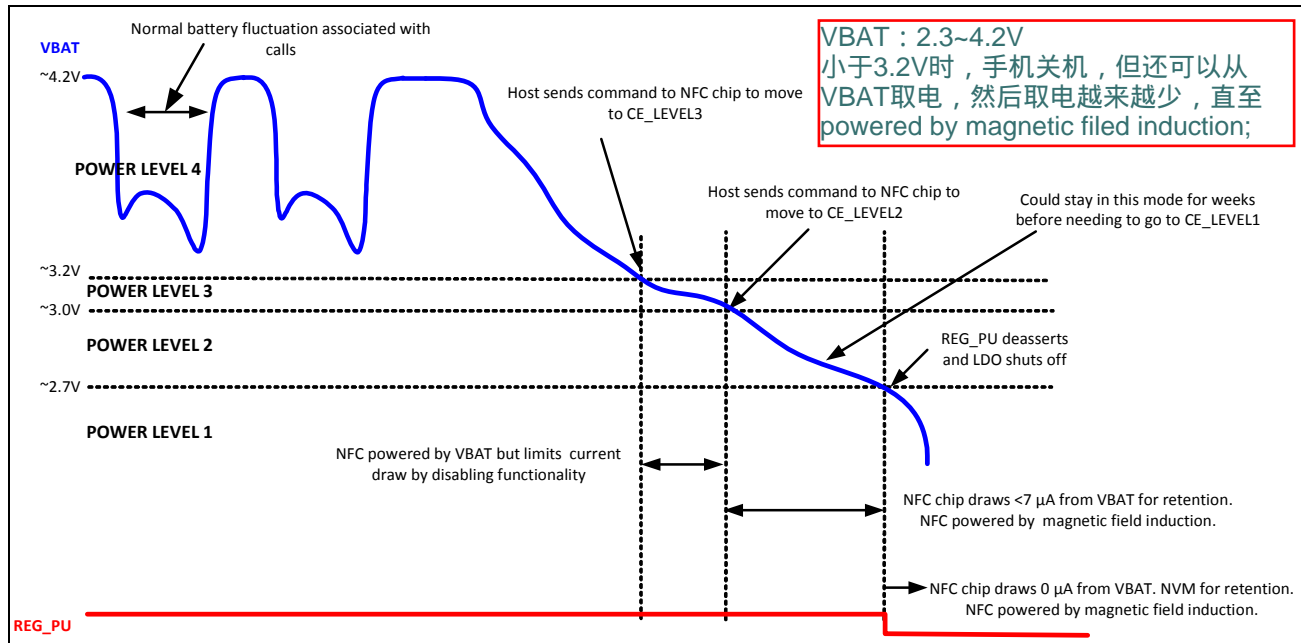
Figure 7: CE Power Level Control

Full Power Mode (R/W, P2P, and CE)

- System power is available and maintains NFC IP registers.
- The host devices and host interface transport are active.
- The Secure Element (UICC) is powered.

Snooze Standby Mode

- System power is available and maintains NFC IP registers.
- The host has issued the SLEEP command.
- The low-power oscillator wakes up periodically for mode switch polling and LPTD.
- The carrier detector wakes up in CE mode when a reader is detected.

CE Level 4 (CE Only)

- System power is available, but only used to maintain NFC registers.
- The host has issued the SLEEP command and the host interface transport is inactive.
- The carrier detector wakes up in CE mode when a reader is detected.
- The device must boot up the configuration and patch the download before operation. Transactions begin using hardware for time critical elements until the firmware is up.

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CE Level 3, Residual Battery Mode/Battery Assisted Mode (CE Only)

- The host device is inactive.
- System power is available at a reduced current for CE functionality.
- The Secure Element operates in low power mode, as defined in TS 102 613.

CE Level 2, Residual Battery Mode/Partly Field-Powered Mode (CE Only)

- System power is used for register maintenance only.
- Power is harvested for actual card emulation and UICC SE operating in low power mode.
- Allows for very long life on residual battery.

CE Level 1, Battery Off/Field Power Harvesting Mode (CE Only)

- No system power is available, registers are dead.
- Persistence data registers are restored from EEPROM.
- Power is harvested for everything.

Table 4: Power Sources in CE Levels

Power Mode Level	Reader Subsystem	Persistence Registers	Tag Subsystem	UICC or eSE
Full power initiator/ target (CE Level 4)	VBAT	VBAT	VBAT	VBAT
Battery assisted (CE Level 3)	–	VBAT	VBAT	VBAT
Partly field powered (CE Level 2)	–	VBAT	Field powered	Field powered
Fully field powered (CE Level 1)	–	–	Field powered	Field powered

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Power transitions controlled by the host are defined in Table 5.

Table 5: Transitions Controlled by the Host

Power State Name	VDDIO Present?	REG_PU State	Entry	Host Condition	Host Involvement	Description	NFC Modes Available	NFC Power	SE Power	Register Power	EEPROM Required
Full Power	Yes	REG_PU = 1	Boot-up	Handset Active **Note:** Depending on requirements, can also be in Idle (screen off) with LPTD running.	Yes, by HOST_WAKE	Full Power mode — All required regulators are enabled and the necessary circuit blocks are energized as required for the NFC operation mode. The BCM20793S and the host device operate in all NFC operating modes (that is, Peer, Reader/Writer, and Card Emulation). There are various submodes within this level as required to optimize the transient power operation of the BCM20793S host interfaces, the MCU, and NFC subsystems.	R/W, P2P, and CE	VBAT	VBAT	VBAT	No
Snooze Standby	Yes	REG_PU = 1	Host command	Handset Active **Note:** Depending on requirements, can also be in Idle (screen OFF) with LPTD running.	Yes, by HOST_WAKE	Snooze Standby mode — During operation of the NFC Forum Mode Switch, in between the polling events, the BCM20793S enters snooze standby mode, where the analog LDO is off and all main clocks (PLL and crystal oscillator) are shut down to reduce active power to the minimum. Only the LPO clock is running and available for the PMU sequencer. This is used to allow the PMU sequencer to wake up the chip and transition to Full-power mode for the next poll event. In Snooze mode, all firmware patches and configuration data is retained ready to restart the MCU and the primary power consumed is due to leakage current. The carrier detector block is also running from the always-on LDO power domain to detect an external reader during the listen time in between polling events. When an external reader carrier field is detected, then the IC wakes up and enters Card Emulation and Peer Target modes.	R/W, P2P, and CE	VBAT	VBAT	VBAT	No

Table 5: Transitions Controlled by the Host (Cont.)

Power State Name	VDDIO Present?	REG_PU State	Entry	Host Condition	Host Involvement	Description	NFC Modes Available	NFC Power	SE Power	Register Power	EEPROM Required
CE4	Yes	REG_PU=1	Host command	Handset Idle (screen OFF) **Note:** Current solution on Android (handbag mode)	Yes by HOST_WAKE	Level 4 is the full battery voltage mode, in which the device operates in card emulation mode only, and where the BCM20793S can be put into a very low-power standby state, but still have the ability to alert the host for any CE transactions. Current is lower than in the Snooze Standby state because the SoC is powered down, but boot time is a little slower compared to the Snooze Standby state, so the hardware must handle the initial part of the CE transaction.	CE only	VBAT	VBAT	VBAT	No
CE3	Yes	REG_PU = 1	Host Command	Not defined	No	Level 3 is the residual power mode, in which the device operates in card emulation mode only. The operating power for the BCM20793S and Secure Element(s) is derived from the residual capacity of the battery supply. The preset tag personality and persistence data is retained in the NFC front-end registers, ready for immediate use.	CE only	VBAT	VBAT	VBAT	No
CE2	Yes	REG_PU = 1	Host Command	Not defined	No	Level 2 is the partially field-powered mode, in which the device only operates in card emulation modes. All power required for the BCM20793S (and the designated Secure Element) is derived from energy harvested from the illuminating field. Residual power from the battery is only used for a very low current drain necessary to keep register data ready for immediate use.	CE only	Field	Field	VBAT	No
CE1	No	Or REG_PU = 0	Or Battery Removed	Handset OFF	No	Level 1 is the fully field-powered mode where the device operates in card emulation mode only. This operating level requires the option of a small-capacity serial EEPROM IC. When the device is illuminated by a field and the BCM20793S harvests sufficient energy, the BCM20793S can retrieve the necessary personality and persistence data ready to respond to the reader/writer. The predesignated Secure Element is supplied with power from the BCM20793S, and the transaction can proceed to completion.	CE only	Field	Field	Field	Yes

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Power transitions controlled through the VBAT Monitor are defined in Table 6. For VBAT Monitor-controlled transitions, the CE3-CE2 threshold can be configured in a range of 5.2–2V (the default is 3.2V), and the CE2-CE1 threshold can be configured in a range 3.2–2V (the default is 3.0V).

Table 6: Transitions Controlled Through the VBAT Monitor

Power State Name	VDDIO present	REG_PU state	Entry	Host Condition	Host Involvement	Description	NFC Modes Available	NFC Power	SE Power	Register Power	EEPROM Required
Full Power	Yes	REG_PU = 1	Boot-up	Handset Active	Yes, by HOST_WAKE	Full power mode — All required regulators are enabled and the necessary circuit blocks are powered as required for the NFC operation mode. The BCM20793S and the host device operate in all NFC operating modes (that is, Peer, Reader/Writer, and Card Emulation). There are various submodes within this level as required to optimize the transient power operation of the BCM20793S host interfaces, the MCU, and NFC subsystems.	R/W, P2P, and CE	VBAT	VBAT	VBAT	No
Snooze Standby	Yes	REG_PU = 1	Host command	Handset Active **Note:** Depending on requirements, can also be in Idle (screen off) with LPTD running.	Yes, by HOST_WAKE	Snooze standby mode — During operation of the NFC Forum Mode Switch, in between the polling events, the BCM20793S enters Snooze Standby mode, where the analog LDO is off and all main clocks (PLL and crystal oscillator) are shut down to reduce active power to the minimum. Only the LPO clock is running and available for the PMU sequencer. This is used to allow the PMU sequencer to wake up the chip and transition to Full Power mode for the next poll event. In Snooze Standby mode, all firmware patches and configuration data are retained ready to restart the MCU. The primary power consumed is due to leakage current. The carrier detector block is also running from the always-on LDO power domain to detect an external reader during the listen time in between polling events. When an external reader carrier field is detected, then the IC wakes up and enters Card Emulation and Peer Target modes.	R/W, P2P, and CE	VBAT	VBAT	VBAT	No

Table 6: Transitions Controlled Through the VBAT Monitor

Power State Name	VDDIO present	REG_PU state	Entry	Host Condition	Host Involvement	Description	NFC Modes Available	NFC Power	SE Power	Register Power	EEPROM Required
CE4	Yes	REG_PU = 1	Host command	Handset Idle (screen OFF) **Note:** Current solution on Android (handbag mode)	Yes, by HOST_WAKE	Level 4 is the full battery voltage mode in which the device operates in card emulation mode only, and where the BCM20793S can be put into a very low-power standby state, but still have the ability to alert the host for any CE transactions. It is lower current than the Snooze Standby state because the SoC is powered down, but boot time is a little slower compared to the Snooze Standby state, so the hardware must handle the initial part of the CE transaction.	CE only	VBAT	VBAT	VBAT	No
CE3	X	REG_PU = 0	Host Command and REG_PU=0	Handset OFF	No	Level 3 is the residual power mode in which the device operates in card emulation mode only. The operating power for the BCM20793S and Secure Element(s) is derived from the residual capacity of the battery supply. The preset tag personality and persistence data is retained in the NFC front-end registers, ready for immediate use.	CE only	VBAT	VBAT	VBAT	No
CE2	X	REG_PU = 0	Vbatt < Threshold CE3-C2	Handset OFF	No	Level 2 is the partially field-powered mode in which the device only operates in the card emulation modes. All power required for the BCM20793S (and the designated Secure Element) is derived from energy harvested from the illuminating field. Residual power from the battery is only used for a very low current drain necessary to keep register data ready for immediate use.	CE only	Field	Field	VBAT	No
CE1	X	REG_PU = 0	VBAT < Threshold CE2-CE1 or Battery Removed	Handset OFF	No	Level 1 is the fully field-powered mode where the device operates in card emulation mode only. This operating level requires the option of a small-capacity serial EEPROM IC. When the device is illuminated by a field and the BCM20793S harvests sufficient energy, the BCM20793S can retrieve the necessary personality and persistence data ready to respond to the reader/writer. The predesignated Secure Element is supplied with power from the BCM20793S, and the transaction can proceed to completion.	CE only	Field	Field	Field	Yes

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Secure Element Configuration Options

Figure 8 shows the NFC secure element configuration.
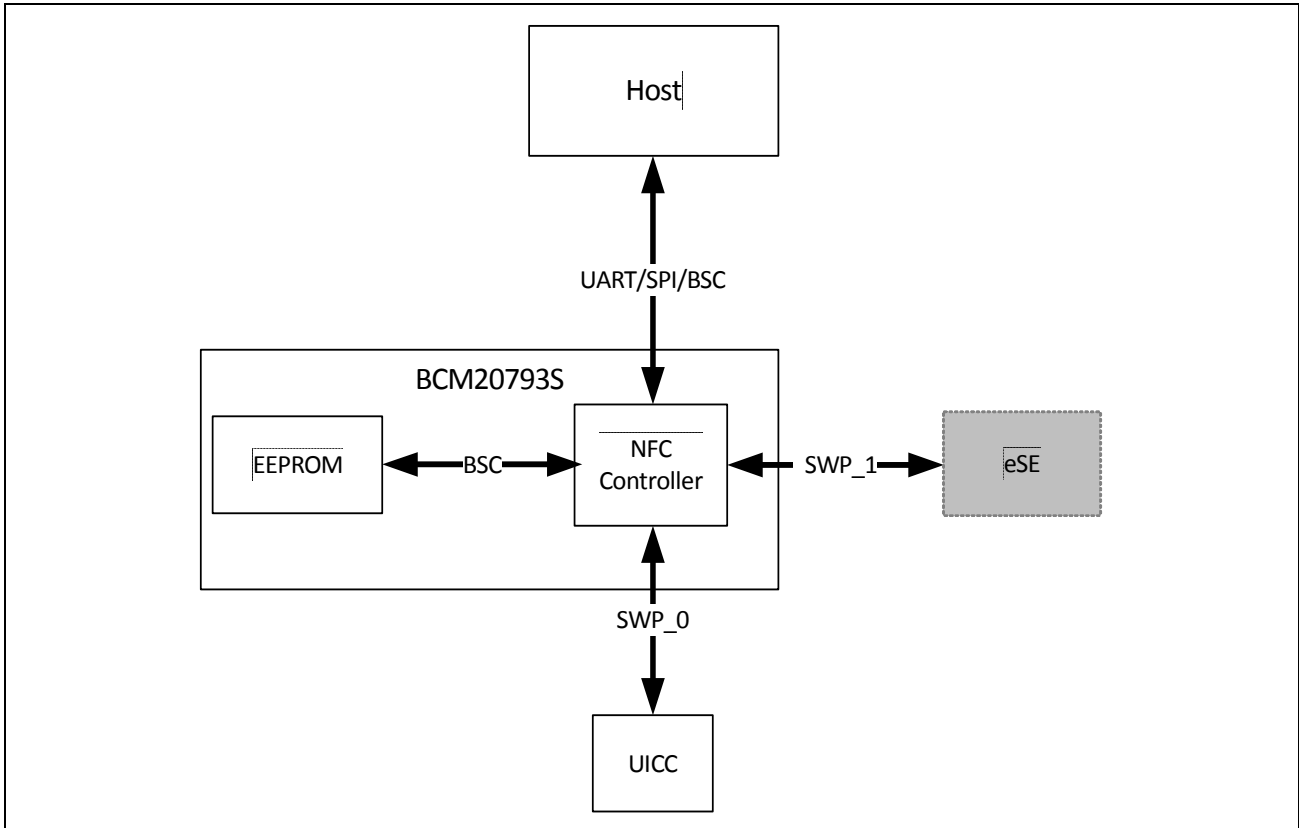
Figure 8: NFC Secure Element Configuration

Battery-off Source of Personality and Persistence Data

For CE mode level 1 (field-powered operation), the BCM20793S requires a source of pre-configured storage for personality and persistence data. The BCM20793S uses the integral EEPROM to provide this.

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Section 3: Interfaces

Host Interfaces

Host Interface Selection

The BCM20793S supports UART, BSC (I^2C-compatible), and SPI for the host interface transport physical layer.

The host interface type is selected on power up depending on the state of pin 15:
- Pin 15 strapped low — UART
- Pin 15 strapped high — BSC
- Pin 15 floating — SPI

After boot, this becomes SPI_INT output. During boot, the host must leave pin 15 floating (like a tri-state or input). The host must ignore interrupts from this line for 10 ms until after boot-up.

The interface signals are multiplexed onto common pins, as shown in Table 7.

Table 7: Host Interface Transport Selection

Pin	UART	BSC	SPI
15	Strap low	Strap high	Floating at boot-up, then becomes SPI_INT output
12	UART_TXD	I2C_SDA	SPI_MOSI
14	UART_RTS_N	I2C_SCL	SPI_MISO
16	UART_CTS_N	I2C_REQ	SPI_CS
17	UART_RXD	–	SPI_CLK

UART

Following are the main features for the BCM20793S UART:

- UART 2-wire/4-wire: RXD, TXD, RTS, CTS
- Default baud rate is 115200 bps, host may change adjustable baud rates from 9600 bps to 3.0 Mbps
- RTS and CTS hardware flow control is supported
- Hardware auto baud circuit: Applications using this UART auto baud feature at other than the pre-defined frequencies (9.6, 13, 26, 19.2, 38.4, 52 MHz) should have the NFC_WAKE pin pulled low on power-up.
- Optional in-band Xon/Xoff flow control
- 272-byte transmit FIFO and 272-byte receive FIFO
- Supports 8-bit characters with 1 or 2 stop bits and no parity

The UART timing waveform is shown in Figure 9.
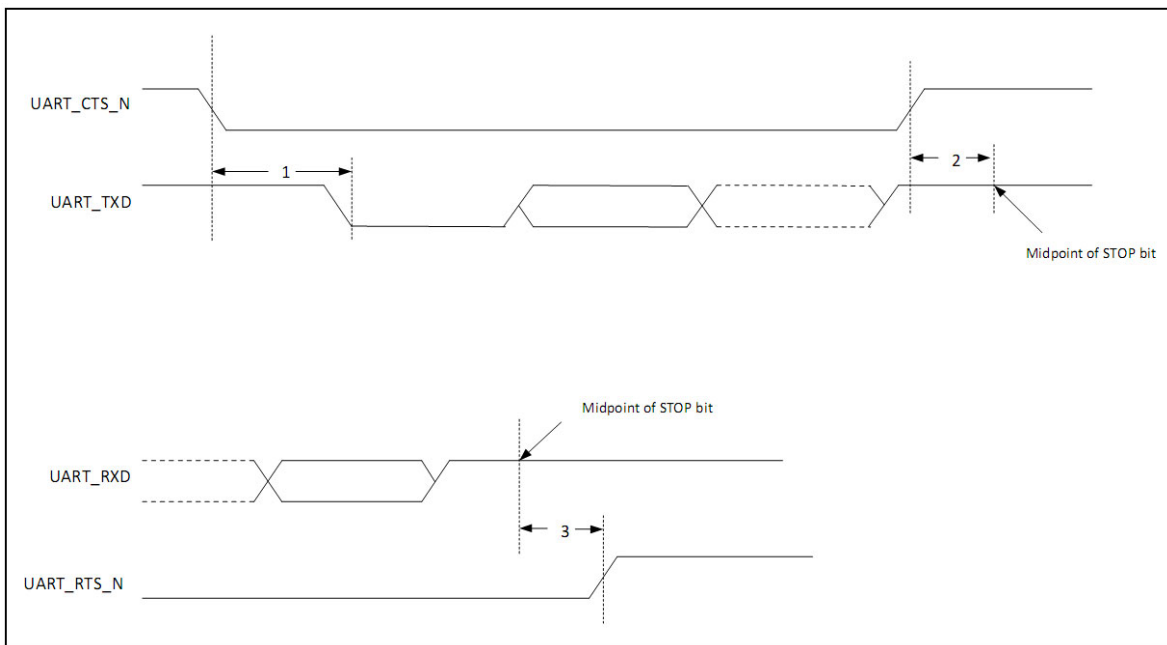
Figure 9: UART Timing Waveform

The UART host interface is shown in Figure 10 and the pins are described in Table 8.
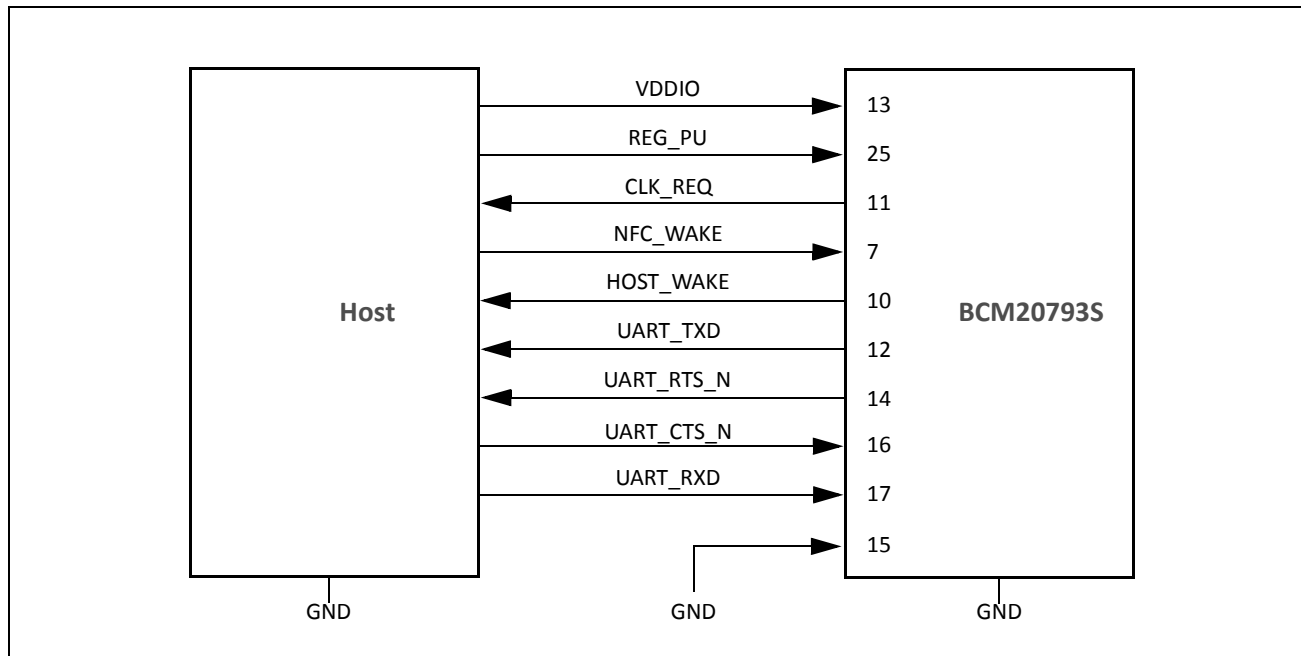
Figure 10: UART Host Interface

Table 8: UART Host Interface Pin Operation

Name	Pin	I/O	Polarity	Description
VDDIO	13	P	–	I/O supply; externally regulated.
REG_PU	25	I	Active high	Regulator power up. Low: Shut down with all LDOs off (battery-off still functional). High: LDOs are available.
CLK_REQ	11	O	Active high (Not configurable)	Clock request. Signal to host requesting that it generate a reference clock input. Also a request to host PMU to power the UICC (SIM) card.
NFC_WAKE	7	I	Default is rising edge triggered. (Configurable for falling edge.)	NFC wake-up. If the BCM20793S is asleep, then the active edge will wake it up. The BCM20793S can subsequently re-enter sleep mode when it has no more activities to do. Internal 50 kOhm pull-up; must be held low at device power-up.
HOST_WAKE	10	O	Active high	Host wake-up. A means for the chip to alert the host if the BCM20793S wants to communicate with the host.
UART_TXD	12	O	–	UART Transmit Data from BCM20793S to host.
UART_RTS_N	14	O	Active low	UART request to send signal from BCM20793S to host that the BCM20793S is ready to accept receive data.
UART_CTS_N	16	I	Active low	UART clear to send signal from host to BCM20793S that the BCM20793S should send transmit data.
UART_RXD	17	I	–	UART Receive Data from host to BCM20793S.

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Table 8: UART Host Interface Pin Operation (Cont.)

Name	Pin	I/O	Polarity	Description
–	15	I	–	Host interface mode control pin. Strapped to ground at boot up = UART.

BSC (I^{2}C-Compatible)

If using IIC bus, NFC IIC bus is special and do not share with other module;

Following are the main features of the BCM20793S BSC host interface:

• Slave mode

• Low-speed mode (100 kbps), fast mode (400 kbps), and high-speed mode (3.4 Mbps) supported. Due to practical constraints imposed by parasitic capacitance and pull-up resistor values, especially in a multi-drop system, Broadcom engineers recommend that this be limited to 1.7 Mbps.

• 7-bit or 10-bit addressing mode; default boot-up of fixed 10-bit address (0x1FA), thereafter configurable to 7-bit or 10-bit addresses

• Dedicated TX and RX FIFOs, 272 bytes each.

• Digital deglitching filter implemented. Uses simple majority of 3 and will filter spikes up to 42 ns.

• High-speed reference not required for operation. (Certain accesses in sleep mode will initiate the wakeup function.)

The BSC timing waveform is shown in Figure 11.
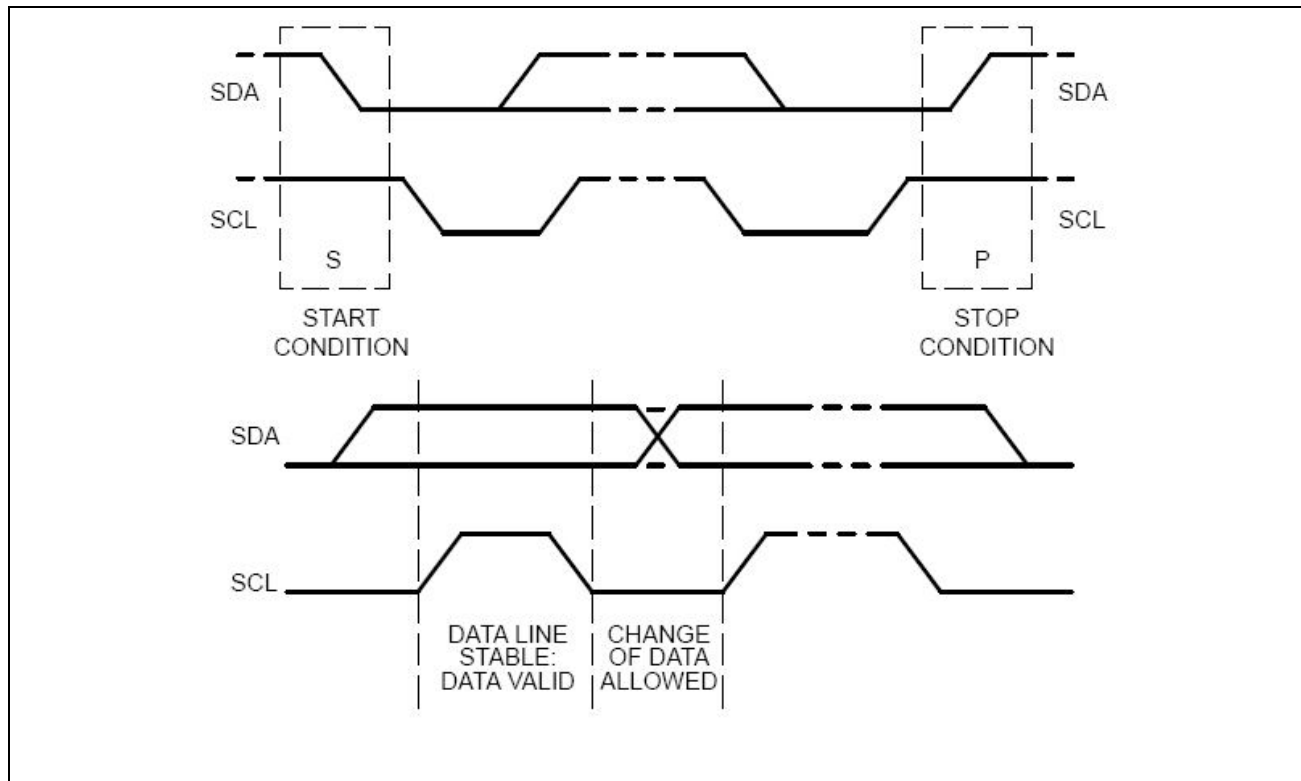
Figure 11: BSC Timing Waveform

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I2C_REQ is an output signal from the BCM20793S to the host that it wishes to communicate. The timing diagram in Figure 12 shows I2C_REQ as active high.

The I2C_REQ signal stays high until after the first byte has been read by the host.
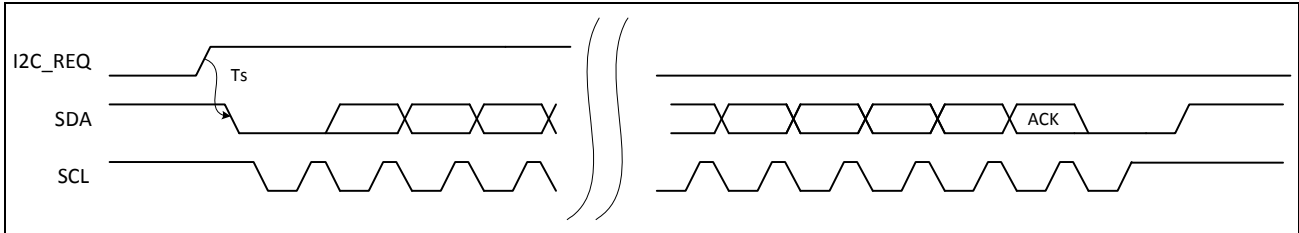
Figure 12: I2C_REQ Timing Waveform

Table 9: I2C_REQ Timing Parameters

Symbol	Description	Minimum	Maximum	Unit
Ts	Rising edge of I2C_REQ to first SDA start	0	–	ns

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The BSC host interface is shown in Figure 13 and the pins are described in Table 10.
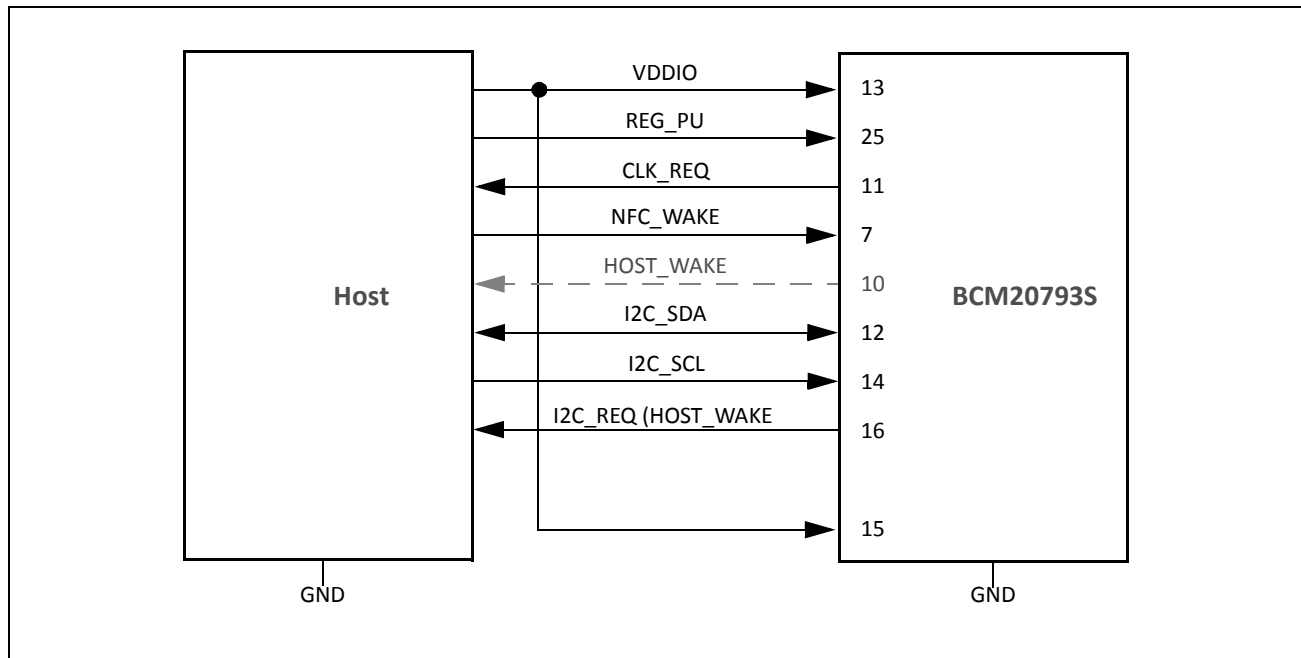
Figure 13: BSC Host Interface

Table 10: BSC Host Interface Pin Operation

Name	Pin	I/O	Polarity	Description
VDDIO	13	P	–	I/O supply; externally regulated.
REG_PU	25	I	Active high	Regulator power up. Low: Shut down with all LDOs off (battery-off still functional). High: LDOs are available.
CLK_REQ	11	O	Active high (Not configurable)	Clock request. Signal to host requesting that it generate a reference clock input. Also a request to host PMU to power the UICC (SIM) card.
NFC_WAKE	7	I	Default is rising edge triggered. (Configurable for falling edge.)	NFC wake-up. If the BCM20793S is asleep, then the active edge will wake it up. The BCM20793S can subsequently re-enter sleep mode when it has no more activities to do. Internal 50 kOhm pull-up; must be held low at device power-up.
HOST_WAKE	10	O	–	Not necessary. Use I2C_REQ instead.
I2C_SDA	12	I/O	Active low	BSC Serial Data Line, bidirectional serial data between the host and the BCM20793S.
I2C_SCL	14	I	–	BSC Serial Clock, generate by host to the BCM20793S.
I2C_REQ	16	O	Active high	BSC Request, signal from the BCM20793S to the host that it needs to communicate.
–	15	I	–	Host interface mode control pin. Strapped to VDDIO at boot up = BSC.

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SPI

The following are the main features of the BCM20793S Serial Peripheral Interconnect (SPI) interface.

The physical interface between the SPI master and the BCM20793S consists of the four SPI signals (SPI_CLK, SPI_MOSI, SPI_MISO, and SPI_CS) and one interrupt signal (SPI_INT). The BCM20793S can be configured to accept active-low or active-high polarity on the SP_CS chip select signal, and it can also be configured to drive an active-low or active-high SPI_INT interrupt signal. The SPI _INT signal facilitates packet level flow control. In addition, the bit ordering on the data lines (SPI_MOSI and SPI_MISO) can be configured to be either little-endian or big-endian. A proprietary sleep mode half-duplex handshaking is implemented between the SPI master and the BCM20793S.

The key characteristics of the SPI slave controller include the following:
- Support for SPI modes 0, 1, 2, and 3. Default mode is 0.
- Support for normal SPI bit ordering (MSB first)
- Allows operation with a wide range of host-generated SPI clock frequencies (up to 16 MHz). Optional interrupt generation when the host needs to service the SPI slave.
- Makes SPI look like a UART to host software (facilitates device driver creation)
- Includes FIFOs to accommodate software bursts (minimizes bus overhead)

The possible SPI modes are shown in Figure 14. The Host decides which SPI mode to use and notifies the device of the selection by the first message transferred to the device. This first message is completed using SPI mode 0 timing (CPOL = 0, CPHA = 0).
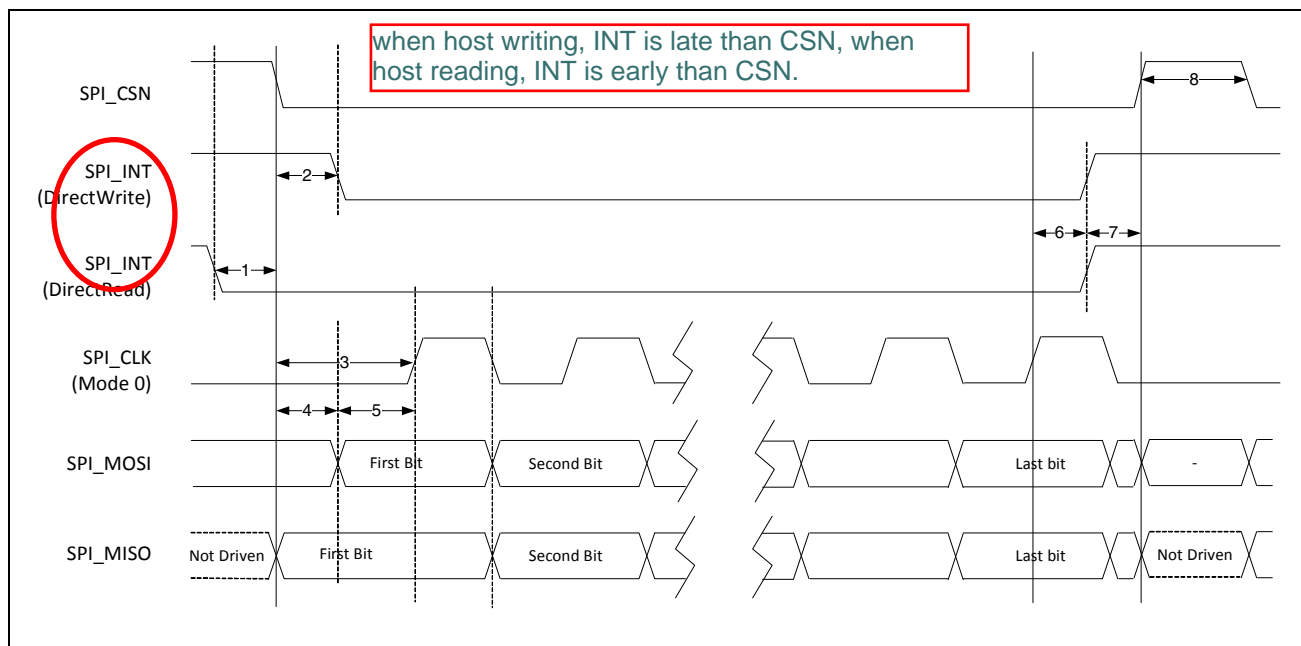
Figure 14: SPI Timing Diagram

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Table 11 contains timing information for SPI Mode 0.

Table 11: SPI Timing Details

Reference	Description	Minimum	Maximum	Unit
1	The time at which the slave asserts SPI_INT to the time at which the master asserts SPI_CSN (DirectRead)	0	–	ns
2	The time at which the master asserts SPI_CSN to the time at which the slave asserts SPI_INT (DirectWrite)	0	–	ns
3	The time at which the master asserts SPI_CSN to the first clock edge	20	–	ns
4	Set-up time for the MOSI data lines	8	SCK × 0.5	ns
5	Hold time for the MOSI data lines	8	SCK × 0.5	ns
6	The time at which the last sample is taken from MOSI/MISO to the time at which the slave deasserts SPI_INT	0	100	ns
7	The time at which the slave deasserts SPI_INT to the time at which the master deasserts SPI_CSN	0	–	ns
8	Idle time between subsequent SPI transactions	SCK × 1	–	ns

Note:

1. SPI_CS Hold time is based on reference 7 in Figure 14 on page 36. SPI_CSN should be held active until SPI_INT is deasserted. Broadcom engineers recommend that a minimum of 20 ns be allowed for deassertion after the last clock edge of SPI_CLK.

2. MISO typically has valid data 10.3 ns after the falling edge of SPI_CLK. Broadcom engineers recommend that a minimum of 20 ns be allowed for MISO to have valid data.

3. MISO is held valid until the next falling edge of the clock, which equates to $^1/_2$ of the clock period in relation to the rising (sampling) edge of the clock.

4. Time when SPI_MISO becomes invalid: MISO is tri-stated when SPI_CSN goes inactive, at which point SPI_MISO becomes invalid (100 ns maximum). See reference 6 in Figure 14 on page 36.

When the device host (master) wants to write data to the BCM20793S (slave):

1. The device host sets SPI_CS = 0.

2. The BCM20793S acknowledges this by setting SPI_INT = 0.

3. Data transfer takes place on the SPI_MOSI and SPI_MOSO lines.

4. The BCM20793S sets SPI_INT = 1.

5. The device host sets SPI_CS = 1.

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When the BCM20793S wants to send data to device host:

1. The BCM20793S sets SPI_INT = 0.

2. The device host acknowledges this by setting SPI_CS = 0.

3. Data transfer takes place on the SPI_MOSI and SPI_MOSO lines.

4. The BCM20793S sets SPI_INT = 1.

5. The device host sets SPI_CS = 1.

The SPI host interface is shown in Figure 15 and the pins are described in Table 12.
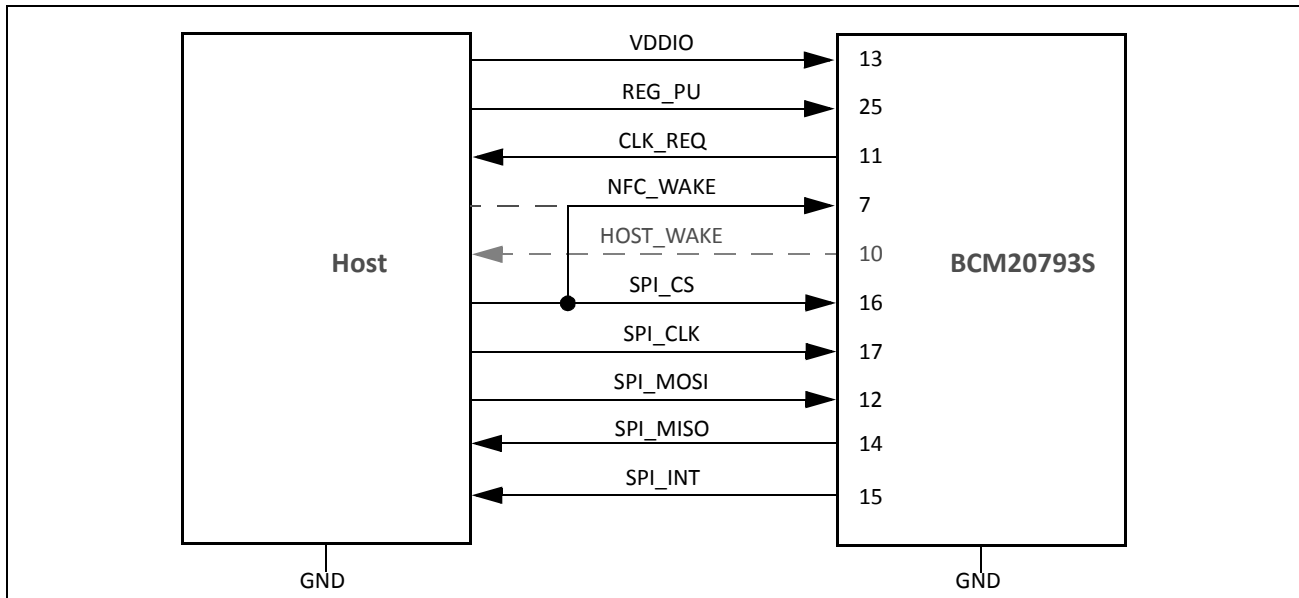
Figure 15: SPI Host Interface

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Table 12: SPI Host Interface Pin Operation

Name	Pin	I/O	Polarity	Description
VDDIO	13	P	–	I/O supply; externally regulated.
REG_PU	25	I	Active high	Regulator power up. Low: Shut down with all LDOs off (battery-off still functional). High: LDOs are available.
CLK_REQ	11	O	Active high (Not configurable)	Clock request. Signal to host requesting that it generate a reference clock input. Also a request to host PMU to power the UICC (SIM) card.
NFC_WAKE	7	I	Default is rising edge triggered. (Configurable for falling edge.)	NFC wake-up. If the BCM20793S is asleep, then the active edge will wake it up. The BCM20793S can subsequently re-enter sleep mode when it has no more activities to do. Internal 50 kOhm pull-up; must be held low at device power-up. Can be joined to SPI_CS.
HOST_WAKE	10	O	–	Not used.
SPI_MOSI	12	O	–	SPI Master Out Slave In, serial data signal from host to BCM20793S.
SPI_MISO	14	I	–	SPI Master In Slave Out, serial data signal from BCM20793S to host.
SPI_CS	16	I	Active low	SPI Chip Select, signal from host to BCM20793S to enable SPI slave interface block onto bus.
SPI_CLK	17	I	–	SPI Clock, generate by host to the BCM20793S.
SPI_INT	15	O	Active low	Host interface mode control pin. Host should power up first and ensure that this line is floating during BCM20793S power up. After boot up this becomes an output. The host shall ignore this signal for up to 10 ms after power up. SPI Interrupt signal from the BCM20793S that it wants to communicate.

Secure Element Interfaces

Single Wire Protocol

The BCM20793S supports two entirely independent SWP data and power supply interfaces, which are labeled as SWP_0 and SWP_1 (see Figure 16 on page 41). The SWP_0 interface supports both Class B and Class C Universal Integrated Circuit Cards (UICCs). The SWP_1 interface supports 1.8V secure elements.

- Master mode
- Extended bit-rate support: 1.507 Mbps. (The maximum speed achievable will be dependant on the level of parasitic capacitance due to PCB tracking on any particular design implementation.)
- Host programmable high impedance or pull down on pin (default is pull-down)
- Dedicated RX and TX 32-byte frame buffers

Power for the UICC connected to the SWP_0 interface can be supplied as follows:

- Derived from the host platform PMU via VDDSWP_IN at 1.8V and 3V. PMU   VDDSWP_IN   Chip   SWP_0
- Derived from VBAT via internal regulators at 1.8V. VBAT   Chip   LDO   SWP_0
- Derived from field power at 1.8V.   Chip   AC-DC   SWP_0

Power for the secure element connected to the SWP_1 interface can be supplied as follows:

- Derived from VBAT through internal regulators at 1.8V.
- Derived from field power at 1.8V.

> **Note:** In low-power card emulation modes, only one SWP interface may be used at a time. In full-power modes, if it is required that both SWP interfaces are used at the same time, then SWP_0 power must be derived from the host platform PMU via VDDSWP_IN.

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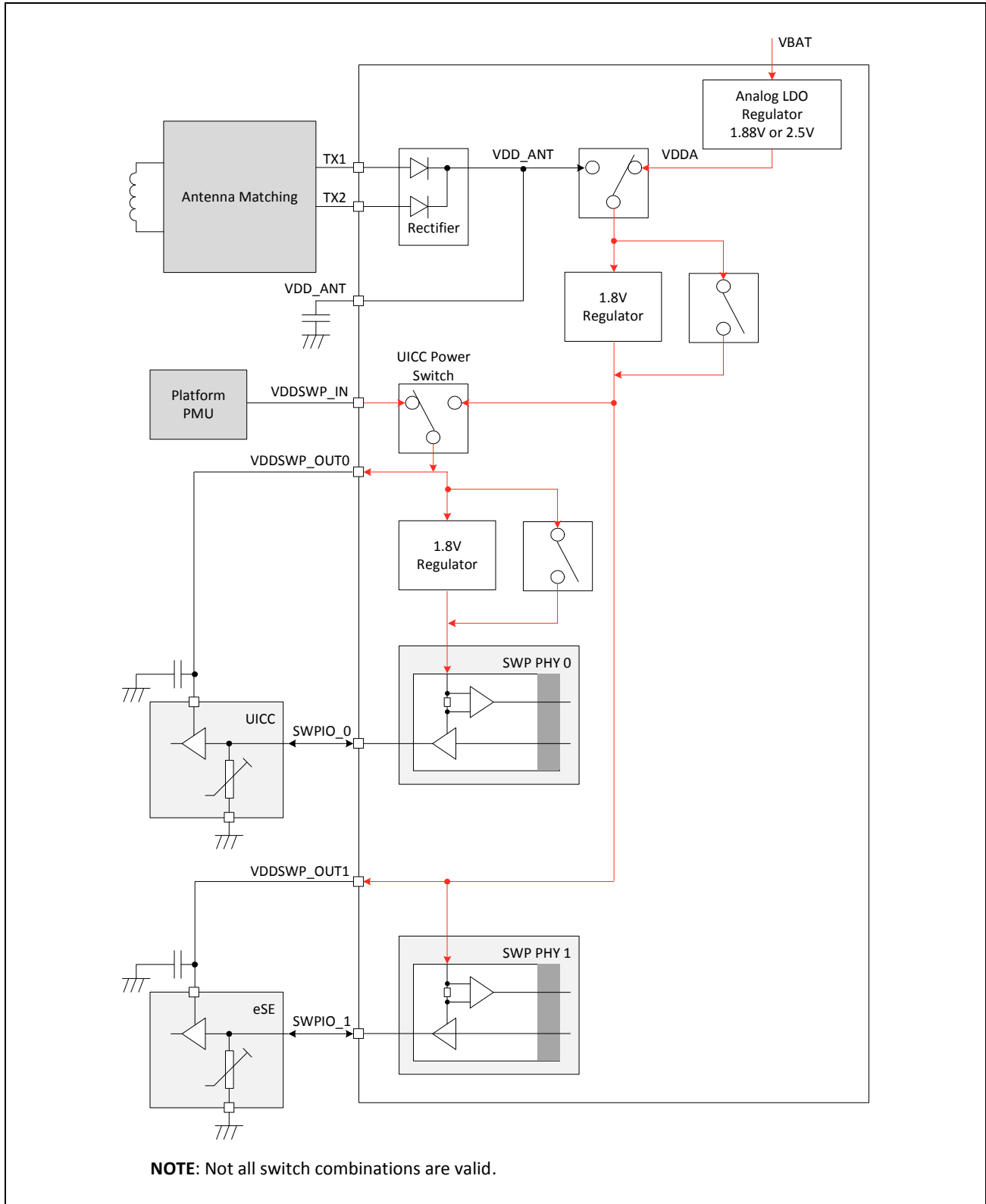
Figure 16: Secure Element Power Switching Architecture

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The Single Wire Protocol (SWP) interfaces implemented in the BCM20793S are compatible with ETSI TS 102 613. This provides connectivity to a SWP-enabled SIM card or UICC for Tag Emulation and Reader modes. They are available in both Battery-On and Battery-Off modes, but Reader mode is supported only in Battery-On mode.

The BCM20793S is able to detect the presence of a standards-compliant UICC interface. This is accomplished by proceeding through the initialization process. The BCM20793S puts the SWP in ACTIVATED state. When it receives the ACT_SYNC over the SWP interface, a correct interface connection is confirmed.

The SWP interface protocols conform to ETSI 102-613 v9.1.0 and ETSI 102-622 v9.0.0.

Nonvolatile Memory Interface

This interface is used internally for the co-packaged EEPROM. Pull-up resistors are required on the SCL and SDA pins to the VDD_EE pin.

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Section 4: Microprocessor and Memory Unit

The microprocessor core is based on the ARM CM0 processor. It runs embedded software from the link control (LC) layer up to the NFC controller interface (NCI). The ARM core is paired with a memory unit that contains 128 KB of ROM for program storage and boot ROM and 19 KB of RAM.

Configuration settings and embedded software patches may be downloaded to be applied to the ROM-based firmware to provide flexibility for bug fixes or features additions using the new secure download mechanism. This secure download mechanism only needs to operate at the first power up sequence of the BCM20793S and assuming successful verification of the signature information; this data will be installed within the co-packaged EEPROM, ready for immediate use during all subsequent power up sequences.

See Figure 17 on page 44 for an example of the likely "one-time" secure patch download time sequence and Figure 18 on page 44 for each subsequent cold bootup.

The adoption of a secure download mechanism means that direct access to all internal register space must be disabled. During development and debug activity, this strong de-bug feature of Broadcom chips can be temporarily re-enabled by connection of an external hardware key fixture. Contact your Broadcom support representative for details.

The microprocessor, ROM and RAM, patch controller, and other ARM components, such as the interrupt controller, all reside on a single AHB bus. This system is clocked by a dedicated All-Digital Frequency-Locked Loop (AD-FLL). The AD-FLL is continuously tunable up to 24 MHz. The microprocessor/AHB system clock can therefore be programmed to the optimal frequency dictated by the processing demands.

Secure patch download timing is defined in Figure 17 and Figure 18.
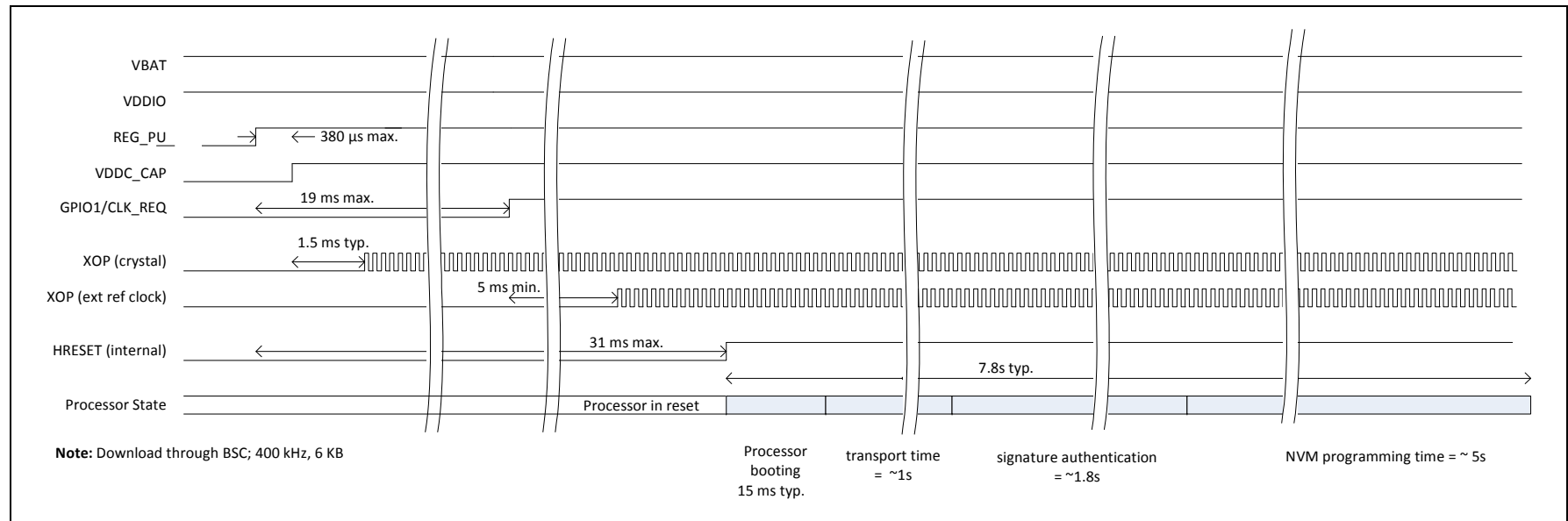
Figure 17: Estimated Time for Downloading a Secured Patch and Configuration to NVM
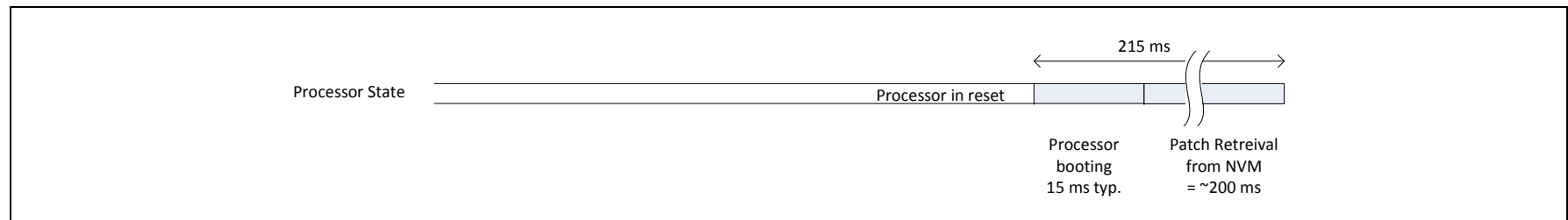
Figure 18: Estimated Time for Cold Bootup and Patch and Configuration Retrieval from NVM

Section 5: Frequency References

Reference Clock Input and XTAL Oscillator Option

The BCM20793S supports the use of either a crystal and on-chip oscillator or an external reference clock input, for accurate control of the carrier frequency generated when working in Initiator mode. The standard reference clock frequencies: 9.6, 13, 16.2, 19.2, 26, 38.4, and 52 MHz are supported from ROM boot up via auto detection mechanisms. A more flexible range of frequencies is supported from 13 MHz to 52 MHz through parameter download over the host interface.

The reference frequency for the BCM20793S can be set in one of two ways:

- Auto-detecting the reference frequency using an internal LPO. Low power oscillator
- Parameter download over host interface

For applications such as mobile handsets and portable smart communication devices, where the reference frequency is one of the standard frequencies commonly used, the BCM20793S automatically detects and programs to the correct reference frequency.

For auto-detection of 13, 26, and 52 MHz, the LPO pin should be tied high. For auto-detection of 9.6, 19.2, and 38.4 MHz, the LPO pin should be tied low. MTK and Qualcomm Platform reference clock frequency

Internal Low-Power Oscillator

The BCM20793S uses an internal low power oscillator (LPO) to generate a low-frequency clock for low-power mode timing.

The BCM20793S uses this sleep clock for time-keeping during active and snooze standby states (for example, Mode Switch timing), as well as for auto-frequency detection of the high-speed reference clock signal or XTAL oscillator blocks.

Reference Clock Input and XTAL Oscillator Specification

The BCM20793S can use either an external reference clock signal or an external crystal to provide a frequency reference. The external reference clock signal should be AC coupled. The recommended configuration for the crystal oscillator, including all external components, is shown in Figure 19. Consult the reference schematics for the latest configuration. The signal characteristics for the crystal interface are listed in Table 13.
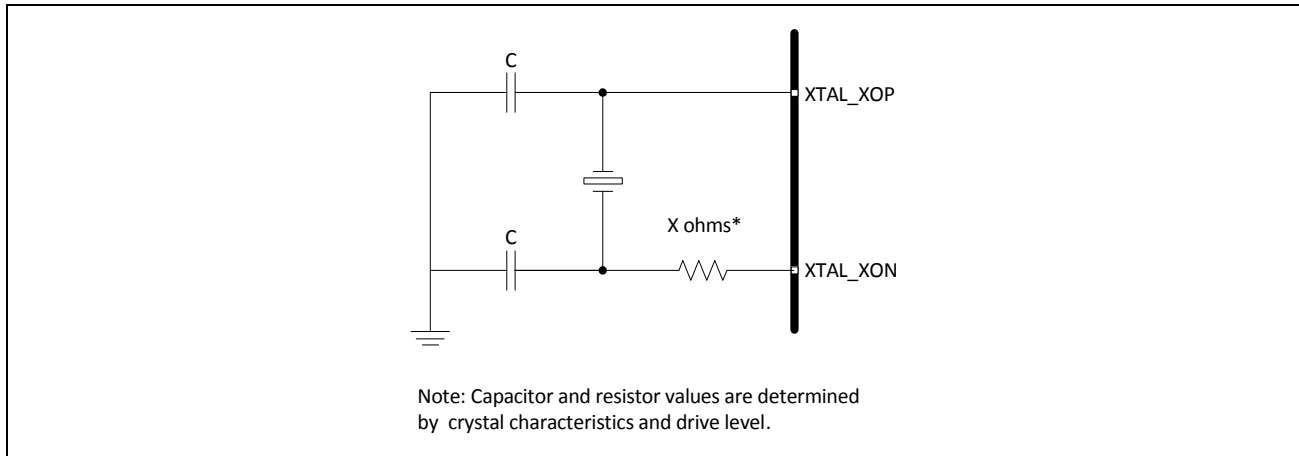
Figure 19: Recommended Oscillator Configuration

Table 13: Crystal Oscillator and External Clock – Requirements and Performance

Parameter	Conditions/Notes	Crystal			External Frequency Reference			Units
		Min	Typ	Max	Min	Typ	Max	
Frequency	–	Between 9.6 and 52						MHz
Crystal load capacitance	–	–	12	–	–	–	–	pF
ESR	–	–	–	60	–	–	–	Ω
Drive level	Configurable with default at 50% of max.	–	–	200	–	–	–	µW
XTAL_XOP Input impedance	Resistive	30	100	–	30	100	–	kΩ
	Capacitive	–	–	7.5	–	–	7.5	pF
XTAL_XOP Input low level	DC-coupled digital signal	–	–	–	0	–	0.2	V
XTAL_XOP Input high level	DC-coupled digital signal	–	–	–	1.0	–	1.26	V
XTAL_XOP Input voltage	AC-coupled digital signal (Recommended 1000 pF)	–	–	–	400	–	1200	mVp-p
Duty cycle	26 MHz clock	–	–	–	40	50	60	%

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Table 13: Crystal Oscillator and External Clock – Requirements and Performance (Cont.)

Parameter	Conditions/Notes	Crystal			External Frequency Reference			Units
		Min	Typ	Max	Min	Typ	Max	
Phase Noise	26 MHz clock at 100 kHz offset	–	–	–	–	–	–140	dBc/Hz
Integrated Phase Noise	26 MHz clock from 100 kHz to 2 MHz	–	–	–	–	–	–90	dBc/Hz
Note: Other frequencies scale from above.								

The recommended XTAL frequency is 26 MHz. A tolerance of ±10 ppm is recommended for worldwide compliance.

Card Emulation and Field Power Harvesting Clock

Card Emulation mode does not require a high-speed reference clock; the tag function block recovers its clock from the incoming carrier field.

tag   magnetic filed

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Section 6: DC Characteristics

Recommended Operating Conditions

Table 14: Recommended Operating Conditions

Element	Symbol		Minimum	Typical	Maximum	Unit
DC Supply Voltage for VBAT	VBAT		2.3	–	5.5	V
DC Supply Voltage for I/O	VDDIO		1.62	–	3.6	V
DC Supply for NFCC Power Switch	VDDSWP_IN	ETSI compliant to power class C	1.78	1.88	1.98	V
		ETSI compliant to power class B	2.9	3.1	3.3	V

Table 15: LDO Current Limits

Specification	Minimum	Typical	Maximum	Unit
Digital LDO (VDDC_CAP) Output current limit	–	100	–	mA
Analog LDO (VDDA_CAP) Output current limit	–	800	–	mA

Absolute Maximum Ratings

Table 16: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Condition
T_j	IP junction temperature	−40	125	°C	Worst case Tj Max is experienced by shunting components at Ta = +85°C under $12A/m_{rms}$ conditions
V_{BATT}	Battery supply voltage	−0.2	5.5	V	Main power supply
V_{tx_max}	Input voltage TX1, TX2 pins	−0.2	2.75	V	Any operating mode
I_{tx_max}	Input current TX1, TX2 pins[a], shunt regulator on[b]	–	650	mA_{pk}	IP Tj ≤ 110°C For ≤ 25 seconds in any 30s period; Tj ≤ 110°C
I_{tx_max}	Input current TX1, TX2 pins, shunt regulator off[b]	–	650	mA_{pk}	–
I_{swio}	Output current SWP_IO pin	−0.1	1.5	mA	DC current out of SWP_IO
I_{swp_max}	Supply current between VDDSWP_IN and VDDSWP_OUT pins	–	500	mA	Worst case when platform precharges capacitor on VDDSWP_IN and application switches power to discharged capacitor on VDDSWP_OUT.
I_{BATT_max}	Supply current between VBAT and VDDA_CAP pins	–	350	mA	Worst case when VDDA_CAP capacitor is discharged and initiator mode starts
V_{tst}	Analog test bus I/O voltage	0	1.8	V	tst1 and tst2 ports
I_{tst}	Analog test bus DC input current	−1.0	1.9	mA	
V_{ESD0}	Maximum ESD voltage 0	–	8	kV	TX1 and TX2 are 8 kV compliant using optional external components for applications where the antenna or connections may be touched by the user.
V_{ESD1}	Maximum ESD voltage 1	–	2	kV	HBM/MM standard ESD using 2.5/3.3 standard power clamps

a. I_{tx} limits in shunt regulating mode are also influenced and derived from process electromigration limits.
b. Default is for the shunt regulator to be on (even in Battery-off).

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Internal Regulators

Power Supply

The BCM20793S power management unit (PMU) architecture incorporates a high-voltage LDO that can take 2.3V–5.5V VBAT input and is designed to survive a pulse of 5.5V.

The BCM20793S PMU also includes a field-harvesting block for the field-powered mode of operation.

I/O Supply Voltages

The BCM20793S supports an I/O voltage range of 1.65 V to 3.6 V with backdrive capability. The maximum current on the VDDIO rail is expected to be no more than 2 mA.

The BCM20793S supports dual rail I/O architecture such that the host interface I/O voltage can be independent from the Secure Element interfaces.

V$_{BATT}$ Monitor

VBAT

The V$_{BATT}$ Monitor block is used as part of the power level control. In the low power mode, even though the rest of the system is powered down, the battery is used to keep the personality data stored in the battery-backed memory. V$_{BATT}$ Monitor is used by the BCM20793S to control movement from one power state to the next lower power state. This block can be pre-programmed by the host with threshold values for comparators that are is used to monitor the battery level to shut down the system and stop the current draw to prevent damage to the battery.

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Section 7: AC Characteristics

I/O Digital Level Specifications

Table 17 defines the voltage input parameters for the BCM20793S.

Table 17: Digital Input Voltage Level Specifications

Signal Name	Parameter	Minimum	Typical	Maximum	Unit
Inputs					
VDDIO = 1.8V	VIL	0	–	0.6	V
	VIH	1.1	–	1.8	V
VDDIO = 2.5V	VIL	0	–	0.7	V
	VIH	1.6	–	2.5	V
VDDIO = 3.3V	VIL	0	–	0.8	V
	VIH	2.0	–	3.3	V

Table 18 defines the voltage output parameters for the BCM20793S.

Table 18: Digital Output Voltage Level Specifications

Parameter	Minimum	Typical	Maximum	Units
VOL	0	–	0.4	V
VOH	VDDIO – 0.4	–	VDDIO	V

Table 19: Digital Output Rise and Fall Times

Parameter	Test Condition	Maximum
T_{rise}	VDDIO = 3.3V, Cload = 10 pF, from 10–90% of VDDIO	18 ns
T_{fall}	VDDIO = 3.3V, Cload = 10 pF, from 90–10% of VDDIO	20 ns

⚠️ **Caution!** The analog I/O cell for pins SWPIO_0, SWPIO_1, TX1, TX2, LPO, XTAL_XON, XTAL_XOP, and REG_PU contains an ESD protection up-diode to the relevant analog supply.

If the application circuit ramps up the voltage on these pins before the VBAT and internal analog supplies are enabled (or while holding the Vbatt or VDDA_CAP pins at 0V), there is a risk of overload that may damage BCM20793S.

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Typical Current Consumption

> **Note:** The current consumption values in Table 20 are provisional. These values will be updated after additional data is available. The values are typical for a specific version of the firmware configuration.

Table 20: Current Consumption Figures[a]

Mode	Description	Settings	Conditions	Typical Current from V_{BATT}	Unit
Shutdown	REG_PU = Low	–	–	1.2	µA
Snooze standby	Background current drain when in-between poll events: listening for incoming carrier.	–	Digital LDO on, carrier detector on, internal LPO timer running to provide periodic wake-up.	93.6	µA
Polling (peak current)[b]	During Mode Switch Polling. The peak current during the time that the chip is generating a field (for example, during the 38 ms when polling for NFC-A, B, and F).	High Supply Mode during poll (VDDA_CAP = 2.5V)	$R_L = 36\Omega$	167.3	mA
			$R_L = 16.2\Omega$	196.1	mA
			$R_L = 12.1\Omega$	215.6	mA
		Tx pin signal nominally 1.6V pk-pk	$R_L = 8\Omega$	251	mA
		Low Supply Mode during poll (VDDA_CAP = 1.88V)	$R_L = 36\Omega$	127.7	mA
			$R_L = 16.2\Omega$	143.5	mA
			$R_L = 12.1\Omega$	155.4	mA
		Tx pin signal nominally 1.1V pk-pk	$R_L = 8\Omega$	177.4	mA
Polling (averaged current during traditional A/B/F mode switch polling)[b]	During Mode Switch Polling. The time-averaged current for NFC-A, B, F polling (~38 ms duration at 3 times per second), and snooze mode in between polls, giving a 1:11 duty cycle.	High Supply Mode during poll (VDDA_CAP = 2.5V)	$R_L = 36\Omega$	11	mA
			$R_L = 16.2\Omega$	12	mA
			$R_L = 12.1\Omega$	12.8	mA
		Tx pin signal nominally 1.6V pk-pk	$R_L = 8\Omega$	13.3	mA
		Low Supply Mode during poll (VDDA_CAP=1.88V)	$R_L = 36\Omega$	9.4	mA
			$R_L = 16.2\Omega$	9.6	mA
			$R_L = 12.1\Omega$	10.0	mA
		Tx pin signal nominally 1.1 V pk-pk	$R_L = 8\Omega$	10.7	mA

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Table 20: Current Consumption Figures[a] (Cont.)

Mode	Description	Settings	Conditions	Typical Current from V_{BATT}	Unit
Low Power Target Detection (averaged current during LPTD operation)[b]	LPTD algorithm "sniffing" for approximately 50 µs, 1 time per second (depends on level of analog LDO in-rush). Snooze mode in-between sniffs.	High Supply Mode during LPTD "sniff" (VDDA_CAP = 2.5V)	R_L = 8Ω	125–144[c]	µA
Target Mode	CE and P2P Target Mode operation during a transaction.	Low Supply Mode (VDDA_CAP = 1.88V)	–	4.1	mA
CE_Level_4	Standby (register retention and carrier detector on).	–	–	7.6	µA
	CE transaction with UICC: Full battery powered.	Low Supply Mode (VDDA_CAP = 1.88V)	Excludes 5 mA typically required for SE and 1 mA SWP signaling.	5.6	mA
CE_Level_3	Standby (register retention and carrier detector on).	–	–	7.6	µA
	CE transaction with UICC: Using residual battery power.	Low Supply Mode (VDDA_CAP = 1.88V)	Excludes 5 mA typically required for SE and 1 mA SWP signaling.	5.6	mA
CE_Level_2	Standby (only register retention).	–	–	7.2	µA
	CE transaction with UICC: All except registers powered by field.	–	–	30.2	µA
CE_Level_1	Standby and CE transaction with UICC: everything powered by field.	–	–	–	µA

a. The values in this table were measured on QFN using Patch 20.
b. During initiator mode, when the device is generating the carrier field, the VBAT supply current will be heavily dependent on the antenna drive output current. The antenna drive Tx pin current is a function of the internal supply mode, the internal amplifier gain settings for the output signal swing, and the effective impedance of the antenna network. The High/Low Supply Mode and associated output signal swing is given in the "Settings" column and the antenna load is represented by an AC coupled resistive load RL, given in the "Conditions" column.
c. Depending on setup.

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Section 8: Pin Information

Pin List

Table 21: Pin List

Pin Number	Pin Name	Comment
1	VDDSWP_IN	Platform UICC supply in
2	VDDSWP_OUT0	UICC supply out
3	SWPIO_0	SWP I/O 0
4	SWPIO_1	SWP I/O 1
5	VDDSWP_OUT1	Supply to embedded secure element
6	VDD_ADC	Decoupling, need linking to VDDC_CAP via the target PCB
7	NFC_WAKE	Signal from host to the BCM20793S
8	TM2	ATE test mode (grounded for normal operation)
9	VDD_EEPROM_IN	1.8V power input to the co-packaged EEPROM
10	HOST_WAKE	Interrupt signal from the BCM20793S to host
11	CLK_REQ	Clock request
12	UART_TXD	UART transmit
13	VDDIO	I/O supply; externally regulated
14	UART_RTS_N	UART ready to send
15	SPI_INT	Host interface selection and SPI interrupt to host in SPI mode only
16	UART_CTS_N	UART clear to send
17	UART_RXD	UART receive
18	N/C	No connect
19	XTAL_XON	Crystal N
20	XTAL_XOP	Crystal P/clock reference input
21	VDD_XTAL	Decoupling, need linking to VDDC_CAP via the target PCB
22	LPO	Frequency selection, strap high or low (refer to "Reference Clock Input and XTAL Oscillator Option" on page 45)
23	VDD_VCO	Decoupling, need linking to VDDC_CAP via the target PCB
24	VDDC_CAP	Decoupling, links VDDADC, VDD_XTAL, and VDD_VCO via the target PCB
25	REG_PU	Regulator power control from host
26	VBAT	Battery supply
27	VDDA_CAP	Analog LDO supply decoupling (1.88V/2.5V)
28	TX2	Coil output 2
29	TX1	Coil output 1
30	VDD_ANT	Rectifier output, external cap
31	N/C	Do not connect

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Table 21: Pin List (Cont.)

Pin Number	Pin Name	Comment
32	VDD_EE	Output 1.8V supply voltage to be linked to VDD_SE_IN to power co-packaged EEPROM.
33	SDA	BSC data internally connected to co-packaged EEPROM. Pull-up resistor required to VDD_EE.
34	SCL	BSC clock internally connected to co-packaged EEPROM. Pull-up resistor required to VDD_EE.

Note: The QFN paddle is used to connect all the VSS/ground pads together, and should be connected to the PCB ground plane.

QFN-34L Pin Diagram
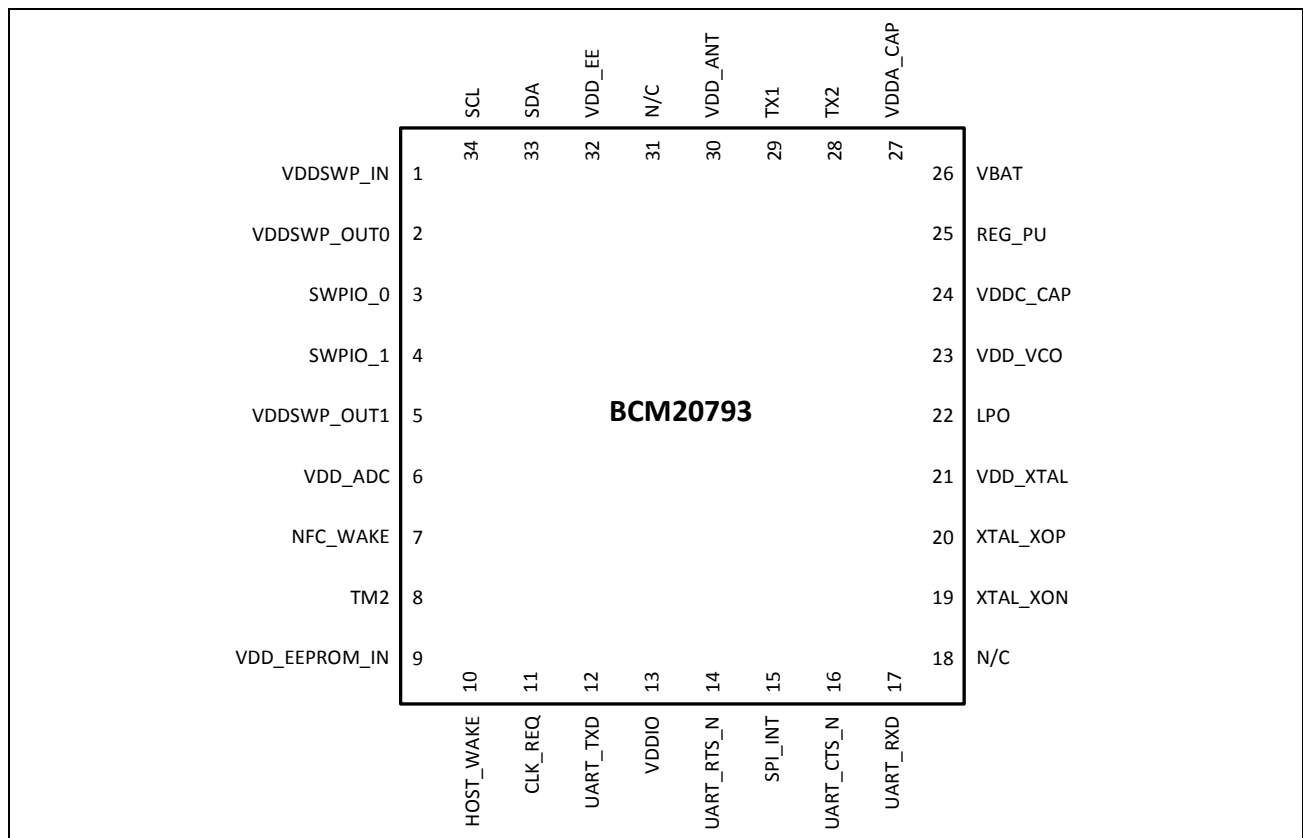
Figure 20: Pin Diagram

In normal operation, pins 9 and 32 must be connected together via target PCB with a decoupling capacitor to provide a switched power supply to the internal EEPROM device.

Section 9: Antenna Interface

The BCM20793S supports a 2-pin antenna interface, which requires minimal external components, none of which are active. Figure 21 and Figure 22 show two recommended interface circuit topologies.
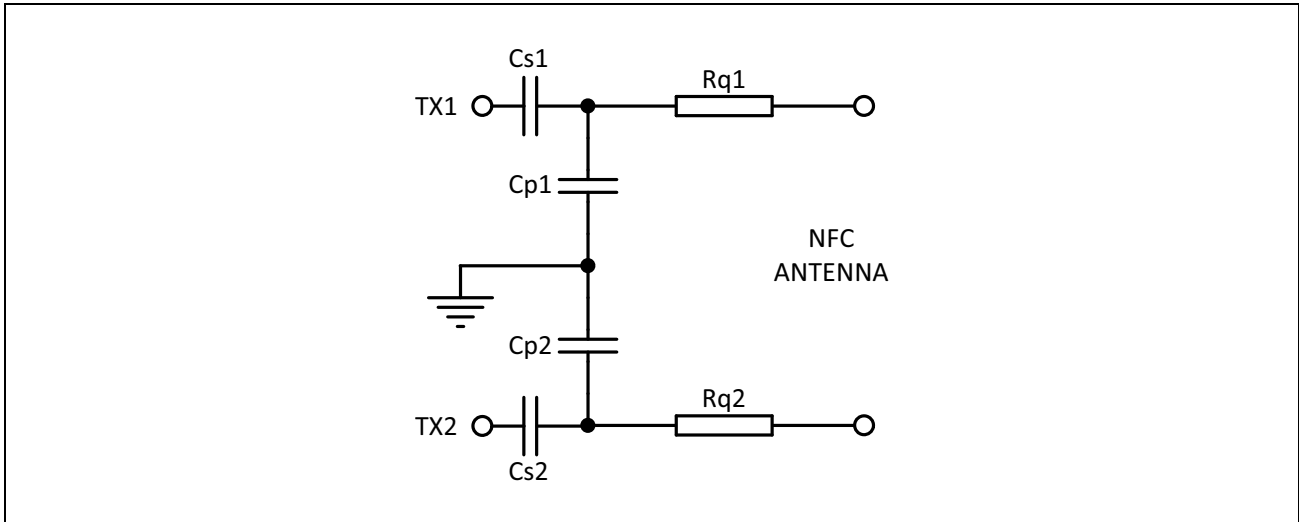

Figure 21: Recommended Antenna Interface Circuit 1
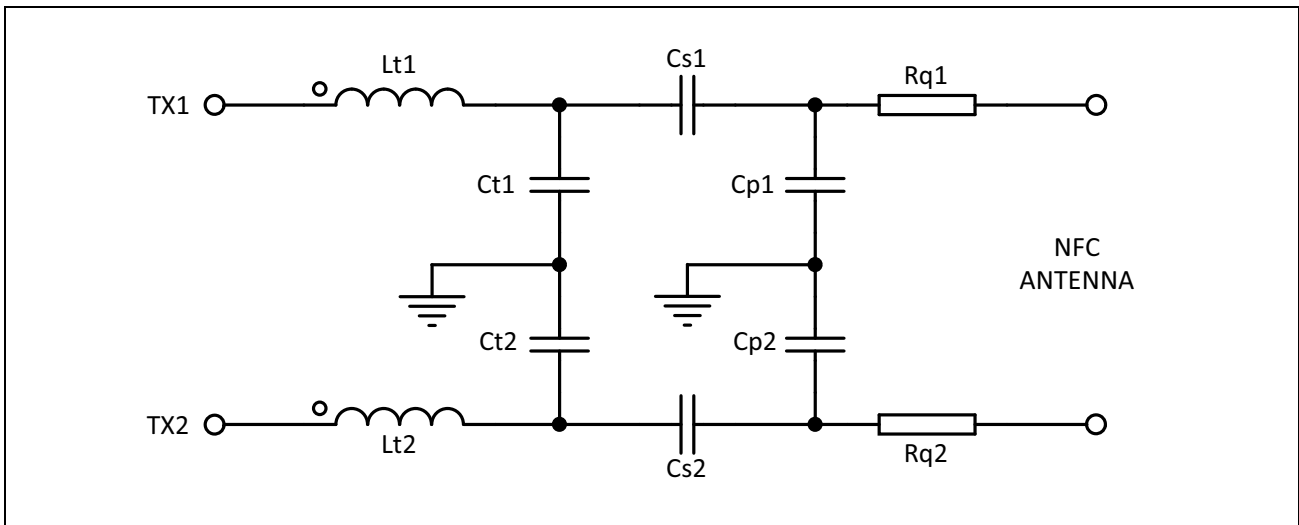

Figure 22: Recommended Antenna Interface Circuit 2

Note: Work with your local Broadcom representative when selecting an antenna design to gain Applications support and for guidance on component values.

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Section 10: Mechanical Specifications

Package Thermal Characteristics

Table 22: Package Thermal Characteristics Per JEDEC Standards

Device power dissipation, P(W)	0.969
Ambient air temperature, T_A (°C)	70
θ_{JA} in still air (°C/W)	46.49
θ_{JB} in still air (°C/W)	14.24
θ_{JC} in still air (°C/W)	87.69

2s2p board, package only						
Air Velocity		T_{J_max} (°C)	T_T (°C)	θ_{JA} (°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB} (°C/W)
m/s	**ft/min**					
0	0	115.0	102.8	46.49	12.61	21.62
0.508	100	110.6	98.5	41.94	12.52	21.32
1.016	200	109.6	97.2	40.83	12.71	21.23
2.032	400	108.4	95.8	39.62	13.00	21.13
3.048	600	107.7	94.8	38.88	13.24	21.06

Environmental Ratings

Table 23: Environmental Characteristics

Characteristic	*Minimum*	*Nominal*	*Maximum*	*Units*	*Conditions/Comments*
Ambient Temperature (T_A)	−40	25	+85	°C	Operation
Storage Temperature	TBD	TBD	TBD	°C	–
Relative Humidity	TBD	TBD	TBD	%	Storage
	TBD	TBD	TBD	%	Operation

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QFN-34L Package Dimensions

Figure 23: QFN-34L Package Dimensions

DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	–	–	0.05
D	3.90	4.00	4.10
D1	2.65	2.80	2.95
E	4.40	4.50	4.60
E1	3.15	3.30	3.45
b	0.15	0.20	0.25
e	0.40 BSC		
L	0.25	0.30	0.35
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.08
ddd	–	–	0.07
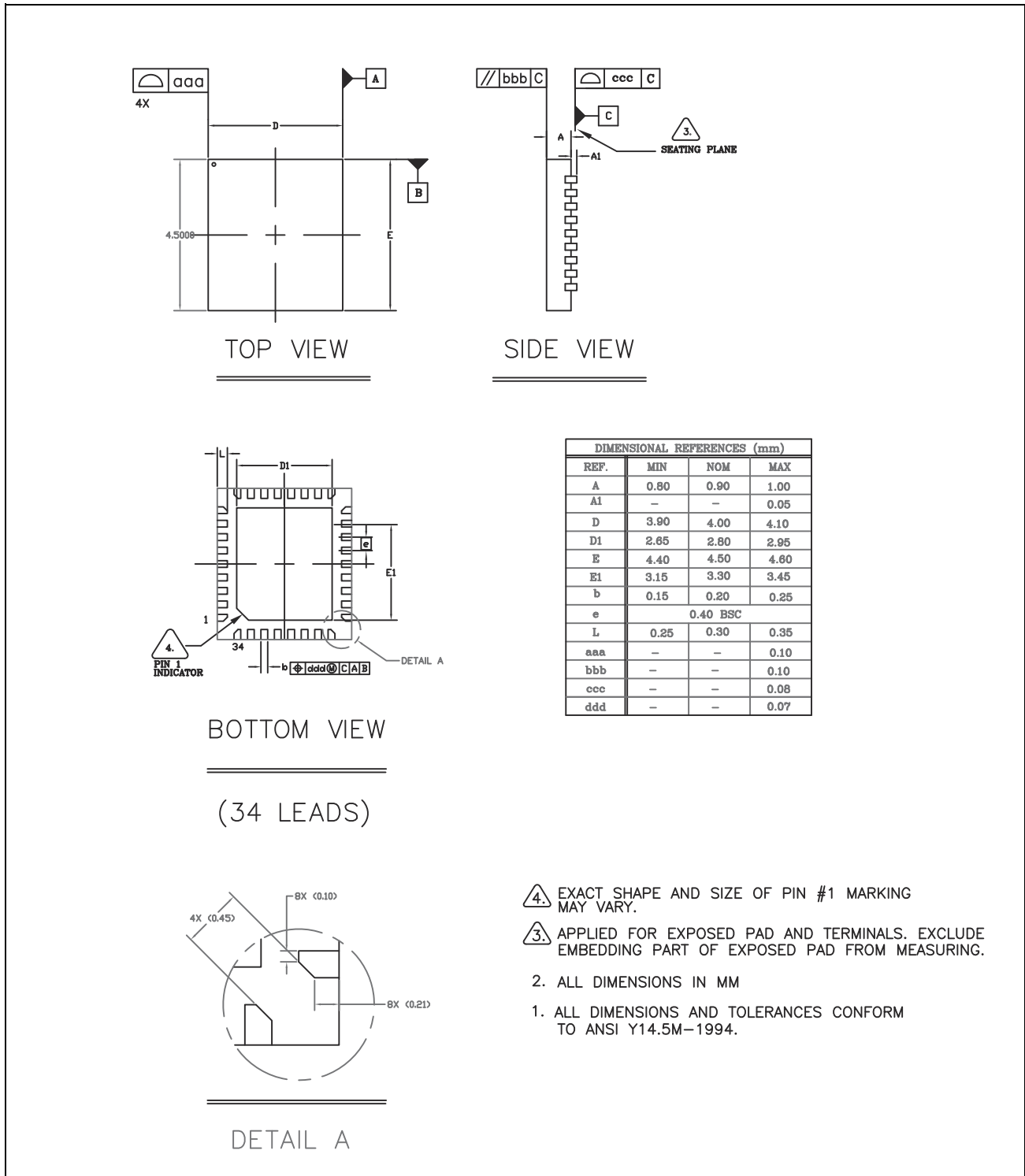
4. EXACT SHAPE AND SIZE OF PIN #1 MARKING MAY VARY.

3. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.

2. ALL DIMENSIONS IN MM

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ANSI Y14.5M—1994.

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Section 11: Ordering Information

Table 24: Ordering Information

Part Number	Package
BCM20793SKMLG	QFN-34L 4.0 mm × 4.5 mm × 0.9 mm (nominal) with 0.4 mm ball pitch

Appendix A: Acronyms

Acronym	Definition
AD-FLL	All-Digital Frequency-Locked Loop
BLE	Bluetooth Low Energy
CE	Card Emulation
eSE	Embedded Secure Element
FeliCa	Felicity Card
IEC	International Electrotechnical Commission
ISO	International Organization for Standardization
JIS	Japanese Industrial Standard
LC	link control
LLCP	Link Layer Control Protocol
LPO	low power oscillator
LPTD	Low Power Target Detection
MCU	Microcontroller
NCI	NFC Controller Interface
NFC	Near Field Communication
NFC-WI	NFC-Wired Interface
PCD	Proximity Coupling Device
PICC	Proximity Integrated Circuit Card
PMU	Power Management Unit
QFN	Quad Flat No leads
RFID	Radio Frequency Identification
RX	receive
SE	Secure Element
SPI	Serial Peripheral Interconnect
SWP	Single Wire Protocol
TX	transmit
UART	universal asynchronous receiver/transmitter
UICC	Universal Integrated Circuit Cards
XTAL	Crystal

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