DS3131-1.0

2 MBIT PCM SIGNALLING CIRCUIT

MJ1446

TIME SLOT 16 RECEIVER AND TRANSMITTER

The 2.048 Mbit PCM signalling circuits comprise a group of circuits which will perform the common signalling and error detection functions for a 2.048 Mbit 30 channel PCM transmission link operating to the appropriate CCITT recommendations. The circuits are fabricated in N-channel metal gate MOS and operate from a single 5volt supply. Relevant inputs and outputs are TTL compatible.

The MJ1446 has two modes of operation dependent on the state of the mode control input. With the mode control high the device is in the transmit mode and with the mode control low the device is in the receive mode.

In the transmit mode the device accepts 64kbits/sec signalling information in either binary or AMI format and outputs it at 2Mbits/sec on to the digital highway during time slot 16.

In the receive mode the device accepts 2Mbit/sec information from the digital highway, during time slot 16 and output is at 64kbits/sec in both binary and AMI format.

In both receive and transmit mode there is an AMI coded clock output, AMI output and $\overline{\text{AMI}}$ output which conforms to CCITT recommendation no G372 for a 64kbits/sec contradirectional interface. The alarm inhibit input causes the 8kHz timing signal to be removed from the AMI clock output.

The device is reset in both modes by a time slot 16 channel pulse and the alarm output provides an indication that the internal counter is operating correctly.

Also provided are 64kHz, 16kHz and 8kHz clock outputs.

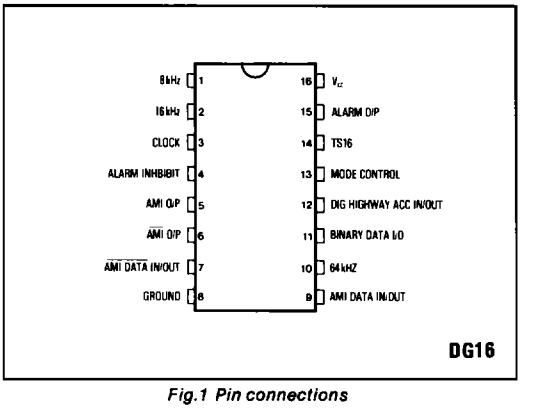

Fig.1 Pin connections

FEATURES

- 5V ±5% Supply—20mA Typical
- Conforms to CCITT Recommendations
- Provides Both AMI and Binary Format Data Outputs
- Single Chip Receive or Transmit
- All Inputs and Outputs are TTL Compatible.

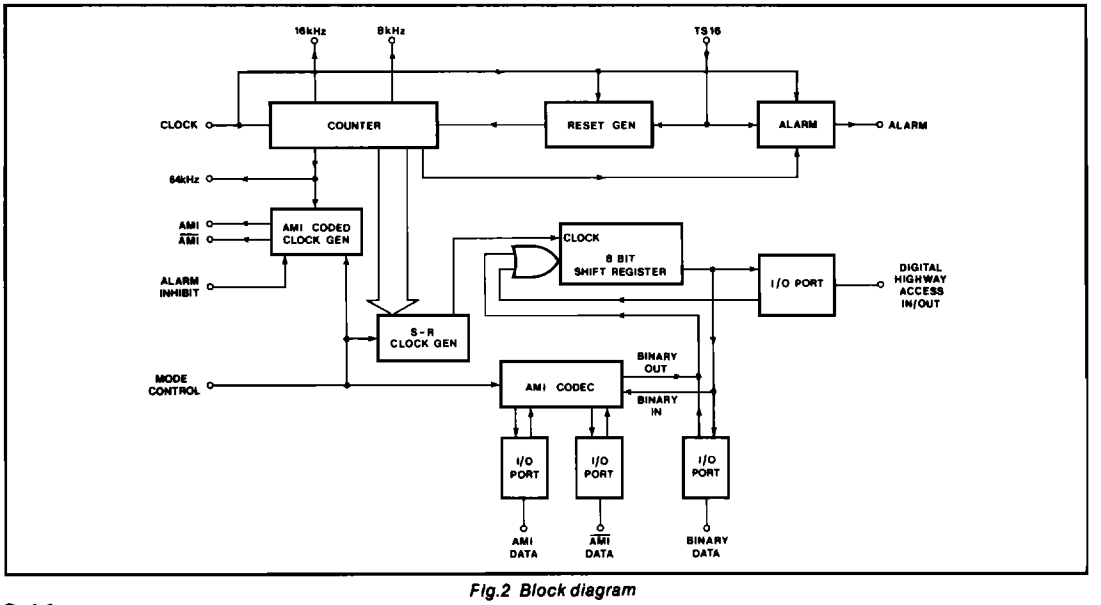

Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):

Supply voltage V_{CC} = 5V ± 0.25V, Ambient temperature T_{amb} = -10°C to +70°C,

Static Characteristics

Characteristic	Symbol	Pins	Value			Units	Conditions
			Min.	Typ.	Max.		
Low level input voltage	V_{IL}	3, 4, 7, 9, 11, 12, 13, 14	-0.3		0.8	V	
Low level input current High level input current	I_{IN}	11		1	50	µA	
High level input voltage	V_{IH}	11	2.4		V_{CC}	V	
Low level output	V_{OL}	1, 2, 5, 6, 7, 9, 10, 11, 15			0.5	V	I_{sink} = 2mA
		12			0.5	V	I_{sink} = 5mA
High level output voltage	V_{OH}	1, 2, 10, 5, 6, 15	2.8			V	I_{source} = 200µA
High level output leakage current	I_{CH}	7, 9, 11, 12			20	µA	$V_{OUT} = V_{CC}$
Supply current	I_{CC}			20		mA	V_{CC} = 5.25V

Dynamic Characteristics (f_{clock} = 2.048 MHz)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Propogation delay clock to data out to digital highway	t_p	20		200	ns	Fig.7
Propogation delay clock to 64kHz out	t_p	20		200	ns	Fig.7
Input delay, clock to digital highway access	$t_{d\,DATA}$	20		200	ns	
Input delay, clock to time slot 16	$t_{d\,TS16}$	80		200	ns	
Output delay 64kHz to 16kHz output	$t_{p\,16}$			70	ns	Fig.7
Output delay, 64kHz to 8kHz output	$t_{p\,8}$			170	ns	Fig.7
Output delay, 64kHz to binary data output (64kHz)	$t_{p\,BIN}$	20		450	ns	Fig.8
Output delay 64kHz to AMI, $\overline{AMI}$, AMI data & $\overline{AMI}$ data o/p's	$t_{p\,AMI}$	20		400	ns	Fig.8
Input delay, 64kHz to binary data in (64kHz)	$t_{d\,BIN}$			100	ns	

FUNCTIONAL DESCRIPTION

Functions listed by pin number

1. 8kHz
8kHz square wave output.

2. 16kHz
16kHz square wave output.

3. Clock
System clock input (2.048MHz for a 2Mbit PCM system)

4. Alarm Inhibit
A high level on this input inhibits the 8kHz timing signal on the AMI clock outputs.

5. AMI output
Alternative Mark Inversion coded 64kHz.

6. $\overline{AMI}$ output

7. $\overline{AMI}$ Data In/out
In the transmit mode 64kHz signalling data in AMI format is accepted at these inputs for output to PCM highway during time slot 16.

8. GND
Zero volts.

9. AMI Data In/out
In the receive mode data accepted from the PCM highway during time slot 16 appears on these outputs at 64kbits/sec in AMI format.

10. 64kHz
64kHz square wave output.

11. Binary data In/out
In the transmit mode 64k bit/sec signalling data in binary form is accepted at this input for output to the PCM data highway during time slot 16. In the receive mode data is accepted from the PCM highway during TS16 and appears at this output at 64k bits/sec in binary format.

12. Digital Highway access In/out
In the receive mode 2Mbit/sec signalling data is accepted at this input during time slot 16 from the PCM digital highway. In the transmit mode signalling data is output to the PCM digital highway during time slot 16 at 2Mbits/sec.

13. Mode control
A high level on this input causes the MJ1446 to operate in the transmit mode while a low level causes it to operate in the receive mode.

14. TS16
This input should be connected to time slot 16 channel pulse of the PCM system to synchronise the MJ1446 with the rest of the system.

15. Alarm output
A high level on this output indicates that the internal counter has stopped or is out of synchronisation with the time slot 16 channel pulse.

16 V_{CC}
Positive supply 5V ±5%.

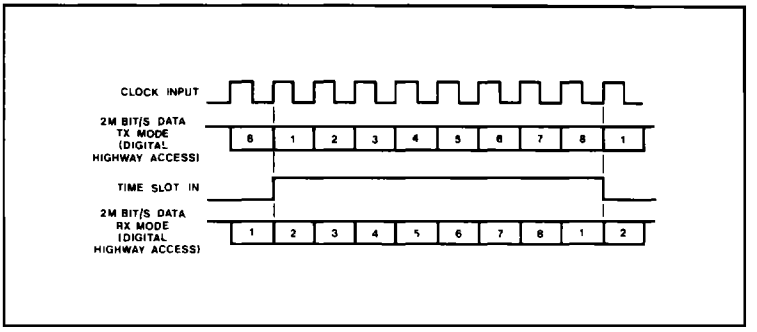

Fig.3 2MBit/s operation

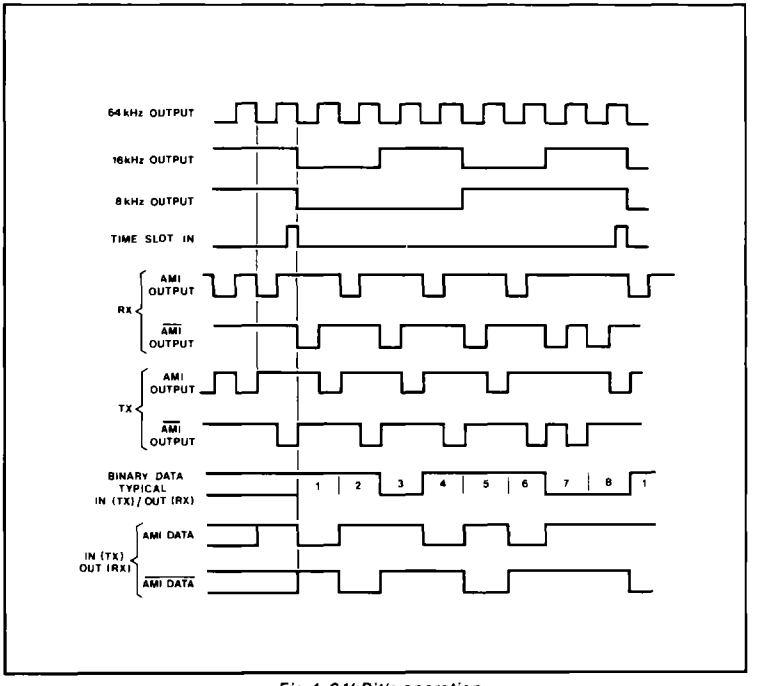

Fig.4 64kBit/s operation

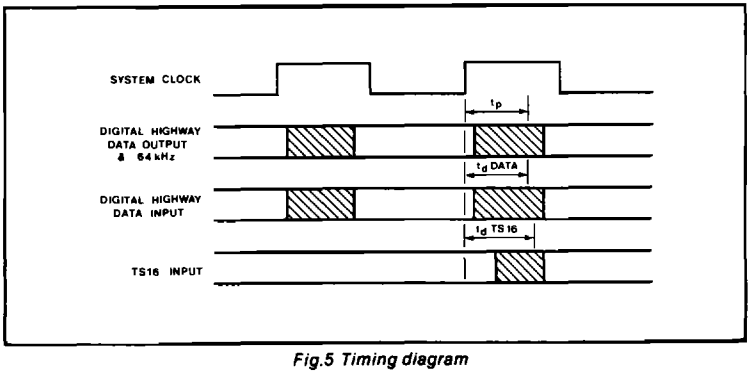

Fig.5 Timing diagram

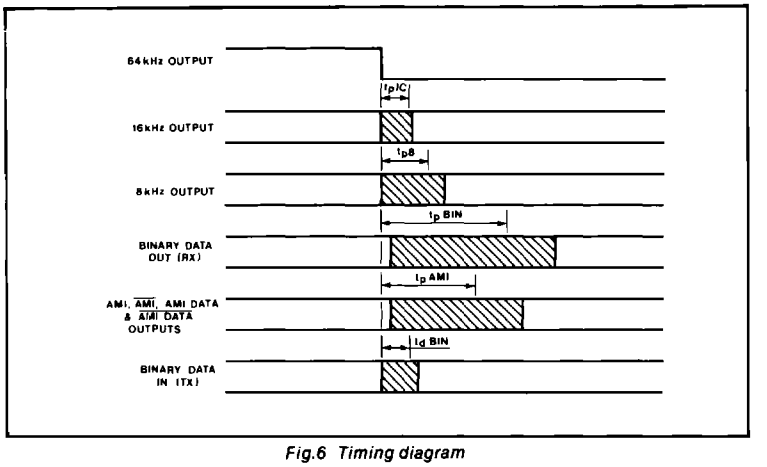

Fig.6 Timing diagram

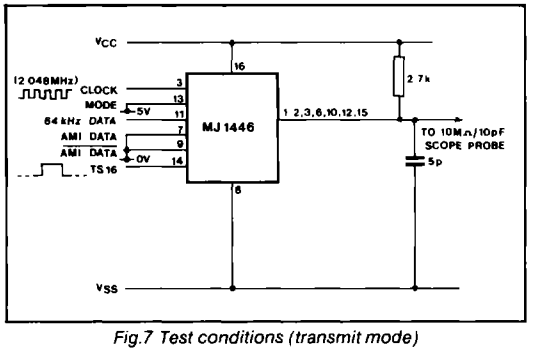

Fig.7 Test conditions (transmit mode)

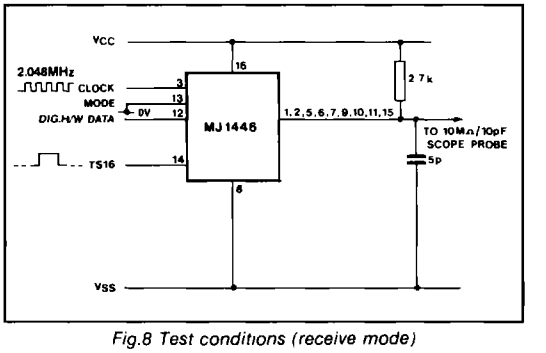

Fig.8 Test conditions (receive mode)