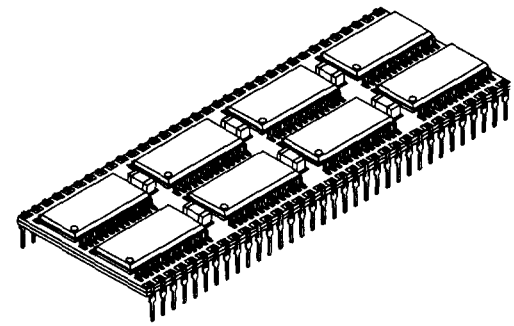
DPS96122

256K X 16 / 512K X 8 CMOS SRAM MODULE



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DESCRIPTION:

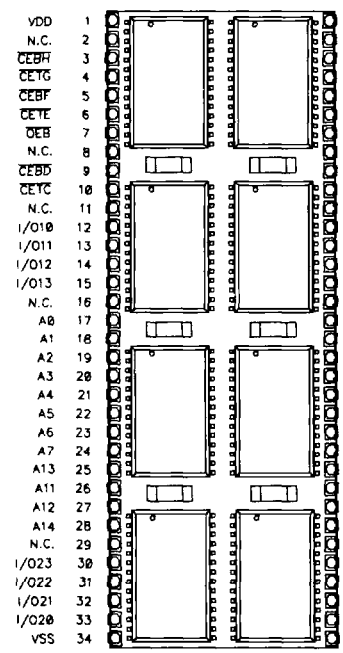
The DPS96122 is a four megabit Static Random Access Memory (SRAM), complete with decoupling capacitors. It can be organized as 256K X 16 or as 512K X 8.

The DPS96122 is ideally suited for large memory applications where low power and ease of use is required.

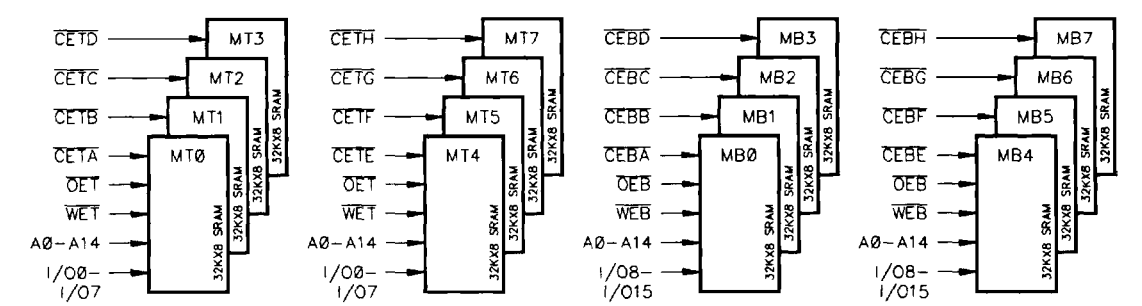
FEATURES:

- Fast Access Times: 85, 100, 120, 150ns (max.)
- Faster Speed Available Upon Request
- Fully Static Operation; No Clock or Refresh Required
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Common Data Input and Output
- Low Data Retention Voltage: 2.0V min.
- Standard 68-Pin DIP Package

PIN-OUT DIAGRAMS



FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A19	Address Inputs
I/O0 - I/O15	Data In/Out
$\overline{CETA}$ - $\overline{CETH}$	Chip Enables Top
$\overline{CEBA}$ - $\overline{CEBH}$	Chip Enables Bottom
$\overline{WET}$	Write Enable Top
$\overline{WEB}$	Write Enable Bottom
$\overline{OET}$	Output Enable Top
$\overline{OEB}$	Output Enable Bottom
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

RECOMMENDED OPERATING RANGE [1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD} +0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -1.0mA	2.4	-	V
V_{OL}	LOW Voltage	I_{OL} = 2.1mA	-	0.4	V

ABSOLUTE MAXIMUM RATINGS [3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-50 to + 100	°C
T_{BIAS}	Temperature Under Bias	-40 to + 85	°C
V_{DD}	Supply Voltage [1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD} + 0.5	V

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	160	pF	V_{IN} = 0V
C_{CE}	Chip Enable	160		
C_{WE}	Write Enable	80		
C_{OE}	Output Enable	160		
$C_{I/O}$	Data Input/Output	80		

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	HIGH-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

DC OPERATING CHARACTERISTICS: Over operating ranges							
Symbol	Characteristics	Test Conditions	C		I		Unit
			Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-20	+20	-20	+20	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-20	+20	-20	+20	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA		75 (120)		75 (120)	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA		100 (170)		100 (170)	mA
I_{SB1}	Full Standby Supply Current	See Note 5		1.6		3.2	mA
I_{SB2}	Standby Supply	$\overline{CE}$ = V_{IH}		32		32	mA
I_{CCDR2}	Data Retention Supply Current	V_{DR} = 2V		0.50		0.65	mA
I_{CCDR3}	Data Retention Supply Current	V_{DR} = 3V		0.65		0.80	mA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA		2.4		2.4	V

NOTE: Characteristics listed in parentheses are listed for the 256K x 16 organization when they differ from the 512K x 8 organization.

DATA RETENTION CHARACTERISTICS						
Symbol	**Parameter**	**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{DR}	Data Retention Voltage	$\overline{CE} \geq V_{DD}$ -0.2V	2.0	5.0	5.5	V
t_{CDR}	Chip Disable to Data Retention Time		0			ns
t_R	Recovery Time	t_{RC} = Read Cycle Timing	t_{RC}			ns

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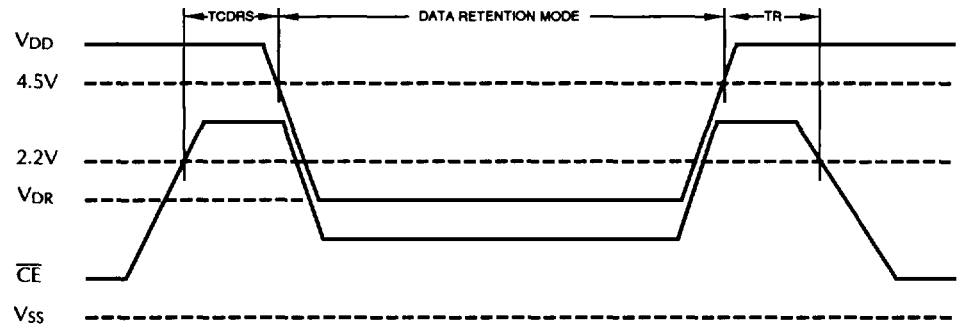
DATA RETENTION WAVEFORM

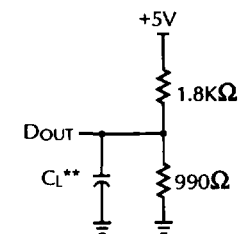


AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input Timing Reference Levels	1.5V

* *Transition measured from 0.8V and 2.2V.*

AC TEST CONDITIONS		
Load	C_L	***Parameters Measured***
1	100pF	except t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{WLZ}, t_{OLZ} and t_{OHZ}
2	5pF	t_{CLZ}, t_{CHZ}, t_{WHZ}, t_{WLZ}, t_{OLZ} and t_{OHZ}

Figure 1. Output Load
** Including Probe and Jig Capacitance.

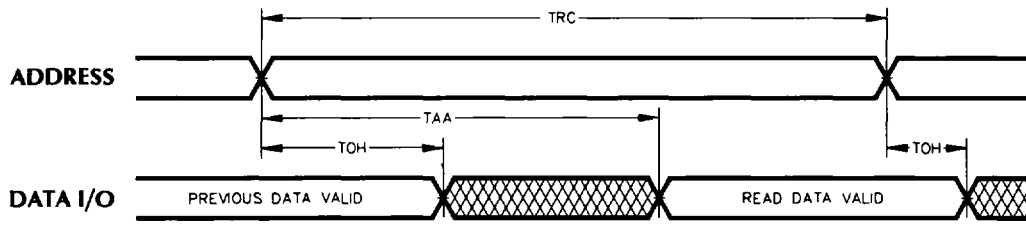


AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges										
No.	**Symbol**	**Parameter**	**-85**		**-100**		**-120**		**-150**		**Unit**
			Min.	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	
1	t_{RC}	Read Cycle Time	85		100		120		150		ns
2	t_{AA}	Address Access Time		85		100		120		150	ns
3	t_{CO}	Chip Enable to Output Valid		85		100		120		150	ns
4	t_{OV}	Output Enable to Output Valid		60		60		60		70	ns
5	t_{OH}	Output Hold from Address Change	3		10		10		10		ns
6	t_{CLZ}	Chip Enable to Output in LOW-Z [6, 7]	10		10		10		10		ns
7	t_{OLZ}	Output Enable to Output in LOW-Z [6, 7]	3		5		5		5		ns
8	t_{CHZ}	Chip Enable to Output in HIGH-Z [6, 7]		35		40		45		55	ns
9	t_{OHZ}	Output Enable to Output in HIGH-Z [6, 7]		30		35		40		50	ns
10	t_{OC}	Output Hold from Chip Enable	0		0		0		0		ns

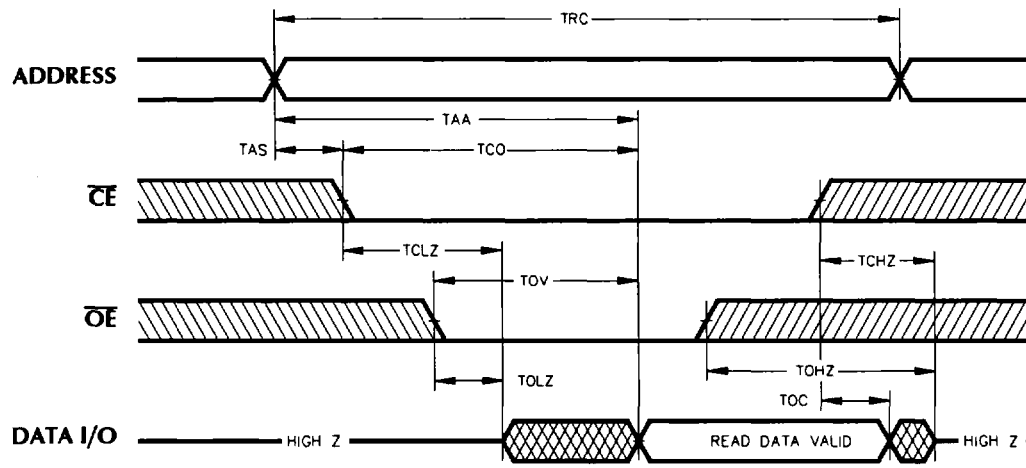
AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [8]											
No.	Symbol	Parameter	-85		-100		-120		-150		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
11	t_{WC}	Write Cycle Time	85		100		120		150		ns
12	t_{AW}	Address Valid to End of Write	75		90		100		120		ns
13	t_{CW}	Chip Enable to End of Write	75		90		100		120		ns
14	t_{DW}	Data Valid to End of Write	35		40		50		60		ns
15	t_{DH}	Data Hold Time	0		0		0		0		ns
16	t_{WP}	Write Pulse Width	65		75		90		110		ns
17	t_{AS}	Address Set-up Time ***	0		0		0		0		ns
18	t_{AH}	Address Hold Time	5		5		5		5		ns
19	t_{WHZ}	Write Enable to Output in HIGH-Z [6, 7]		35		40		45		55	ns
20	t_{WLZ}	Write Enable to Output in LOW-Z [6, 7]	5		5		5		5		ns

*** Valid for both Read and Write Cycles.

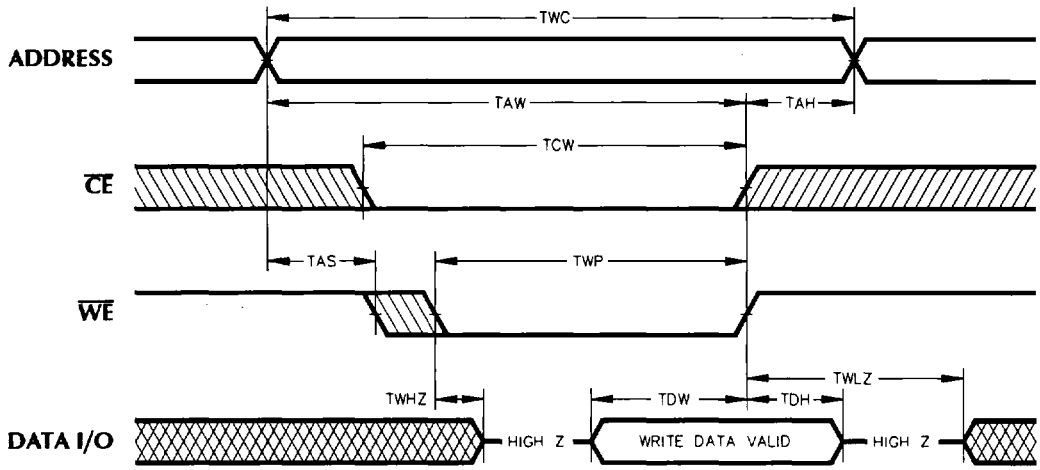
READ CYCLE 1: Address Controlled. $\overline{WE}$ is HIGH. $\overline{CE}$ and $\overline{OE}$ are LOW.



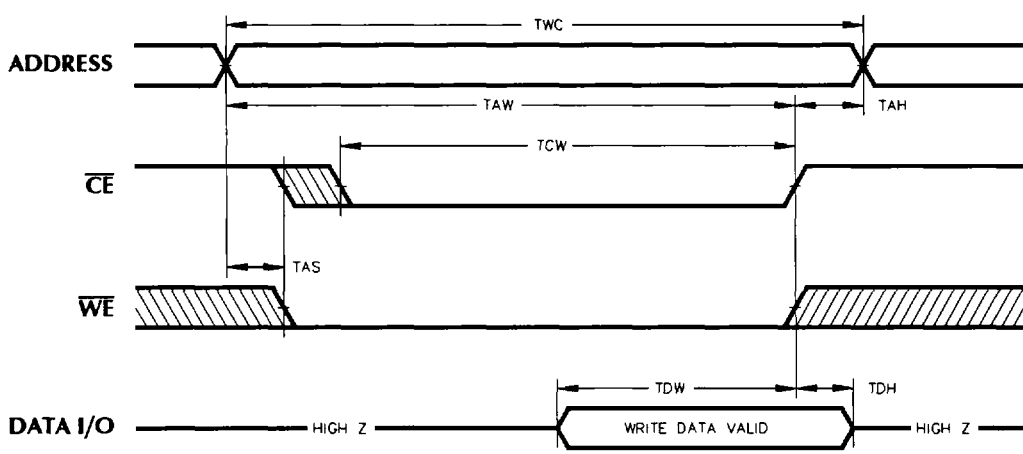
READ CYCLE 2: $\overline{CE}$ Controlled. $\overline{WE}$ is HIGH.



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW.



WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is HIGH.



WAVEFORM KEY

Data Valid	Transition from HIGH to LOW	Transition from LOW to HIGH	Data Undefined or Don't Care

ORDERING INFORMATION

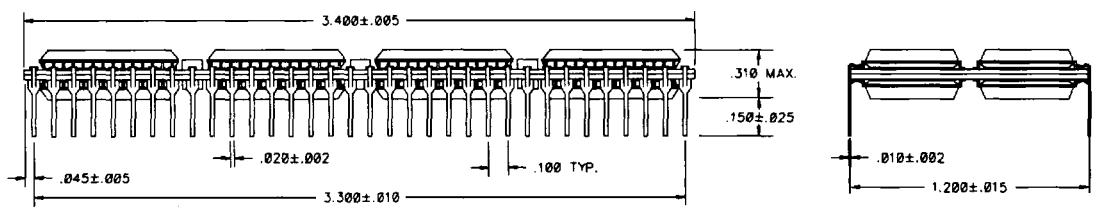
DP S96122 – XXX X

PREFIX			
DEVICE TYPE			256Kx16 OR 512Kx8 CMOS SRAM MODULE
SPEED	85	85ns	
	100	100ns	
	120	120ns	
	150	150ns	
GRADE	C	COMMERCIAL	0°C to +70°C
	I	INDUSTRIAL	–40°C to +85°C

NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min.= -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ± 500mV from steady state voltage.
6. This parameter is measured with specified loading in Figure 1.
7. When $\overline{OE}$ and $\overline{CE}$ are LOW and. $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
8. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

MECHANICAL DRAWING



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