AZ100EP16FE

PECL/ECL High Speed VCSEL Driver with Variable Output Swing or Limiting Amplifier

www.azmicrotek.com

DESCRIPTION

The AZ100EP16FE is a Silicon–Germanium (SiGe) differential VCSEL driver with variable output swing or limiting post amplifier. The AZ100EP16FE is optimized for OC-12, OC-24, OC-48, Ethernet, Sonnet, Fiber Channel or related applications at data rates up to 2.5Gbps. An input controls the amplitude of the Q/$\overline{Q}$ outputs, which allows compensation for differing VCSEL characteristics.

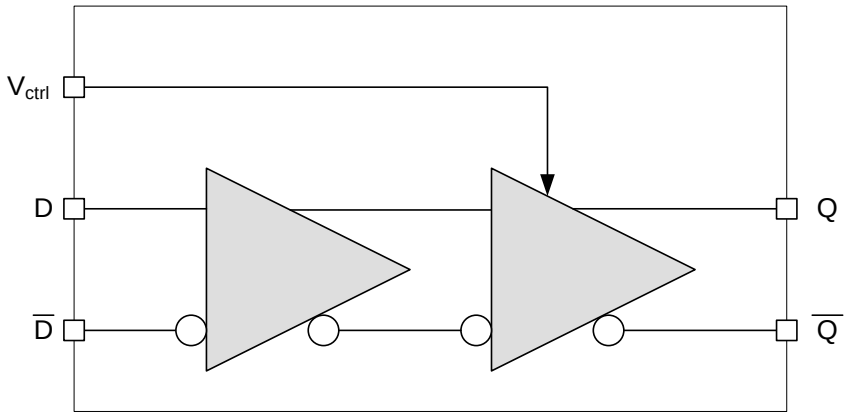
FEATURES

- Silicon-Germanium for high-speed operation
- <100ps typical rise/fall times
- Optimized for 0.622 to 2.5Gbps fiber applications

APPLICATIONS

- OC-12, OC-24, OC-48 Applications
- Ethernet, Sonnet Fiber Channel Applications

BLOCK DIAGRAM



PACKAGE AVAILABILITY

- MSOP8
  - Green/RoHS Compliant/Pb-Free

Order Number	Package	Marking
AZ100EP16FETG[1]	MSOP8	AZHPG16FE[2]

[1] Tape & Reel - Add 'R1' at end of order number for 7in (1k parts), 'R2' (2.5k) for 13in

[2] See www.azmicrotek.com for date code format

PIN DESCRIPTION AND CONFIGURATION

Table 1 - Pin Description

Pin	Name	Type	Function
1	V_{CTRL}	Input	Output Swing Control
2	D	Input	Data Input
3	$\overline{D}$	Input	Data Input
4	V_{REF}	Output	Reference Voltage Output
5	V_{EE}	Power	Negative Supply
6	$\overline{Q}$	Output	Data Output
7	Q	Output	Data Output
8	V_{CC}	Power	Positive Supply

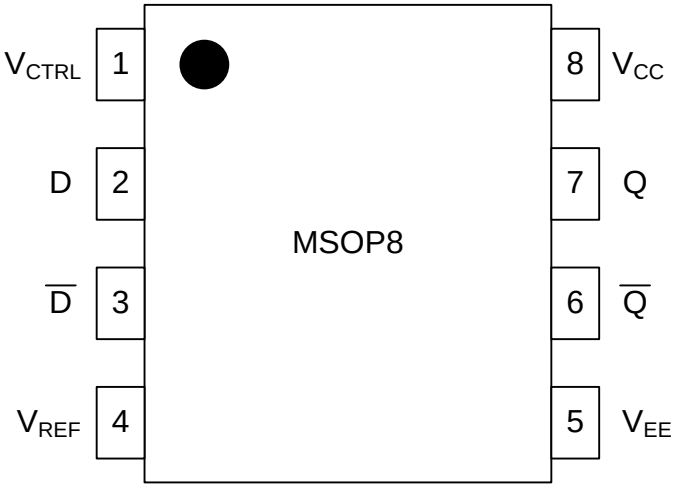


Figure 1 - Pin Configuration for MSOP8

ENGINEERING NOTES

The operational range of the AZ100EP16FE control input, V_{CTRL}, is from V_{REF} (full swing) to V_{CC} (small swing). For post amplifier applications, maximum swing is achieved by leaving the V_{CTRL} pin open or by tying it to the negative supply pin (V_{EE}). Simple control of the output swing can be obtained by a variable resistor between the V_{REF} and V_{CC} pins, with the wiper driving V_{CTRL}. A typical application circuit is shown in Figure 2.

The AZ100EP16FE also provides a V_{REF} output which functions as a DC bias for input AC coupling to the device. The V_{REF} pin should be used only as a bias for the AZ100EP16FE as its current sink/source capability is limited. When used, the V_{REF} pin should be bypassed to ground via a 0.01µF capacitor.

The maximum DC output current should be kept below 16mA. Connecting each output (Q/$\overline{Q}$) to V_{EE} with a 180Ω resistor is typically used. The load is then AC coupled from the output. DC and AC symmetrical loading of the Q/$\overline{Q}$ outputs will provide the best output wave shape.

Under open input conditions for D/$\overline{D}$, the Q/$\overline{Q}$ outputs are not guaranteed.

NOTE: Specifications in ECL/PECL tables are valid when thermal equilibrium is established.

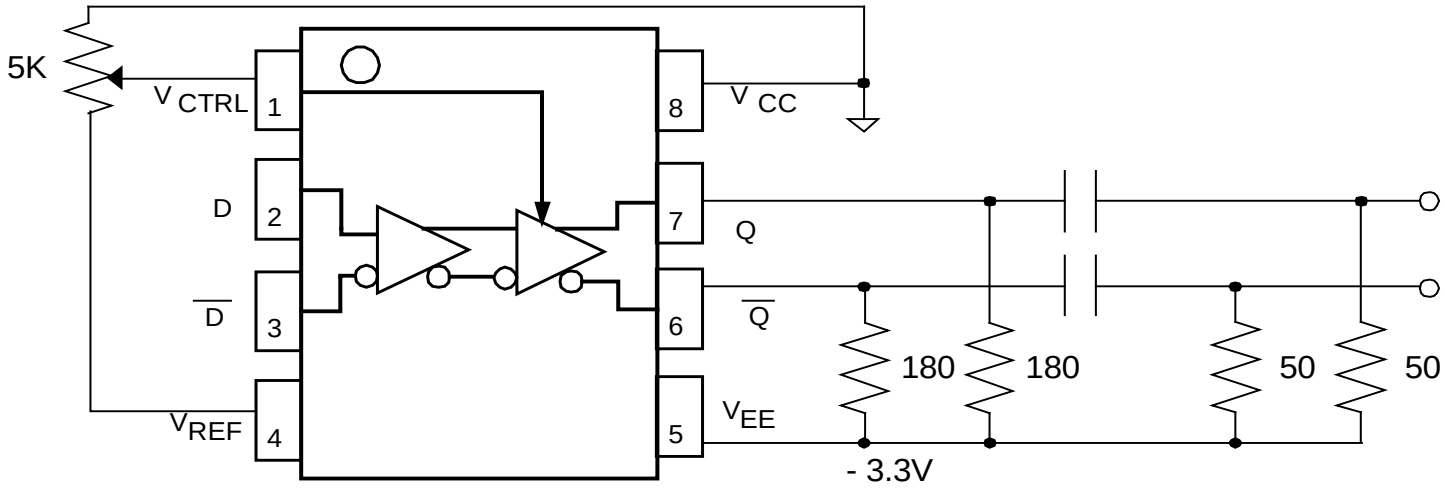


Figure 2 - AZ10/100EP16 Large Signal Performance

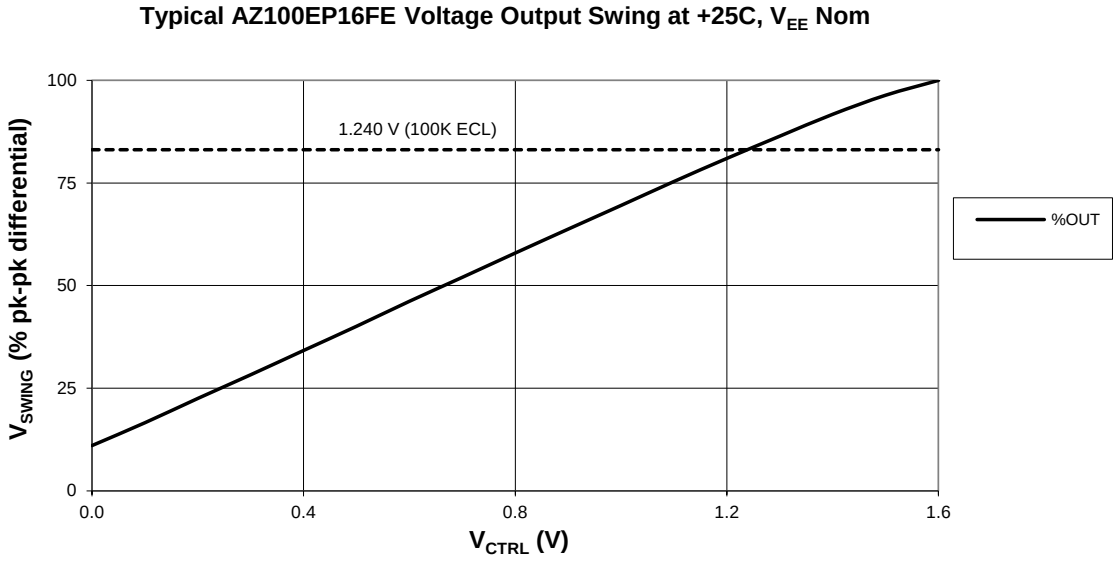


Figure 3 - Typical Voltage Output Swing at Nominal Conditions

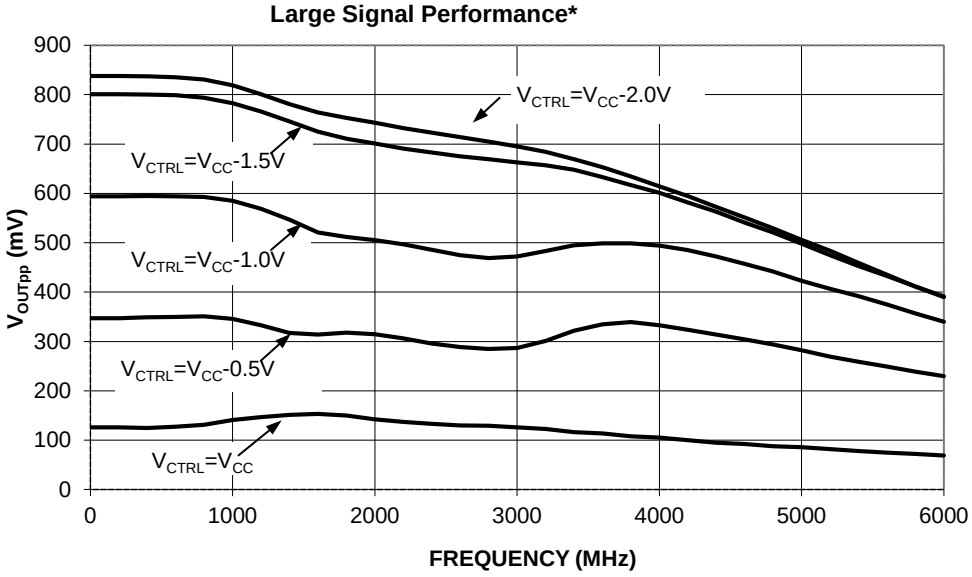


Figure 4 - Large Signal Performance

PERFORMANCE DATA

Table 2 – Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which device life may be impaired.

Symbol	Characteristic	Condition	Rating	Unit
V_{CC}	PECL Power Supply	V_{EE} = 0V	0 to +4.5	V
V_I	PECL Input Voltage	V_{EE} = 0V	0 to +4.5	V
V_{EE}	ECL Power Supply	V_{CC} = 0V	-4.5 to 0	V
V_I	ECL Input Voltage	V_{CC} = 0V	-4.5 to 0	V
I_{OUT}	Output Current	Continuous	22	mA
		Surge	44	
T_A	Operating Temperature Range		-40 to +85	°C
T_{STG}	Storage Temperature Range		-65 to +150	°C
ESD_{HBM}	Human Body Model		2500	V
ESD_{MM}	Machine Model		200	V
ESD_{CDM}	Charged Device Model		2500	V

Table 3 - 100K ECL DC Characteristics

100K ECL DC Characteristics (V_{EE} = -3.0V to -3.6V, V_{CC} = GND)

Symbol	Characteristic	-40 °C			0 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	-1095		-890	-1035		-870	-1000	-920	-840	-940		-760	mV
V_{OL}	Output LOW Voltage[1] V_{CTRL} = V_{REF}	-1935		-1745	-1905		-1715	-1885	-1790	-1790	-1830		-1640	mV
V_{OL}	Output LOW Voltage[1] V_{CTRL} = V_{CC}	-1140		-950	-1120		-930	-1100	-1005	-1005	-1055		-865	mV
V_{REF}	Reference Voltage	-1700		-1500	-1700		-1500	-1700		-1500	-1700		-1500	mV
I_{IH}	Input HIGH Current			80			80			80			80	µA
	D, $\overline{D}$			400			400			400			400	
I_{IL}	V_{CTRL}	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current	20	26	35	21	27	36	21	28	36	22	31	38	mA

[1] Each output is terminated through a 180Ω resistor to V_{EE}

Table 4 - 100K LVPECL DC Characteristics

100K LVPECL DC Characteristics (V_{EE} = GND V_{CC} = +3.3V)

Symbol	Characteristic	-40 °C			0 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output HIGH Voltage[1]	2205		2410	2265		2430	2300	2380	2460	2360		2540	mV
V_{OL}	Output LOW Voltage[1] V_{CTRL} = V_{REF}	1365		1555	1395		1585	1415	1510	1605	1470		1660	mV
V_{OL}	Output LOW Voltage[1] V_{CTRL} = V_{CC}	2160		2350	2180		2370	2200	2295	2390	2245		2435	mV
V_{REF}	Reference Voltage	1600		1800	1600		1800	1600		1800	1600		1800	mV
I_{IH}	Input HIGH Current			80			80			80			80	µA
	D, $\overline{D}$			400			400			400			400	
I_{IL}	V_{CTRL}	0.5			0.5			0.5			0.5			µA
I_{EE}	Power Supply Current	20	26	35	21	27	36	21	28	36	22	31	38	mA

[1] Each output is terminated through a 180Ω resistor to V_{EE}

Table 5 - AC Characteristics

AC Characteristics (V_{EE} = -3.0V to -3.6V, V_{CC} = GND or V_{EE} = GND, V_{CC} = +3.0V to +3.6V, V_{CTRL} = V_{REF})

Symbol	Characteristic	-40 °C			0 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Max Toggle Frequency[5]		>6			>6			>6			>6		GHz
t_{PLH}/t_{PHL}	Propagation Delay to Output (Diff/SE)	100	150	240	100	150	240	100	150	240	120	170	280	ps
			155			155			155			175		ps
t_{skew}	Duty Cycle Skew[1]		4	20		4	15		4	15		4	15	ps
V_{PP}	Minimum Input Swing[2]	150			150			150			150			mV
V_{CMR}	Common Mode Range[3]	V_{EE} + 2.0		V_{CC}	V_{EE} + 2.0		V_{CC}	V_{EE} + 2.0		V_{CC}	V_{EE} + 2.0		V_{CC}	V
A_v	Small Signal Gain[4]								28					dB
t_r/t_f	Output Rise/Fall Times Q (20%-80%)			130		130	130			130			130	ps

[1] Duty cycle skew is the difference between a t_{PLH} and t_{PHL} propagation delay through a device.

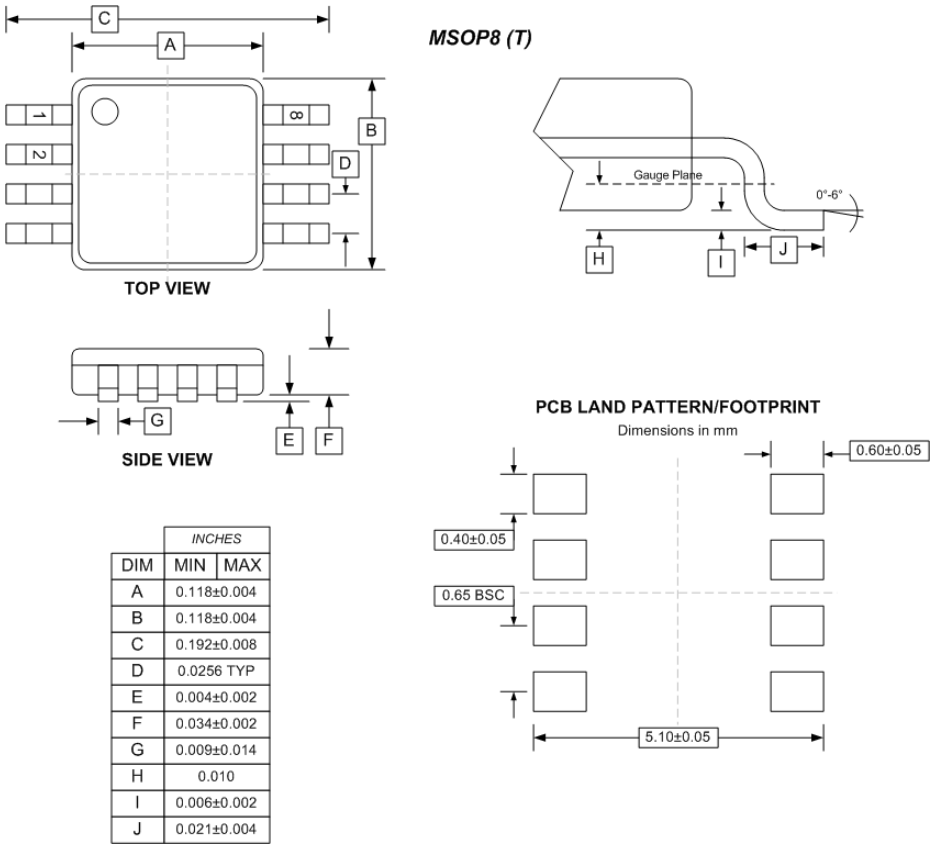
[2] V_{PP} is the minimum peak-to-peak differential input swing for which AC parameters guaranteed.

[3] The VCMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} (min) and 1V. The lower end of the V_{CMR} range varies 1:1 with V_{EE} and is equal to V_{EE}+2V

[4] See Figure 4

PACKAGE DIAGRAM

MSOP8
Green/RoHS compliant/Pb-Free
MSL=1



DIM	INCHES MIN	MAX
A	0.118±0.004	
B	0.118±0.004	
C	0.192±0.008	
D	0.0256 TYP	
E	0.004±0.002	
F	0.034±0.002	
G	0.009±0.014	
H	0.010	
I	0.006±0.002	
J	0.021±0.004	