



# MITSUBISHI LSIs

## M5M27C102K, -12, -15, -2/ M5M27C102JK -12, -15, -2

1048576-BIT (65536-WORD BY 16-BIT)  
CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### DESCRIPTION

The Mitsubishi M5M27C102K, JK is a high-speed 1048576-bit ultraviolet erasable and electrically reprogrammable read only memory. It is suitable for microprocessor programming applications where rapid turn-around is required. The M5M27C102K, JK is fabricated by N-channel double polysilicon gate for Memory and CMOS technology for peripheral circuits, and is available in DIP/CLCC with a transparent lid.

### FEATURES

- 65536 word x 16 bit organization
- Access time M5M27C102K-12, JK-12 . . . 120ns (max.)  
M5M27C102K-15, JK-15 . . . 150ns (max.)  
M5M27C102K-2, JK-2 . . . . . 200ns (max.)  
M5M27C102K . . . . . 250ns (max.)
- Two line control  $\overline{OE}$ ,  $\overline{CE}$
- Low power current ( $I_{CC}$ ): Active . . . . . 50mA (max.)  
Stand by . . . . . 1mA (max.)
- Single 5V power supply
- Programming voltage . . . . . 12.5V
- 3-State output buffer
- Input and output TTL-compatible in read and program mode
- Standard 40 pin DIP
- Word programming algorithm
- Page programming algorithm

### APPLICATION

Microcomputer systems and peripheral equipment

### FUNCTION

#### Read

Set the  $\overline{CE}$  and  $\overline{OE}$  terminals to the read mode (low level). Low level input to  $\overline{CE}$  and  $\overline{OE}$  and address signals to the address inputs ( $A_0 \sim A_{15}$ ) make the data contents of the designated address location available at the data input/output ( $D_0 \sim D_{15}$ ). When the  $\overline{CE}$  or  $\overline{OE}$  signal is high, data input/output are in a floating state.

When the  $\overline{CE}$  signal is high, the device is in the standby mode or power-down mode.

#### Programming

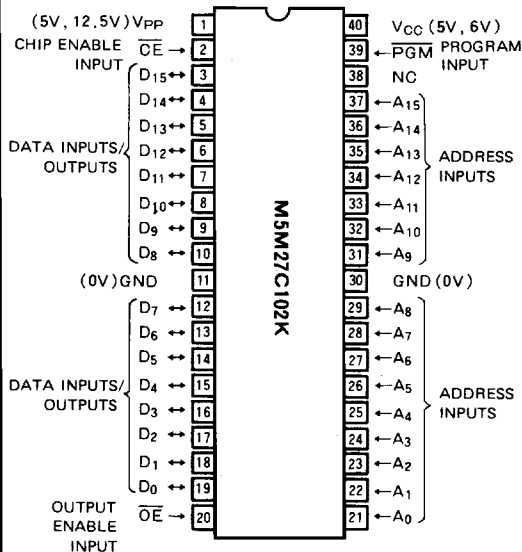
##### (Word programming algorithm)

The M5M27C102K, JK enters the byte programming mode when 12.5V is supplied to the  $V_{PP}$  power supply input,  $\overline{CE}$  is at low level and  $\overline{OE}$  is at high level. A location is designated by address signals ( $A_0 \sim A_{15}$ ), and the data to be programmed must be applied at 16-bits in parallel to the data inputs ( $D_0 \sim D_{15}$ ). In this state, word programming is completed when  $\overline{PGM}$  is at low level.

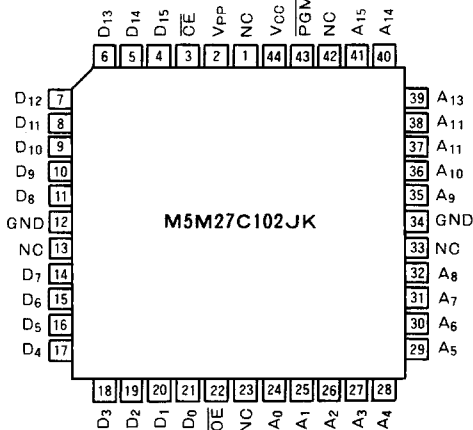
##### (Page programming algorithm)

Page programming feature of the M5M27C102K, JK allows 2 works of data to be simultaneously programmed. The

### PIN CONFIGURATION (TOP VIEW)



Outline 40K4 (DIP: K)



Outline 44K0 (CLCC: JK)

NC: NO CONNECTION

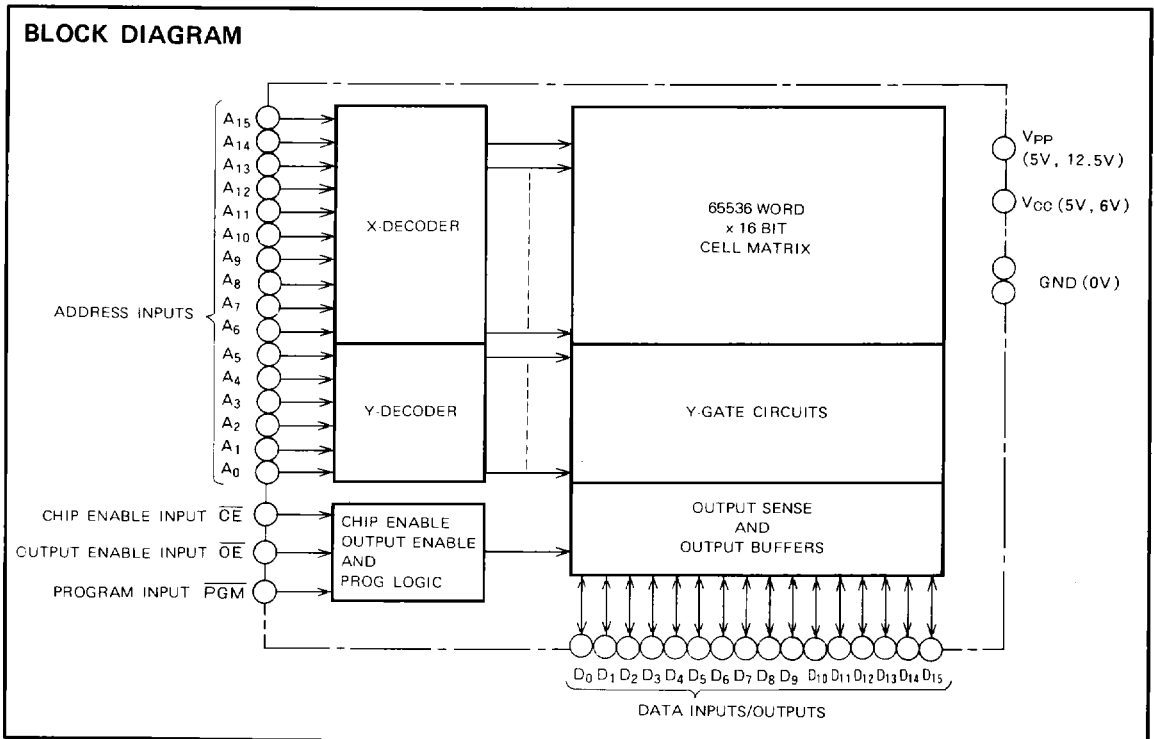
destination addresses for a page programming operation must reside on the same page; that is,  $A_1$  through  $A_{15}$  must not change. At first, the M5M27C102K, JK enters the page data latch mode when  $V_{PP} = 12.5V$ ,  $\overline{CE} = "H"$ ,  $\overline{OE} = "L"$  and  $\overline{PGM} = "H"$ . A first and second locations in same page are designated by address signals ( $A_0 \sim A_{15}$ ), and the data to be programmed must be applied to each location at 16-bits in parallel to the data inputs ( $D_0 \sim D_{15}$ ). In this state, the data (2 words) latch is completed. Then the M5M27C102K, JK enters the page programming mode when  $\overline{OE} = "H"$ . In this state, page (2 words) programming is completed when  $\overline{PGM} = "L"$ .

# M5M27C102K,-12,-15,-2/M5M27C102JK -12,-15,-2

## 1048576-BIT(65536-WORD BY 16-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### Erase

Erase is effected by exposure to ultraviolet light with a wavelength of 2537Å at an intensity of approximately 15WS/cm<sup>2</sup>. Sunlight and fluorescent light may contain ultraviolet light sufficient to erase the programmed information. For any operation in the read mode, the transparent lid should be covered with opaque tape.



### MODE SELECTION

Mode	Pins (K/JK)	$\overline{CE}$ (2/3)	$\overline{OE}$ (20/22)	$\overline{PGM}$ (39/43)	V <sub>PP</sub> (1/2)	V <sub>CC</sub> (40/44)	Data I/O (3~10, 12~19) (4~11, 14~21)
Read		V <sub>IL</sub>	V <sub>IL</sub>	X*	5V	5V	Data out
Output disable		V <sub>IL</sub>	V <sub>IH</sub>	X*	5V	5V	Floating
Standby (Power down)		V <sub>IH</sub>	X*	X*	5V	5V	Floating
Word program		V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	12.5V	6V	Data in
Program verify		V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	12.5V	6V	Data out
Page data latch		V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	12.5V	6V	Data in
Page program		V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IL</sub>	12.5V	6V	Floating
Program inhibit		V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IL</sub>	12.5V	6V	Floating
		V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	12.5V	6V	
		V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	12.5V	6V	
		V <sub>IH</sub>	V <sub>IH</sub>	V <sub>IH</sub>	12.5V	6V	

\* : X can be either V<sub>IL</sub> or V<sub>IH</sub>.

# M5M27C102K, -12, -15, -2 / M5M27C102JK -12, -15, -2

## 1048576-BIT(65536-WORD BY 16-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Test condition	Ratings	Unit
V <sub>I1</sub>	All input or output voltage except V <sub>PP</sub> , A <sub>0</sub>	With respect to Ground	-0.6 ~ 7	V
V <sub>I2</sub>	V <sub>PP</sub> supply voltage		-0.6 ~ 14.0	V
V <sub>I3</sub>	A <sub>9</sub> supply voltage		-0.6 ~ 13.5	V
T <sub>OPR</sub>	Operating temperature		-10 ~ 80	°C
T <sub>STG</sub>	Storage temperature		-65 ~ 125	°C

Note 1: Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods affects device reliability.

### READ OPERATION

#### DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 0 ~ 70°C, V<sub>CC</sub> = 5V ± 5%, V<sub>PP</sub> = V<sub>CC</sub>, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I <sub>LI</sub>	Input load current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>			10	μA
I <sub>LO</sub>	Output leakage current	V <sub>OUT</sub> = 0 ~ V <sub>CC</sub>			10	μA
I <sub>PP1</sub>	V <sub>PP</sub> current read	V <sub>PP</sub> = 5.5V		1	100	μA
I <sub>SB1</sub>	V <sub>CC</sub> current standby	$\overline{OE} = V_{IH}$			1	mA
I <sub>SB2</sub>		$\overline{OE} = V_{CC}$		1	100	μA
I <sub>CC1</sub>	V <sub>CC</sub> current Active	$\overline{OE} = \overline{OE} = V_{IL}$			50	mA
I <sub>CC2</sub>		f = 6.7MHz, I <sub>out</sub> = 0mA			50	mA
V <sub>IL</sub>	Input low voltage		-0.1		0.8	V
V <sub>IH</sub>	Input high voltage		2.0		V <sub>CC</sub> + 1	V
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 2.1mA			0.45	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> = -400μA	2.4			V

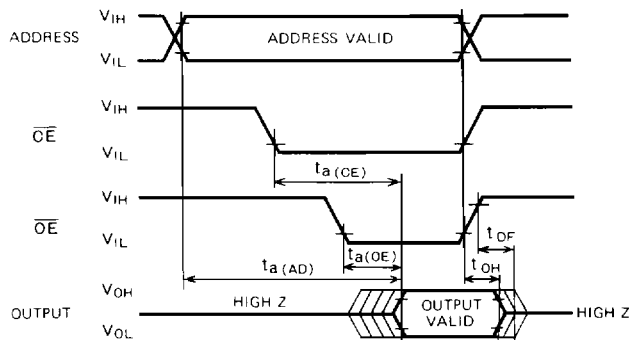
Note 2: Typical values are at T<sub>a</sub> = 25°C and nominal supply voltages.

#### AC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 0 ~ 70°C, V<sub>CC</sub> = 5V ± 5%, V<sub>PP</sub> = V<sub>CC</sub>, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits						Unit		
			M5M27C102K-12		M5M27C102K-15		M5M27C102K-2				
			Min	Max	Min	Max	Min	Max			
t <sub>a</sub> (AD)	Address to output delay	$\overline{OE} = \overline{OE} = V_{IL}$		120		150		200		250	ns
t <sub>a</sub> (OE)	$\overline{OE}$ to output delay	$\overline{OE} = V_{IL}$		120		150		200		250	ns
t <sub>a</sub> (OE)	Output enable to output delay	$\overline{OE} = V_{IL}$		60		60		75		100	ns
t <sub>DF</sub>	Output enable high to output float	$\overline{OE} = V_{IL}$	0	50	0	50	0	60	0	60	ns
t <sub>OH</sub>	Output hold from $\overline{OE}$ or $\overline{OE}$	$\overline{OE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

Note 3: V<sub>CC</sub> must be applied simultaneously V<sub>PP</sub> and removed simultaneously V<sub>PP</sub>.

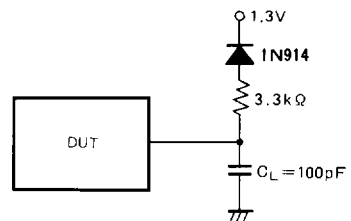
### AC WAVEFORMS



Test conditions for A.C. characteristics  
 Input voltage: V<sub>IL</sub> = 0.45V, V<sub>IH</sub> = 2.4V  
 Input rise and fall times: ≤ 20ns  
 Reference voltage at timing measurement: Input, Output  
 "L" = 0.8V, "H" = 2V.

Output load: 1TTL gate + C<sub>L</sub> (100pF)

or



# M5M27C102K, -12, -15, -2/M5M27C102JK -12, -15, -2

## 1048576-BIT(65536-WORD BY 16-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C <sub>IN</sub>	Input capacitance (Address, $\overline{CE}$ , $\overline{OE}$ , PGM)	T <sub>a</sub> = 25°C, f = 1MHz, V <sub>I</sub> = V <sub>O</sub> = 0V			15	pF
C <sub>OUT</sub>	Output capacitance				15	pF

### PROGRAM OPERATION

#### WORD PROGRAMMING ALGORITHM

First set V<sub>CC</sub> = 6V, V<sub>PP</sub> = 12.5V and then set an address to first address to be programmed. After applying 0.2 ms program pulse (PGM) to the address, verify is performed. If the output data of that address is not verified correctly, apply one more 0.2 ms program pulse. The programmer continues 0.2 ms pulse-then-verify routines until the device verify correctly or twenty five of these pulse-then-verify routines have been completed. The programmer also

maintains its total number of 0.2 ms pulse applied to that address in register X. And then applied a program pulse X times of 0.2 ms width as an overprogram pulse. When the programming procedure above is finished, step to the next address and repeat this procedure till last address to be programmed. When the entire addresses have been programmed completely, all addresses should be verified with V<sub>CC</sub> = V<sub>PP</sub> = 5V.

#### DC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I <sub>LI</sub>	Input current	V <sub>IN</sub> = 0 ~ V <sub>CC</sub>			10	μA
V <sub>OL</sub>	Output low voltage	I <sub>OL</sub> = 2.1mA			0.45	V
V <sub>OH</sub>	Output high voltage	I <sub>OH</sub> = -400μA	2.4			V
V <sub>IL</sub>	Input low voltage		-0.1		0.8	V
V <sub>IH</sub>	Input high voltage		2.0		V <sub>CC</sub>	V
I <sub>CC</sub>	V <sub>CC</sub> supply current				50	mA
I <sub>PP</sub>	V <sub>PP</sub> supply current	$\overline{CE} = \overline{PGM} = V_{IL}$			50	mA

#### AC ELECTRICAL CHARACTERISTICS (T<sub>a</sub> = 25 ± 5°C, V<sub>CC</sub> = 6V ± 0.25V, V<sub>PP</sub> = 12.5V ± 0.3V, unless otherwise noted)

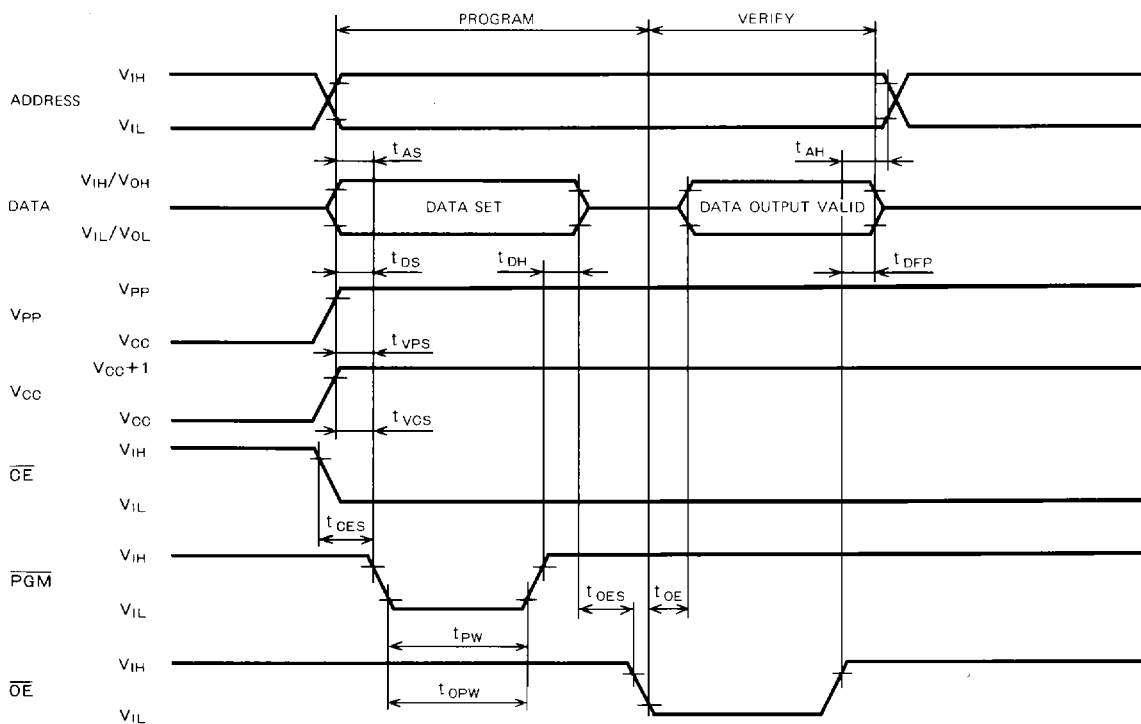
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t <sub>AS</sub>	Address setup time		2			μs
t <sub>OES</sub>	$\overline{OE}$ set up time		2			μs
t <sub>DS</sub>	Data setup time		2			μs
t <sub>AH</sub>	Address hold time		0			μs
t <sub>DH</sub>	Data hold time		2			μs
t <sub>DFF</sub>	Chip enable to output float delay		0		130	ns
t <sub>VCS</sub>	V <sub>CC</sub> setup time		2			μs
t <sub>VPS</sub>	V <sub>PP</sub> setup time		2			μs
t <sub>PW</sub>	PGM initial program pulse width		0.19	0.2	0.21	ms
t <sub>OPW</sub>	PGM over program pulse width		0.19		5.25	ms
t <sub>CES</sub>	$\overline{CE}$ setup time		2			μs
t <sub>OE</sub>	Data valid from $\overline{OE}$				150	ns

Note 4: V<sub>CC</sub> must be applied simultaneously V<sub>PP</sub> and removed simultaneously V<sub>PP</sub>.

# M5M27C102K, -12, -15, -2/M5M27C102JK -12, -15, -2

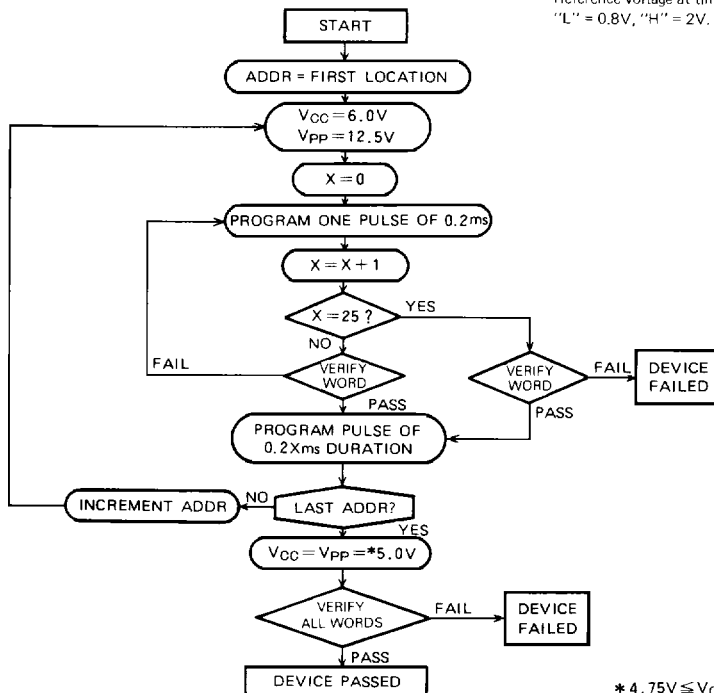
## 1048576-BIT(65536-WORD BY 16-BIT) CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

### AC WAVEFORMS



Test conditions for A.C. characteristics  
 Input voltage:  $V_{IL} = 0.45V$ ,  $V_{IH} = 2.4V$   
 Input rise and fall times:  $\leq 20ns$   
 Reference voltage at timing measurement: Input, Output  
 "L" = 0.8V, "H" = 2V.

### WORD PROGRAMMING ALGORITHM FLOW CHART



\*  $4.75V \leq V_{CC} = V_{pp} \leq 5.25V$

**M5M27C102K, -12, -15, -2/M5M27C102JK -12, -15, -2****1048576-BIT(65536-WORD BY 16-BIT)  
CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM****PAGE PROGRAMMING ALGORITHM**

First set  $V_{CC} = 6V$ ,  $V_{PP} = 12.5V$  and then set an address to first page address to be programmed. After data of 2 words are latched, these latch data are programmed simultaneously by applying 0.2 ms program pulse. Then a verify is performed. If each output data is not verified correctly, apply one more 0.2 ms program pulse. The programmer continues 0.2 ms pulse-then-verify routines until each output data is verified correctly or twenty five of these pulse-then-verify routines have been completed.

The programmer also maintains its total number of 0.2 ms pulse applied to that page addresses in register X. And then applied a program pulse X times of 0.2 ms width as an overprogram pulse. When the programming procedure above is finished, step to the next page address and repeat this procedure till last page address to be programmed. When the entire page addresses have been programmed completely, all addresses should be verified with  $V_{CC} = V_{PP} = 5V$ .

**DC ELECTRICAL CHARACTERISTICS** ( $T_a = 25 \pm 5^\circ C$ ,  $V_{CC} = 6V \pm 0.25V$ ,  $V_{PP} = 12.5V \pm 0.3V$ , unless otherwise noted)

Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$I_{LI}$	Input current	$V_{IN} = 0 \sim V_{CC}$			10	$\mu A$
$V_{OL}$	Output low voltage	$I_{OL} = 2.1mA$			0.45	V
$V_{OH}$	Output high voltage	$I_{OH} = -400\mu A$	2.4			V
$V_{IL}$	Input low voltage		-0.1		0.8	V
$V_{IH}$	Input high voltage		2.0		$V_{CC}$	V
$I_{CC}$	$V_{CC}$ supply current				50	mA
$I_{PP}$	$V_{PP}$ supply current	$\overline{PGM} = V_{IL}$			100	mA

**AC ELECTRICAL CHARACTERISTICS** ( $T_a = 25 \pm 5^\circ C$ ,  $V_{CC} = 6V \pm 0.25V$ ,  $V_{PP} = 12.5V \pm 0.3V$ , unless otherwise noted)

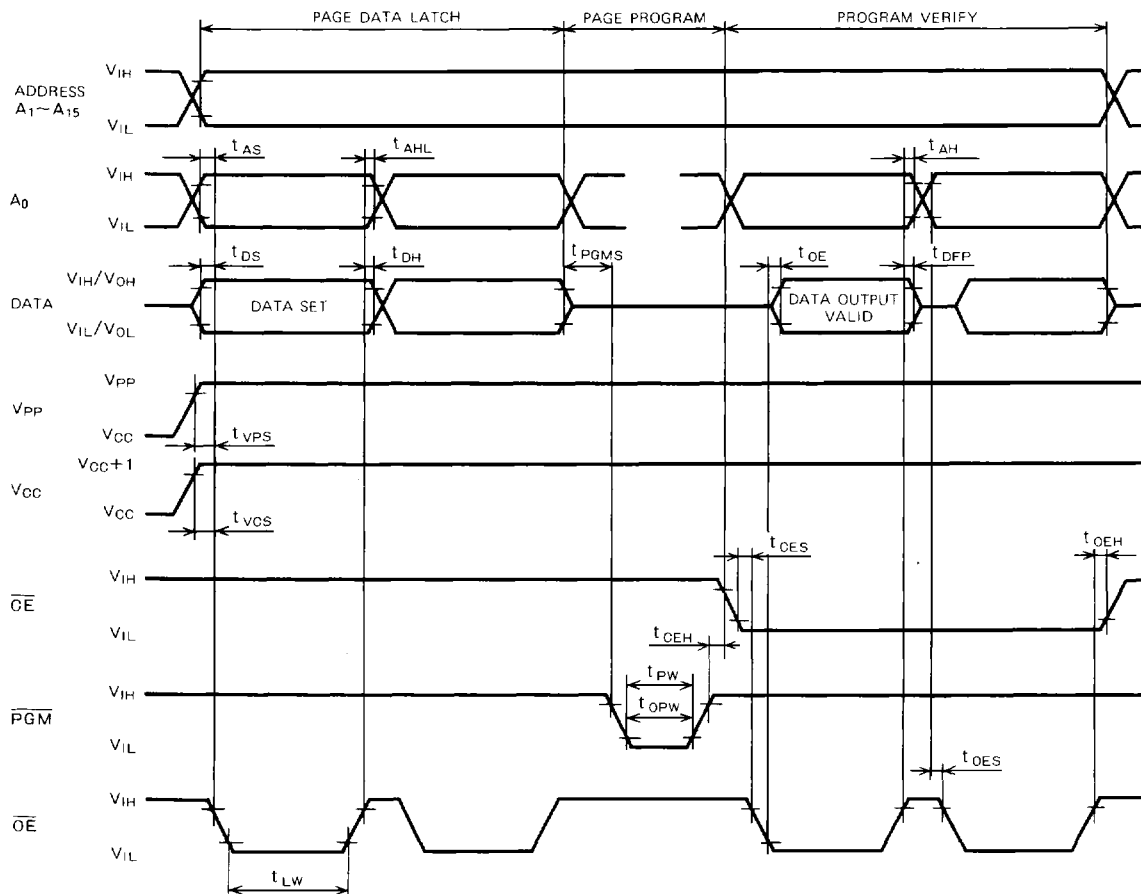
Symbol	Parameter	Test condition	Limits			Unit
			Min	Typ	Max	
$t_{AS}$	Address setup time		2			$\mu S$
$t_{OES}$	$\overline{OE}$ setup time		2			$\mu S$
$t_{DS}$	Data setup time		2			$\mu S$
$t_{AH}$	Address hold time		0			$\mu S$
$t_{AHL}$			2			$\mu S$
$t_{DH}$	Data hold time		2			$\mu S$
$t_{DFP}$	$\overline{OE}$ to output float delay		0		130	ns
$t_{VCS}$	$V_{CC}$ setup time		2			$\mu S$
$t_{VPS}$	$V_{PP}$ setup time		2			$\mu S$
$t_{PW}$	$\overline{PGM}$ initial program pulse width		0.19	0.2	0.21	ms
$t_{OPW}$	$\overline{PGM}$ over program pulse width		0.19		5.25	ms
$t_{CES}$	$\overline{CE}$ setup time		2			$\mu S$
$t_{OE}$	Data valid from $\overline{OE}$				150	ns
$t_{LW}$	Data latch time		1			$\mu S$
$t_{PGMS}$	$\overline{PGM}$ setup time		2			$\mu S$
$t_{CEH}$	$\overline{CE}$ hold time		2			$\mu S$
$t_{OEH}$	$\overline{OE}$ hold time		2			$\mu S$

Note 5.  $V_{CC}$  must be applied simultaneously  $V_{PP}$  and removed simultaneously  $V_{PP}$ .

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## AC WAVEFORMS

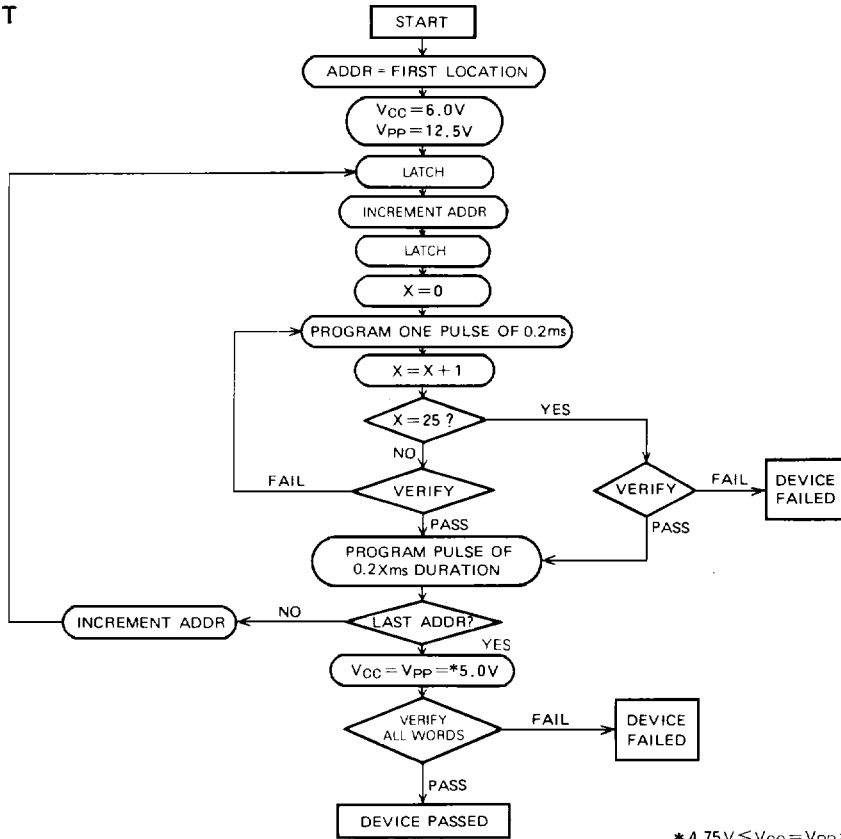


Test condition for A.C characteristics  
 Input voltage V<sub>IL</sub> = 0.45V, V<sub>IH</sub> = 2.4V  
 Input rise and fall time: (10% ~ 90%) ≤ 20ns  
 Reference voltage at timing measurement Input, Output "L" = 0.8V, "H" = 2V.

# M5M27C102K, -12, -15, -2/M5M27C102JK -12, -15, -2

**1048576-BIT(65536-WORD BY 16-BIT)  
CMOS ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM**

## PAGE PROGRAMMING ALGORITHM FLOW CHART



\* 4.75V ≤ V<sub>CC</sub> = V<sub>PP</sub> ≤ 5.25V

### DEVICE IDENTIFIER MODE

The Device Identifier Mode allows the reading of a binary code from the EPROM that identifies the manufacturer and device type.

The EPROM Programmer reads the manufacturer code and the device code and automatically selects the corresponding programming algorithm.

### M5M27C102K, JK DEVICE IDENTIFIER CODE

Code	Pins (K/JK)	A <sub>0</sub> (21/24)	D <sub>15</sub> (3/4)	D <sub>14</sub> (4/5)	D <sub>13</sub> (5/6)	D <sub>12</sub> (6/7)	D <sub>11</sub> (7/8)	D <sub>10</sub> (8/9)	D <sub>9</sub> (9/10)	D <sub>8</sub> (10/11)	D <sub>7</sub> (12/14)	D <sub>6</sub> (13/15)	D <sub>5</sub> (14/16)	D <sub>4</sub> (15/17)	D <sub>3</sub> (16/18)	D <sub>2</sub> (17/19)	D <sub>1</sub> (18/20)	D <sub>0</sub> (19/21)	Hex Data
Manufacturer code	V <sub>IL</sub>	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	001C
Device code	V <sub>IH</sub>	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1	0	1	0085

Note 6: A<sub>9</sub> = 12.0±0.5V  
 A<sub>1</sub> ~ A<sub>8</sub>, A<sub>10</sub> ~ A<sub>15</sub>,  $\overline{CE}$ ,  $\overline{OE}$  = V<sub>IL</sub>, PGM = V<sub>IH</sub>  
 V<sub>CC</sub> = V<sub>PP</sub> = 5V ± 5%