

**COS/MOS
INTEGRATED
CIRCUIT**

41C 09153 D T-46-07-10

7929225 S G S SEMICONDUCTOR CORP

HEX "D" - TYPE FLIP-FLOP

- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED AT 20V FOR HCC DEVICE
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT CURRENT OF 100 nA AT 18V AND 25°C FOR HCC DEVICE
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC TENTATIVE STANDARD No. 13A, "STANDARD SPECIFICATIONS FOR DESCRIPTION OF "B" SERIES CMOS DEVICES"

The **HCC 40174B** (extended temperature range) and **HCF 40174B** (intermediate temperature range) are monolithic integrated circuits available in 16-lead dual in-line plastic or ceramic package, ceramic flat package and plastic micropackage.

The **HCC/HCF 40174B** consists of six identical 'D'-type flip-flops having independent DATA inputs. The **CLOCK** and **CLEAR** inputs are common to all six units. Data is transferred to the Q outputs on the positive-going transition of the clock pulse. All six flip-flops are simultaneously reset by a low level on the **CLEAR** input.

ABSOLUTE MAXIMUM RATINGS

V_{DD}^*	Supply voltage: HCC types HCF types	-0.5 to 20 -0.5 to 18	V V
V_I	Input voltage	-0.5 to $V_{DD} + 0.5$	V
I_I	DC input current (any one input)	± 10	mA
P_{tot}	Total power dissipation (per package)	200	mW
	Dissipation per output transistor for T_{op} = full package-temperature range	100	mW
T_{op}	Operating temperature: HCC types HCF types	-55 to 125 -40 to 85	°C °C
T_{stg}	Storage temperature	-65 to 150	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

* All voltages are with respect to V_{SS} (GND).

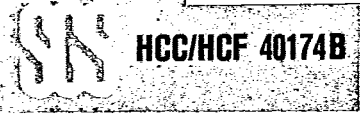
ORDERING NUMBERS:

HCC 40174 BD for dual in-line ceramic package
 HCC 40174 BF for dual in-line ceramic package, frit seal
 HCC 40174 BK for ceramic package
 HCF 40174 BE for dual in-line plastic package
 HCF 40174 BF for dual in-line ceramic package, frit seal
 HCF 40174 BM for plastic micropackage

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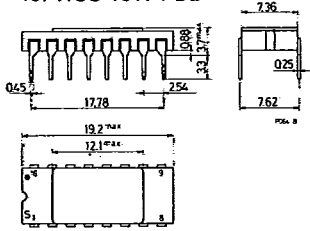


T-46-07-10

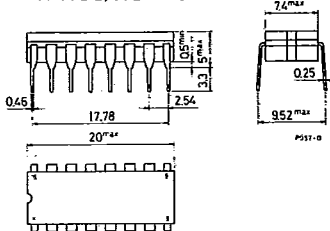
7929225 S G S SEMICONDUCTOR CORP 41C 09154 D

MECHANICAL DATA (dimensions in mm)

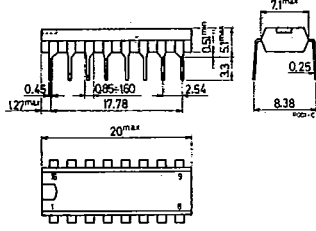
Dual in-line ceramic package for HCC 40174 BD



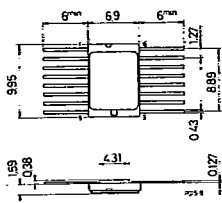
Dual in-line ceramic package for HCC/HCF 40174 BF



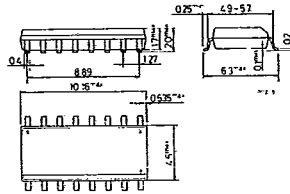
Dual in-line plastic package for HCF 40174 BE



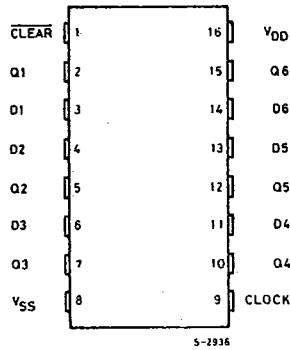
Ceramic flat package for HCC 40174 BK



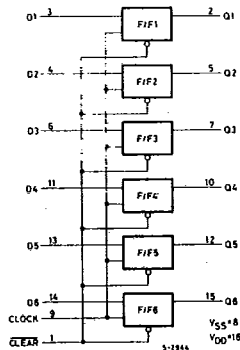
Plastic micropackage for HCF 40174 BM



PIN CONNECTIONS



FUNCTIONAL DIAGRAM

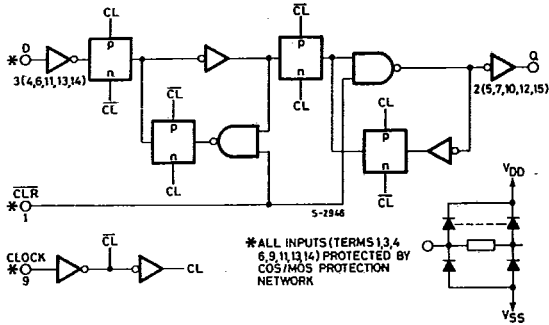


RECOMMENDED OPERATING CONDITIONS

V_{DD}	Supply voltage: HCC types HCF types	3 to 18 3 to 15	V V
V_I	Input voltage	0 to V_{DD}	V
T_{op}	Operating temperature: HCC types HCF types	-55 to 125 -40 to 85	°C °C



LOGIC DIAGRAM AND TRUTH TABLE
(1 of 6 Flip-Flops)

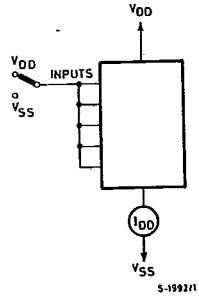


INPUTS			OUTPUT
CLOCK	DATA	CLEAR	Q
	0	1	0
	1	1	1
	X	1	NC
X	X	0	0

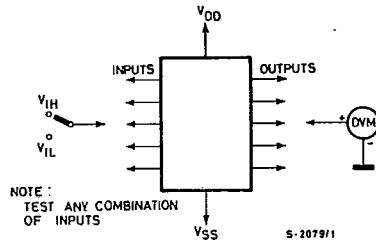
1 = High level
0 = Low level
X = Don't Care
NC = No Change

TEST CIRCUITS

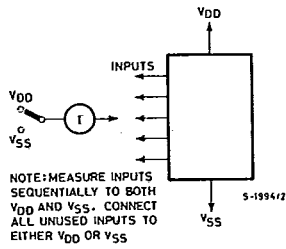
Quiescent device current



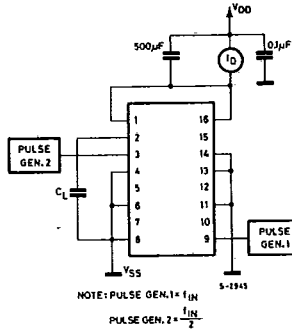
Input voltage



Input leakage current



Dynamic power dissipation





7929225 S G S SEMICONDUCTOR CORP

T-46-07-10

41C 09156 D

STATIC ELECTRICAL CHARACTERISTICS (over recommended operating conditions)

Parameter	Test conditions				Values						Unit		
	V _I (V)	V _O (V)	I _O (μA)	V _{DD} (V)	T _{Low} *		25°C			T _{High} *			
					Min.	Max.	Min.	Typ.	Max.	Min.		Max.	
I _L Quiescent current	HCC types	0/ 5			5		1		0.02	1		30	μA
		0/10			10		2		0.02	2		60	
		0/15			15		4		0.02	4		120	
	HCF types	0/20			20		20		0.04	20		600	
		0/ 5			5		4		0.02	4		30	
		0/10			10		8		0.02	8		60	
V _{OH} Output high voltage	0/ 5		< 1	5	4.95		4.95			4.95		V	
	0/10		< 1	10	9.95		9.95			9.95		V	
	0/15		< 1	15	14.95		14.95			14.95		V	
V _{OL} Output low voltage	5/0		< 1	5		0.05		0.05		0.05		V	
	10/0		< 1	10		0.05		0.05		0.05		V	
	15/0		< 1	15		0.05		0.05		0.05		V	
V _{IH} Input high voltage		0.5/4.5	< 1	5	3.5		3.5			3.5		V	
		1/9	< 1	10	7		7			7		V	
		1.5/13.5	< 1	15	11		11			11		V	
V _{IL} Input low voltage		4.5/0.5	< 1	5		1.5		1.5		1.5		V	
		9/1	< 1	10		3		3		3		V	
		13.5/1.5	< 1	15		4		4		4		V	
I _{OH} Output drive current	HCC types	0/ 5	2.5		5	-2		-1.6	-3.2		-1.15		mA
		0/ 5	4.6		5	-0.64		-0.51	-1		-0.36		
		0/10	9.5		10	-1.6		-1.3	-2.6		-0.9		
	HCF types	0/15	13.5		15	-4.2		-3.4	-6.8		-2.4		
		0/ 5	2.5		5	-1.53		-1.36	-3.2		-1.1		
		0/ 5	4.6		5	-0.52		-0.44	-1		-0.36		
I _{OL} Output sink current	HCC types	0/ 5	0.4		5	0.64		0.51	1		0.36		mA
		0/10	0.5		10	1.6		1.3	2.6		0.9		
		0/15	1.5		15	4.2		3.4	6.8		2.4		
	HCF types	0/ 5	0.4		5	0.52		0.44	1		0.36		
		0/10	0.5		10	1.3		1.1	2.6		0.9		
		0/15	1.5		15	3.6		3.0	6.8		2.4		
I _{IH} , I _{IL} Input leakage current	HCC types	0/18	Any input	18		±0.1		±10 ⁻⁵	±0.1		± 1	μA	
	HCF types	0/15		15		±0.3		±10 ⁻⁵	±0.3		± 1		
C _I Input capacitance	.Any input							5	7.5			pF	

* T_{Low} = - 55°C for HCC device: -40°C for HCF device.
 * T_{High} = +125°C for HCC device: +85°C for HCF device.
 The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD} = 5V
 2V min. with V_{DD} = 10V
 2.5V min. with V_{DD} = 15V



7929225 S G S SEMICONDUCTOR CORP

41C 09157 D T-46-07-10

DYNAMIC ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$, $C_L = 50\text{ pF}$, $R_L = 200\text{ k}\Omega$,
 typical temperature coefficient for all V_{DD} values is $0.3\%/^{\circ}\text{C}$, all input rise and fall time = 20 ns)

Parameter	Test conditions	Values			Unit	
		V_{DD} (V)	Min.	Typ.		Max.
t_{PLH} , t_{PHL}	Propagation delay time Clock to output	5		150	300	ns
		10		70	140	
		15		50	100	
t_{PHL}	Propagation delay time Clear to output	5		100	200	ns
		10		50	100	
		15		40	80	
t_{THL} , t_{TLH}	Transition time	5		100	200	ns
		10		50	100	
		15		40	80	
t_{setup}	Data setup time	5	40	20		ns
		10	20	10		
		15	10	0		
t_{hold}	Data hold time	5	80	40		ns
		10	40	20		
		15	30	15		
t_w	Clock input pulse width Low level	5	130	65		ns
		10	60	30		
		15	40	20		
t_w	Clock input pulse width High level	5	130	65		ns
		10	60	30		
		15	40	20		
t_w	Clear input pulse width Low level	5	100	50		ns
		10	50	25		
		15	40	20		
t_r , t_f	Clock input rise or fall time	5			15	μs
		10			15	
		15			15	
t_{rem}	Clear removal time	5	0	-40		ns
		10	0	-15		
		15	0	-10		
f_{CL}	Maximum clock input frequency	5	3.5	7		MHz
		10	6	12		
		15	8	16		

HCC/DCF 40174B

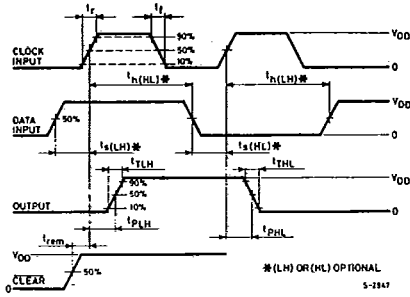
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T-46-07-10

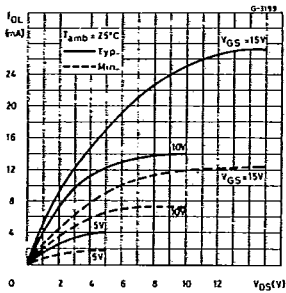
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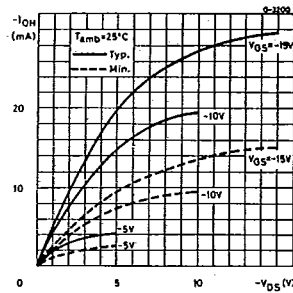
WAVEFORMS



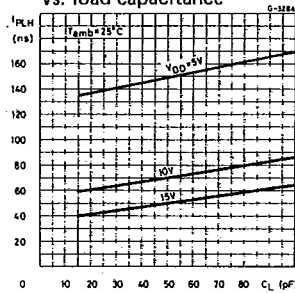
Output low (sink) current characteristics



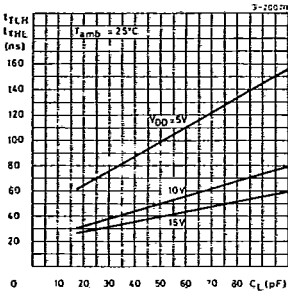
Output high (source) current characteristics



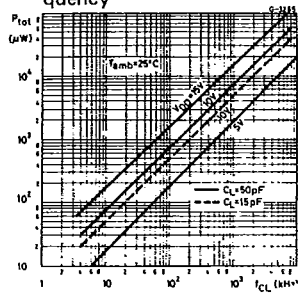
Typical propagation delay time (Clock to output) vs. load capacitance

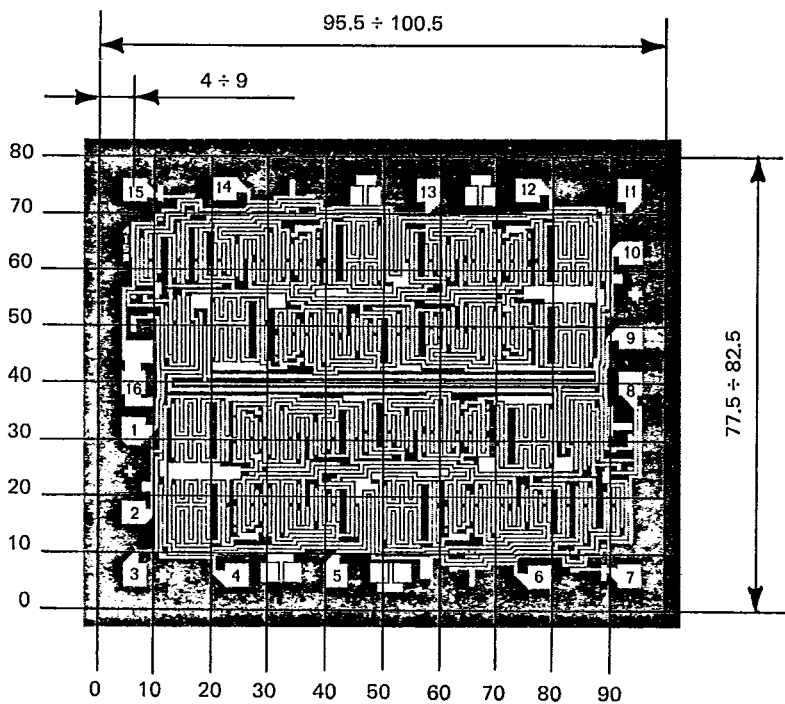


Typical transition time vs. load capacitance

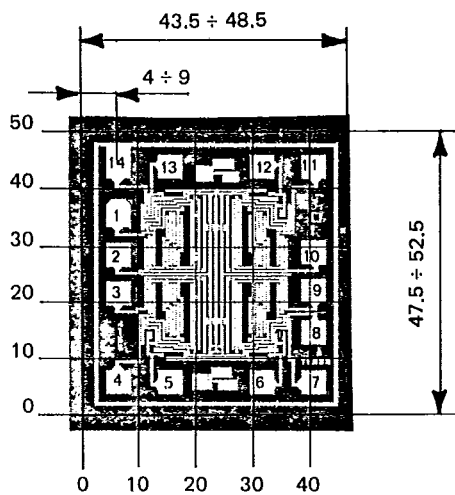


Typical dynamical power dissipation vs. Clock frequency





4015B



4016B