## 9.0 ASCENT DC ELECTRICAL CHARACTERISTICS

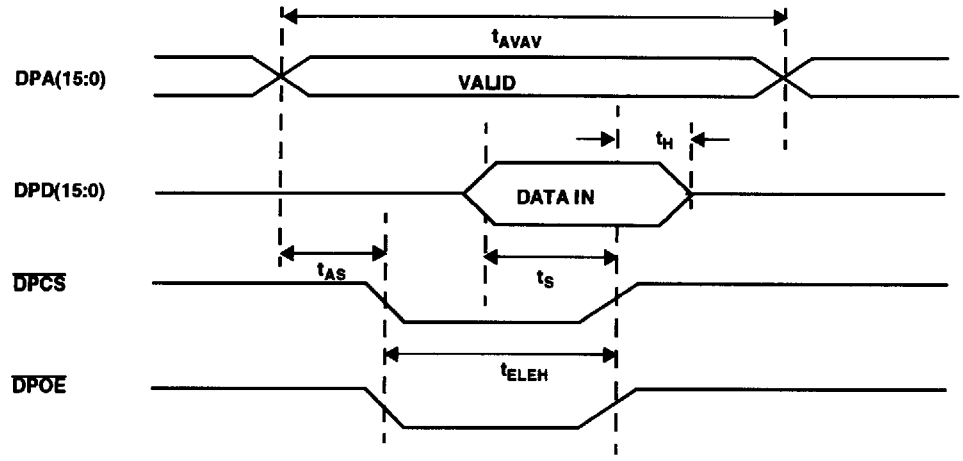
($V_{DD}$ = 5.0V±10%; $V_{SS}$ = 0V [1]; -55°C < Tc < +125°C)

| SYMBOL | PARAMETER | CONDITION | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IL}$ | Low-level input voltage | | | $.3V_{DD}$ | V |
| $V_{IH}$ | High-level input voltage | | $.7V_{DD}$ | | V |
| $I_{IN}$ | Input leakage current<br>Inputs without pull-up resistors<br>Inputs with pull-up resistors<br>Inputs with pull-up resistors | <br>$V_{IN} = V_{DD}$ or $V_{SS}$<br>$V_{IN} = V_{DD}$<br>$V_{IN} = V_{SS}$ | <br>-1<br>-10<br>-100 | <br>+1<br>+10<br>-15 | µA |
| $V_{OL}$ | CMOS low-level output voltage<br>Open drain outputs<br>All other outputs | <br>$I_{OL}$ = 8.0mA<br>$I_{OL}$ = 1.0µA | | <br>.4<br>0.05 | V |
| $V_{OH}$ | CMOS high-level output voltage<br>Open drain outputs<br>All other outputs | <br>N/A<br>$I_{OH}$ = -1.0µA | <br>N/A<br>$V_{DD}$-0.05 | | V |
| $I_{OZ}$ | Three-state output leakage current<br>Open drain outputs<br>All other outputs | <br>$I_O = V_{DD}$ or $V_{SS}$<br>$I_O = V_{DD}$ or $V_{SS}$ | <br>-20<br>-10 | <br>+20<br>+10 | µA |
| $I_{OS}$ | Short-circuit output current [2, 3]<br>All outputs<br>All outputs | <br>$V_{DD}$ = 5.5V, $V_O$ = 0V<br>$V_{DD}$ = 5.5V, $V_O = V_{DD}$ | <br>-100 | <br><br>+100 | mA |
| $C_{IN}$ | Input capacitance [4] | $f$ = 1MHz @ 0V | | 25 | pF |
| $C_{OUT}$ | Output capacitance [4]<br>Single-drive buffer | $f$ = 1MHz @ 0V | | 25 | pF |
| $C_{IO}$ | Bidirectional capacitance [4] | $f$ = 1MHz @ 0V | | 25 | pF |
| $Q_{IDD}$ | Quiescent current [5] | $f$ = 0MHz | | 375 | mA |
| $S_{IDD}$ | Standby operating current[6] | $f$ = 40MHz | | 375 | mA |

**Notes:**
1. Maximum allowable relative shift = 50mV.
2. Supplied as a design limit but not guaranteed or tested.
3. Not more than one output may be shorted at a time for maximum duration of one second.
4. Capacitance measured for initial qualification or design changes which may affect the value.
5. All inputs tied to $V_{DD}$.
6. Guaranteed by characterization, but not tested.

## 10.0 ASCENT AC ELECTRICAL CHARACTERISTICS[1]

($f$= 40MHz ±0.01%, Duty Cycle 50%±10%)

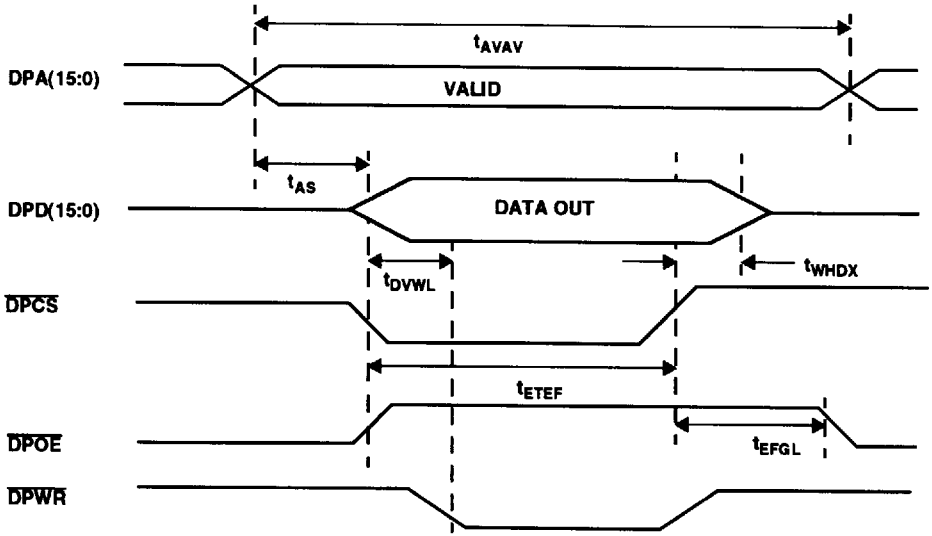



| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{AVAV}$ | Read cycle time | 240 | -- | ns |
| $t_{AS}$ | Address setup time to $\overline{DPCS}$ and $\overline{DPOE}$ | -10 | 15 | ns |
| $t_S$ | Data valid setup to $\overline{DPCS}$, $\overline{DPOE}$ inactive | 20 | -- | ns |
| $t_H$ | Data valid hold time from $\overline{DPCS}$, $\overline{DPOE}$ inactive | 10 | -- | ns |
| $t_{ELEH}$ | $\overline{DPCS}$, $\overline{DPOE}$ low width | 185 | -- | ns |

**Notes:**

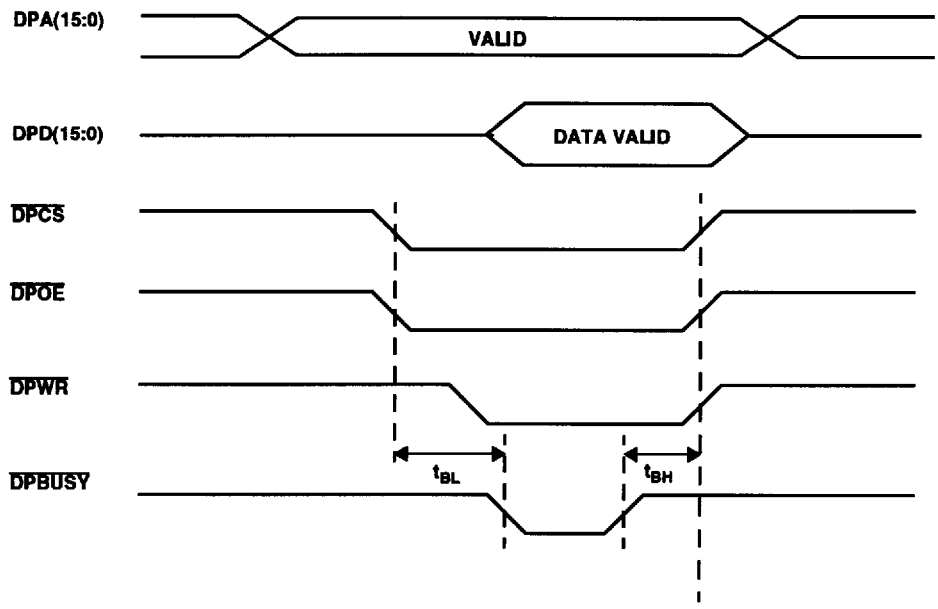
1. Guaranteed by characterization, but not tested.

**Figure 10-1. Dual-port RAM Read Timing Diagram**



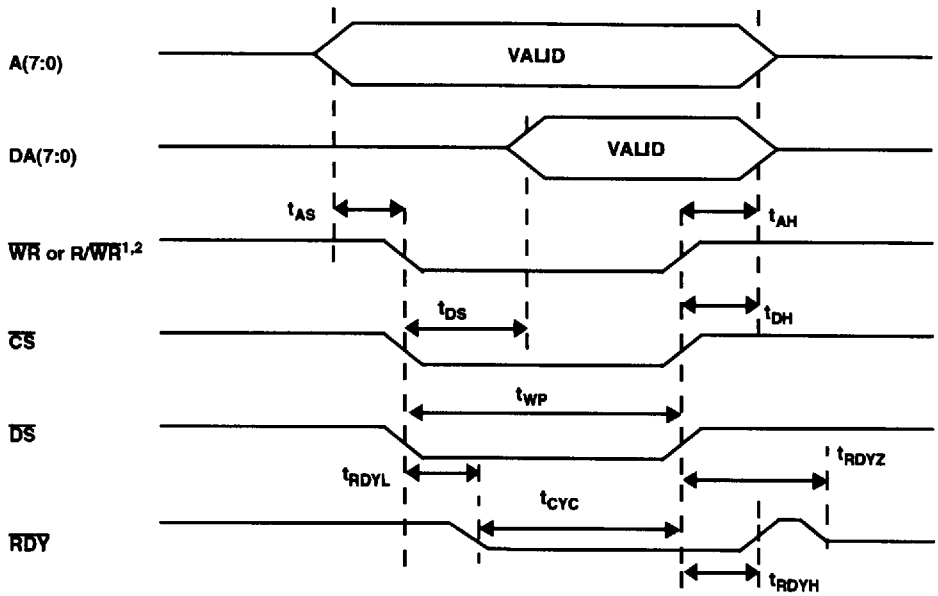

| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{AVAV}$ | Write cycle time | 240 | -- | ns |
| $t_{AS}$ | Address setup time to $\overline{DPCS}$ , $\overline{DPOE}$ and DPD(15:0) valid | -10 | 15 | ns |
| $t_{DVWL}$ | Data valid to $\overline{DPWR}$ active | 40 | 55 | ns |
| $t_{WHDX}$ | $\overline{DPWR}$ high to data invalid | 0 | -- | ns |
| $t_{ETEF}$ | $\overline{DPCS}$ low width | 185 | -- | ns |
| $t_{EFGL}$ | $\overline{DPCS}$ high to $\overline{DPOE}$ low | 45 | -- | ns |

**Figure 10-2. Dual-port RAM Write Timing Diagram**




| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{BL}$ | Busy delay from $\overline{DPCS}$ | -- | 35 | ns |
| $t_{BH}$ | Cycle hold after Busy inactive | 140 | 215 | ns |

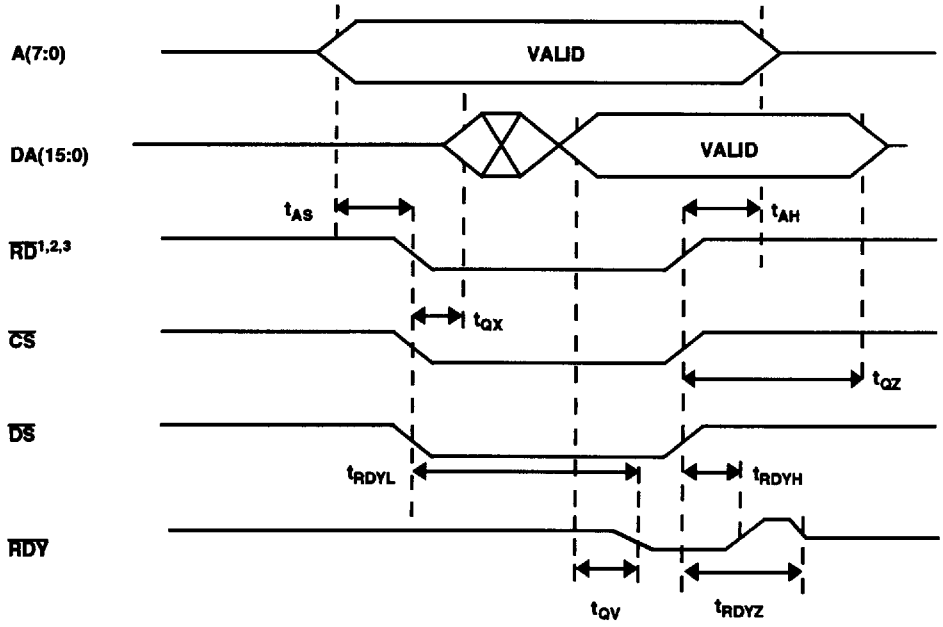
**Figure 10-3. Dual-port RAM Busy Timing**




| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0 | -- | ns |
| $t_{DS}$ | Data setup time | -- | 65 | ns |
| $t_{WP}$ | Write pulse width[3] | 120 | -- | ns |
| $t_{AH}$ | Address hold time | 0 | -- | ns |
| $t_{DH}$ | Data hold time | 0 | -- | ns |
| $t_{RDYL}$ | $\overline{RDY}$ low time | -- | 120 | ns |
| $t_{RDYH}$ | $\overline{RDY}$ high time | -- | 25 | ns |
| $t_{RDYZ}$ | $\overline{RDY}$ high Z | -- | 120 | ns |
| $t_{CYC}$ | Minimum cycle time | 0 | -- | ns |

Notes:
1 A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$.
3. For applications not using $\overline{RDY}$ signal.

**Figure 10-4. Non-Multiplexed Memory/Register Write (8 Bit)**

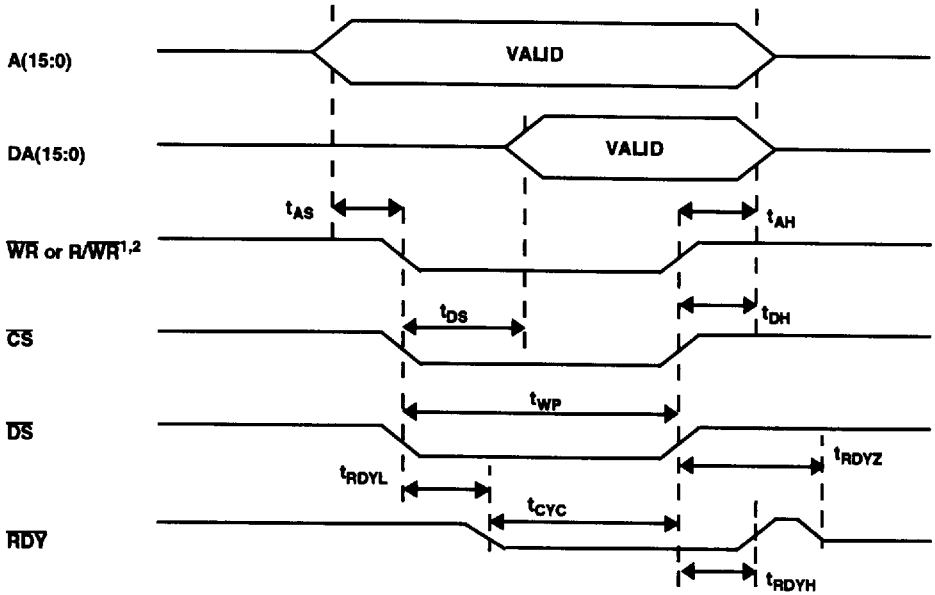



| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0 | -- | ns |
| $t_{QX}$ | Data low Z | 0 | 35 | ns |
| $t_{AH}$ | Address hold time | 0 | -- | ns |
| $t_{QV}$ | Data valid to $\overline{RDY}$ low | 35 | -- | ns |
| $t_{QZ}$ | Data high Z | 0 | 25 | ns |
| $t_{RDYL}$ | $\overline{RDY}$ low time | -- | 350 | ns |
| $t_{RDYH}$ | $\overline{RDY}$ high time | -- | 25 | ns |
| $t_{RDYZ}$ | $\overline{RDY}$ high Z | -- | 120 | ns |

**Note:**

1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
3. When using R/$\overline{WR}$ as an input signal tie $\overline{RD}$ to a logical "1". During the read cycle R/$\overline{WR}$ remains a logical "1".

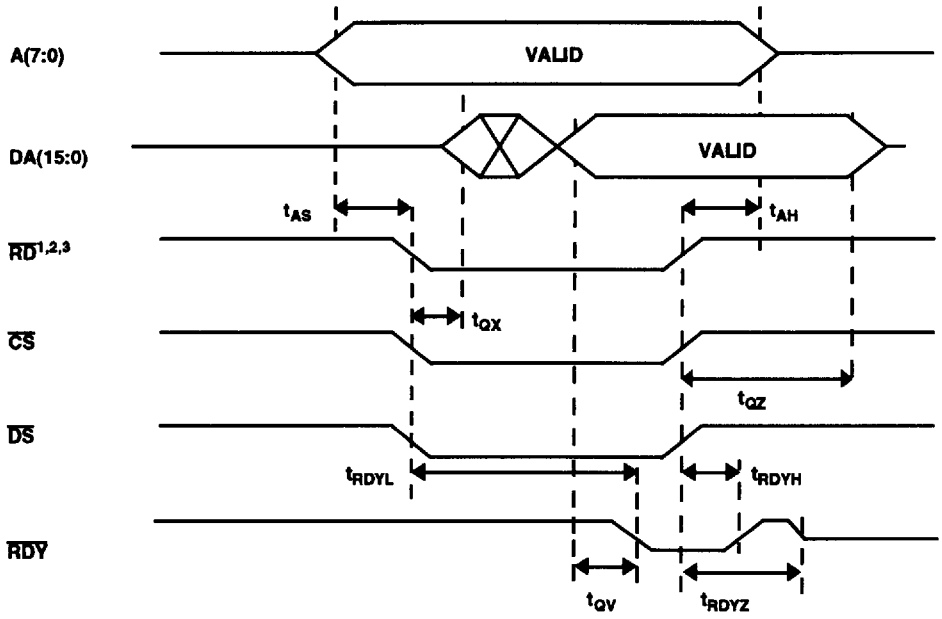
**Figure 10-5. Non-Multiplexed Memory/Register Read (8 Bit)**




| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0 | -- | ns |
| $t_{DS}$ | Data setup time | -- | 65 | ns |
| $t_{WP}$ | Write pulse width[3] | 120 | -- | ns |
| $t_{AH}$ | Address hold time | 0 | -- | ns |
| $t_{DH}$ | Data hold time | 0 | -- | ns |
| $t_{RDYL}$ | $\overline{RDY}$ low time | -- | 120 | ns |
| $t_{RDYH}$ | $\overline{RDY}$ high time | -- | 25 | ns |
| $t_{RDYZ}$ | $\overline{RDY}$ high Z | -- | 120 | ns |
| $t_{CYC}$ | Minimum cycle time | 0 | -- | ns |

**Notes:**
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$.
3. For applications not using $\overline{RDY}$ signal.

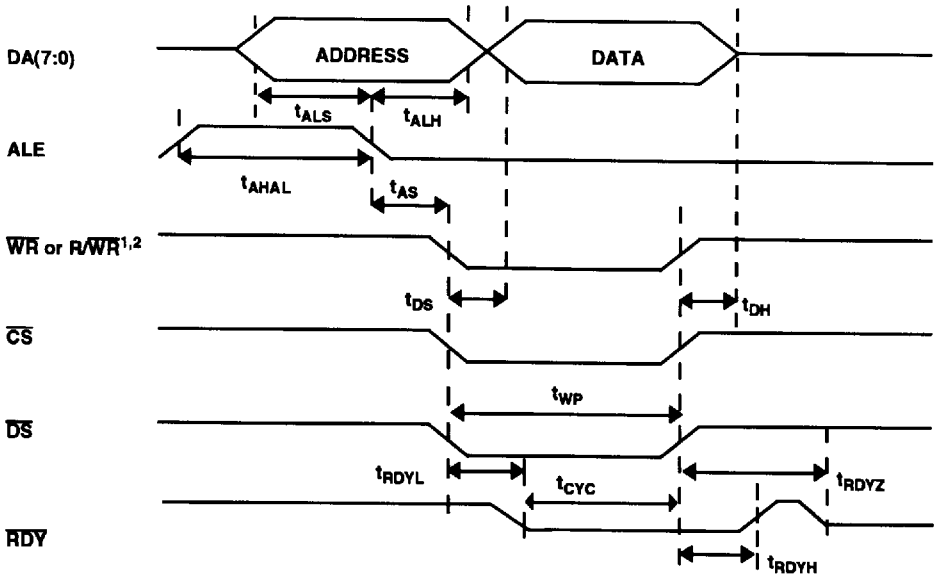
**Figure 10-6. Non-Multiplexed Memory/Register Write (16 Bit)**




| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0 | -- | ns |
| $t_{QX}$ | Data low Z | 0 | 35 | ns |
| $t_{AH}$ | Address hold time | 0 | -- | ns |
| $t_{QV}$ | Data valid to $\overline{RDY}$ low | 35 | -- | ns |
| $t_{QZ}$ | Data high Z | 0 | 25 | ns |
| $t_{RDYL}$ | $\overline{RDY}$ low time | -- | 350 | ns |
| $t_{RDYH}$ | $\overline{RDY}$ high time | -- | 25 | ns |
| $t_{RDYZ}$ | $\overline{RDY}$ high Z | -- | 120 | ns |

**Notes:**
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
3. When using R/$\overline{WR}$ as an input signal tie $\overline{RD}$ to a logical "1". During the read cycle R/$\overline{WR}$ remains a logical "1".

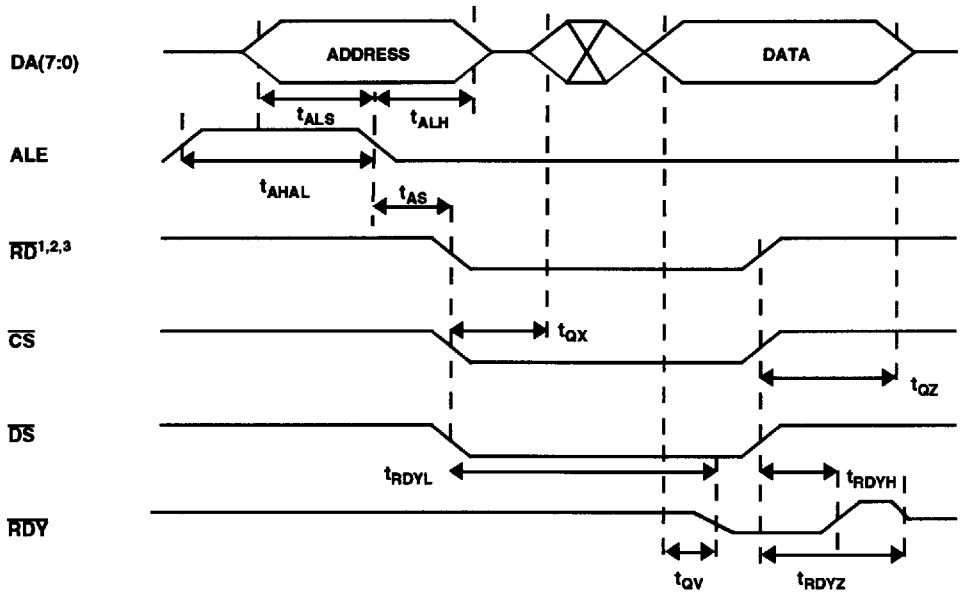
**Figure 10-7. Non-Multiplexed Memory/Register Read (16 Bit)**




| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{AHAL}$ | ALE pulse width | 35 | -- | ns |
| $t_{ALS}$ | Address latch setup time | 10 | -- | ns |
| $t_{ALH}$ | Address latch hold time | 10 | -- | ns |
| $t_{AS}$ | Address setup time | 0 | -- | ns |
| $t_{DS}$ | Data setup time | -- | 65 | ns |
| $t_{WP}$ | Write pulse width[3] | 120 | -- | ns |
| $t_{DH}$ | Data hold time | 0 | -- | ns |
| $t_{RDYL}$ | $\overline{RDY}$ low time | -- | 120 | ns |
| $t_{RDYH}$ | $\overline{RDY}$ high time | -- | 25 | ns |
| $t_{RDYZ}$ | $\overline{RDY}$ high Z | -- | 120 | ns |
| $t_{CYC}$ | Minimum cycle time | 0 | -- | ns |

**Notes:**
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$.
3. For applications not using $\overline{RDY}$ signal.

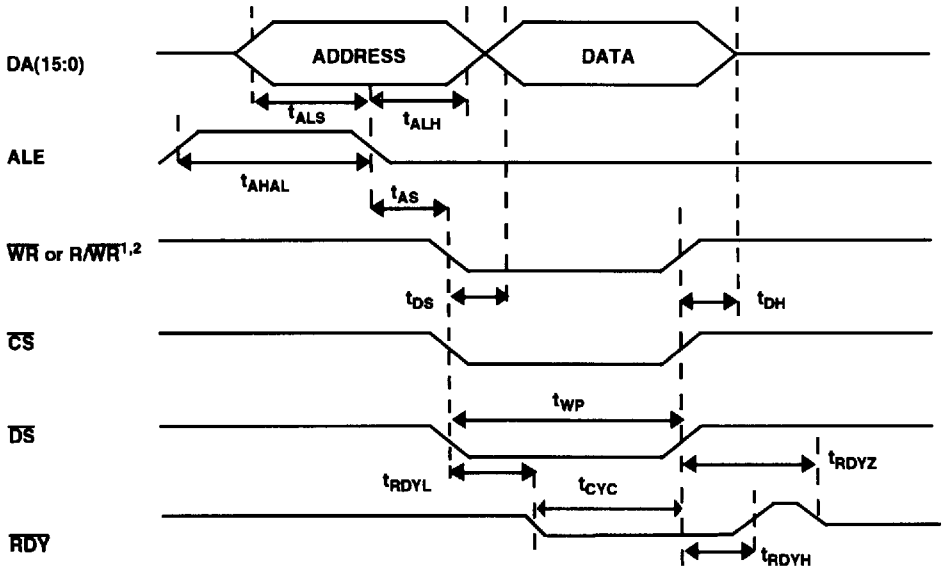
**Figure 10-8. Multiplexed Memory/Register Write (8 Bit)**




| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{AHAL}$ | ALE pulse width | 35 | -- | ns |
| $t_{ALS}$ | Address latch setup time | 10 | -- | ns |
| $t_{ALH}$ | Address latch hold time | 10 | -- | ns |
| $t_{AS}$ | Address setup time | 0 | -- | ns |
| $t_{QX}$ | Data low Z | 0 | 10 | ns |
| $t_{QV}$ | Data valid to $\overline{RDY}$ low | 35 | -- | ns |
| $t_{QZ}$ | Data high Z | 0 | 25 | ns |
| $t_{RDYL}$ | $\overline{RDY}$ low time | -- | 350 | ns |
| $t_{RDYH}$ | $\overline{RDY}$ high time | -- | 25 | ns |
| $t_{RDYZ}$ | $\overline{RDY}$ high Z | -- | 120 | ns |

**Notes:**
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
3. When using R/$\overline{WR}$ as an input signal tie $\overline{RD}$ to a logical "1". During the read cycle R/$\overline{WR}$ remains a logical "1".

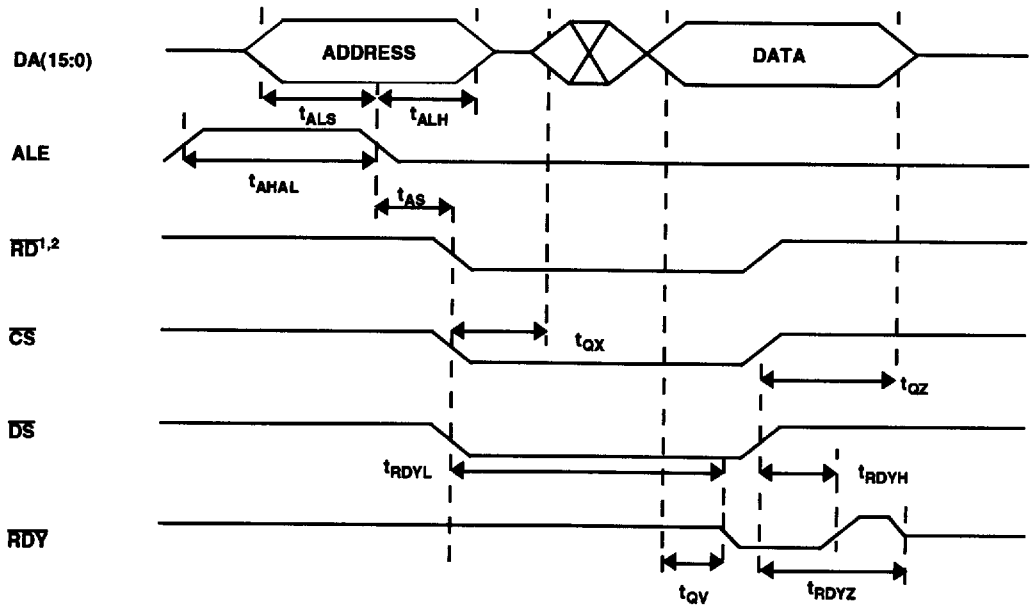
**Figure 10-9. Multiplexed Memory/Register Read (8 Bit)**




| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{AHAL}$ | ALE pulse width | 35 | -- | ns |
| $t_{ALS}$ | Address latch setup time | 10 | -- | ns |
| $t_{ALH}$ | Address latch hold time | 10 | -- | ns |
| $t_{AS}$ | Address setup time | 0 | -- | ns |
| $t_{DS}$ | Data setup time | -- | 65 | ns |
| $t_{WP}$ | Write pulse width[3] | 120 | -- | ns |
| $t_{DH}$ | Data hold time | 0 | -- | ns |
| $t_{RDYL}$ | $\overline{RDY}$ low time | -- | 120 | ns |
| $t_{RDYH}$ | $\overline{RDY}$ high time | -- | 25 | ns |
| $t_{RDYZ}$ | $\overline{RDY}$ high Z | -- | 120 | ns |
| $t_{CYC}$ | Minimum cycle time | 0 | -- | ns |

**Notes:**
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{WR}$ or R/$\overline{WR}$.
3. For applications not using $\overline{RDY}$ signal.

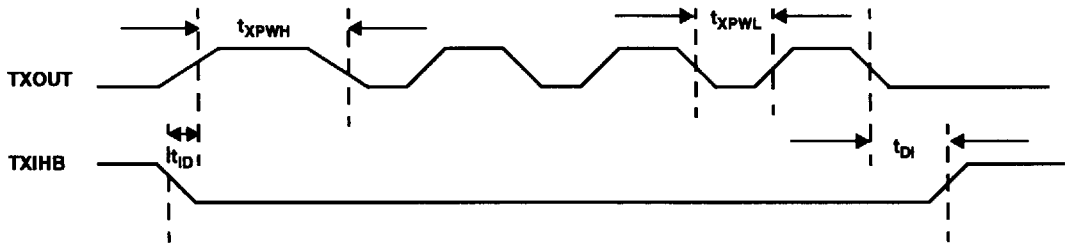
**Figure 10-10. Multiplexed Memory/Register Write (16 Bit)**




| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{AHAL}$ | ALE pulse width | 35 | -- | ns |
| $t_{ALS}$ | Address latch setup time | 10 | -- | ns |
| $t_{ALH}$ | Address latch hold time | 10 | -- | ns |
| $t_{AS}$ | Address setup time | 0 | -- | ns |
| $t_{QX}$ | Data low Z | 0 | 10 | ns |
| $t_{QV}$ | Data valid to $\overline{RDY}$ low | 35 | -- | ns |
| $t_{QZ}$ | Data high Z | 0 | 25 | ns |
| $t_{RDYL}$ | $\overline{RDY}$ low time | -- | 350 | ns |
| $t_{RDYH}$ | $\overline{RDY}$ high time | -- | 25 | ns |
| $t_{RDYZ}$ | $\overline{RDY}$ high Z | -- | 120 | ns |

**Notes:**
1. A cycle begins on the latter falling edge of $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$.
2. A cycle ends on the rising edge of either $\overline{CS}$, $\overline{DS}$ and $\overline{RD}$

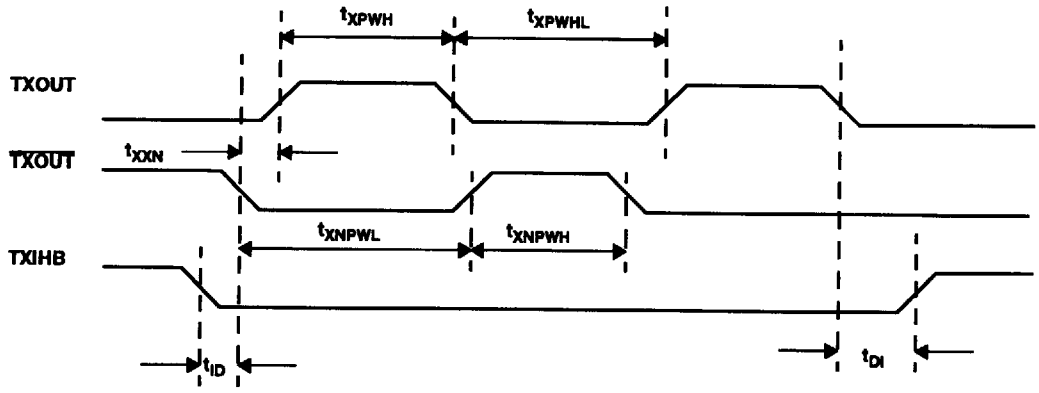
**Figure 10-11. Multiplexed Memory/Register Read (16 Bit)**




| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{XPWH}$ | TXOUT pulse width high | 21 | -- | ns |
| $t_{XPWL}$ | TXOUT pulse width low | 25 | -- | ns |
| $t_{ID}$ | TXIHB inactive to first data | 50 | 150 | ns |
| $t_{DI}$ | Last data to inhibit active[1] | 1005 | 1020 | ns |

**Notes:**
1. TXIM set to 0.

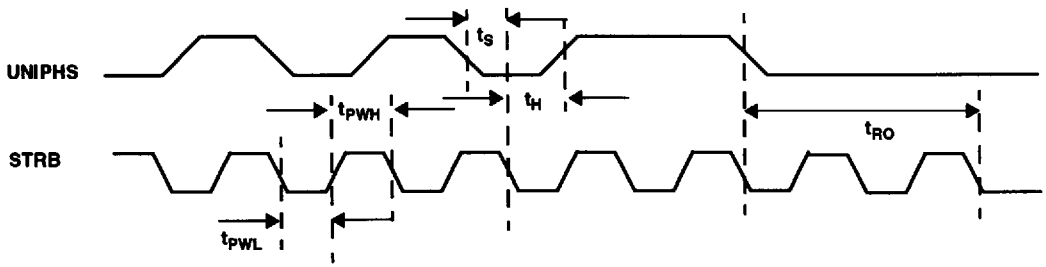
**Figure 10-12. 20Mbps Transmit Timing Diagram**




| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{XPWH}$ | TXOUT pulse with high | 492 | -- | ns |
| $t_{XPWHL}$ | TXOUT pulse width low | 498 | -- | ns |
| $t_{XXN}$ | Skew TXOUT to $\overline{TXOUT}$ | -2 | 10 | ns |
| $t_{XNPWH}$ | $\overline{TXOUT}$ pulse width high | 490 | -- | ns |
| $t_{XNPWL}$ | $\overline{TXOUT}$ pulse width low | 498 | -- | ns |
| $t_{ID}$ | Inhibit release to first data | 275 | 512 | ns |
| $t_{DI}$ | Last data to inhibit active[1] | 950 | 1050 | ns |

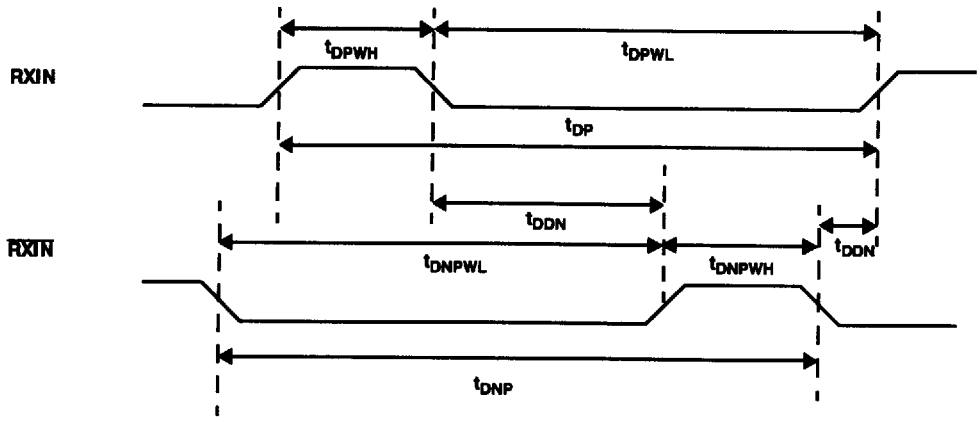
**Notes:**
1. TXIM set to 0.

**Figure 10-13. 1Mbps Transmit Timing Diagram**




| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_H$ | UNIPHS hold from STRB↓ | 5 | -- | ns |
| $t_S$ | UNIPHS setup to STRB ↓ | 5 | -- | ns |
| $t_{PWH}$ | STRB pulse width high | 5 | -- | ns |
| $t_{PWL}$ | STRB pulse width low | 5 | -- | ns |
| $t_{RO}$ | STRB run-on after data end | 33 | -- | clocks |

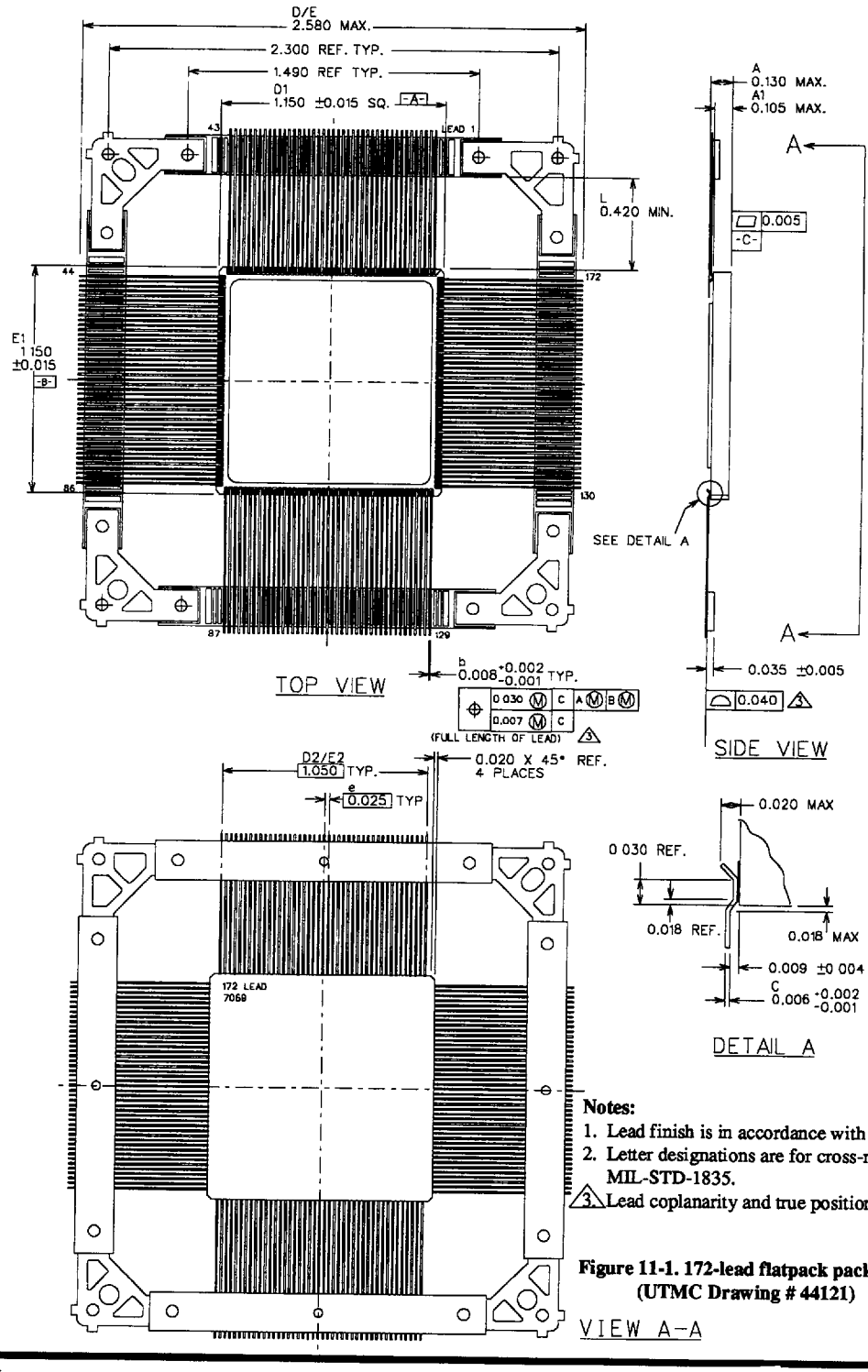
**Figure 10-14. 20Mbps Receive Timing Diagram**




| SYMBOL | PARAMETER | MINIMUM | MAXIMUM | UNITS |
|---|---|---|---|---|
| $t_{DPWH}$ | RXIN pulse width high | 75 | 650 | ns |
| $t_{DPWL}$ | RXIN pulse width low | 75 | 650 | ns |
| $t_{DNPWL}$ | $\overline{RXIN}$ pulse width low | 75 | 650 | ns |
| $t_{DNPWH}$ | $\overline{RXIN}$ pulse width high | 75 | 650 | ns |
| $t_{DP}$ | RXIN bit period | 998 | 1002 | ns |
| $t_{DDN}$ | RXIN to $\overline{RXIN}$ delay | 0 | 225 | ns |
| $t_{DNP}$ | $\overline{RXIN}$ bit period | 998 | 1002 | ns |

**Figure 10-15. 1 Mbps Receive Timing Diagram**

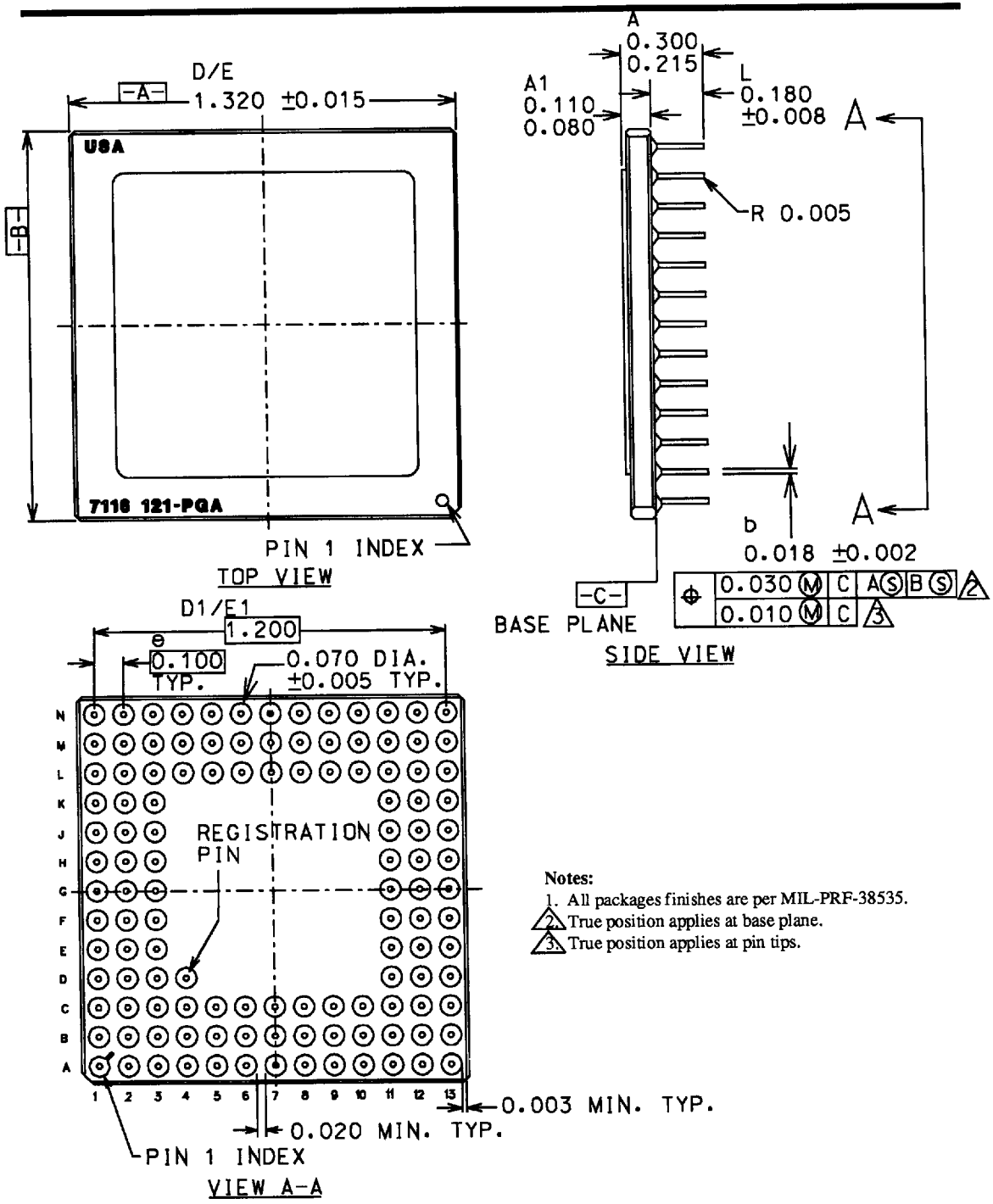
PAGE(S) INTENTIONALLY BLANK




**Notes:**

1. Lead finish is in accordance with MIL-PRF-38535.
2. Letter designations are for cross-reference to MIL-STD-1835.
3. Lead coplanarity and true position are not measured.

**Figure 11-1. 172-lead flatpack package (UTMC Drawing # 44121)**




**Notes:**

1. All packages finishes are per MIL-PRF-38535.
2. True position applies at base plane.
3. True position applies at pin tips.

**Figure 11-2. 121-pin pingrid array package (UTMC Drawing # 44128)**