



I C T INC

, INC.

T-46-19.07
Preliminary Information

PEEL™ 18CV8L-15

CMOS Programmable Electrically Erasable Logic Device

Features

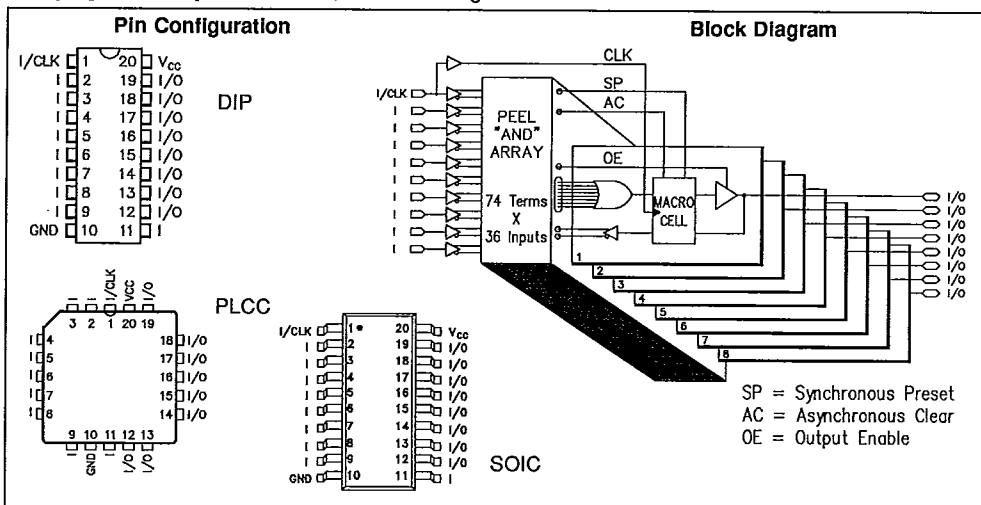
- **Industrial Grade Operation**
- **Low Power Consumption**
 - 32mA at 25MHz
- **High Performance**
 - $t_{PD}=15ns$, $f_{max}=41.6MHz$
- **EE Instant Reprogrammability**
 - 100% factory tested
 - Cost-effective windowless package
 - Erases and programs in seconds
 - Reduces retrofit and development costs
 - Provides low risk inventory
- **Foolproof Design Security**
 - Prevents unauthorized reading or copying of design
- **Architectural Flexibility**
 - 74 product term x 36 input array
 - Up to 18 inputs and 8 I/O pins
 - Independently programmable 12-configuration I/O macro cells
 - Synchronous preset, asynchronous clear
 - Independent output enables
- **Application Versatility**
 - Replaces SSI/MSI logic
 - Emulates PAL*, GAL* and EPLDs
 - Simplifies inventory control
 - Allows new design possibilities
- **Development/Programmer Support**
 - Third party software and programmers
 - ICT PEEL Development System and Software

3

General Description

The ICT PEEL18CV8L-15 is a CMOS Programmable Electrically Erasable Logic device that provides a high-performance, low-power, reprogrammable, and architecturally flexible alternative to early-generation programmable logic devices (PLDs). Designed in advanced CMOS EEPROM technology, the performance of the PEEL18CV8L rivals speed parameters of bipolar PLDs with a dramatic reduction in power consumption. EE reprogrammability simplifies inventory management, reduces development and field retrofit costs, enhances testability to ensure 100% field programmability and function, while allowing

for low-cost "windowless" packaging in a 20-pin, 300-mil DIP. The PEEL18CV8L's flexible architecture allows the device to replace SSI/MSI logic circuitry. ICT's JEDEC file translator allows the PEEL18CV8L to replace existing 20-pin PLDs without the need to rework the existing design. Development software and programming support for the PEEL18CV8L is provided by ICT and third-party manufacturers. The PEEL18CV8L-15 is function and programming compatible with the standard PEEL18CV8L.





INC.

ICT INC

PEEL™ 18CV8L-15

T-46-19-07

Exposure to absolute maximum ratings over extended periods of time may affect device reliability. Exceeding absolute maximum ratings may cause permanent damage

Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Supply Voltage	Relative to GND	-0.5 to +7.0	V
V _I , V _O	Voltage Applied to Any Pin ³	Relative to GND ¹	-0.5 to V _{CC} + 0.6	V
I _O	Output Current	Per pin (I _{OL} , I _{OH})	±25	mA
T _{ST}	Storage Temperature		-65 to +150	°C
T _{LT}	Lead Temperature	Soldering 10 seconds	+300	°C

Operating Ranges²

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	Supply Voltage	Commercial	4.75	5.25	V
		Industrial	4.5	5.5	V
T _A	Ambient Temperature	Commercial	0	+70	°C
		Industrial	-40	+85	°C
T _R	Clock Rise Time	See note 4		250	ns
T _F	Clock Fall Time	See note 4		250	ns
T _{RVCC}	V _{CC} Rise Time	See note 4		250	ms

D.C. Electrical Characteristics

Over the operating range

Symbol	Parameter	Conditions	Min	Max	Unit
V _{OH}	Output HIGH Voltage - TTL	V _{CC} = Min, I _{OH} = -4.0mA	2.4		V
V _{OHc}	Output HIGH Voltage-CMOS	V _{CC} = Min, I _{OH} = -10μA	V _{CC} - 0.1		V
V _{OL}	Output LOW Voltage - TTL	V _{CC} = Min, I _{OL} = 16mA		0.45	V
V _{OLc}	Output LOW Voltage-CMOS	V _{CC} = Min, I _{OL} = 10μA		0.1	V
V _{IH}	Input HIGH Level		2.0	V _{CC} + 0.3	V
V _{IL}	Input LOW Level		-0.3	0.8	V
I _{IL}	Input Leakage Current	V _{CC} = Max, GND ≤ V _{IN} ≤ V _{CC}		±10	μA
I _{OZ}	Output Leakage Current	V _O = High-Z, GND ≤ V _O ≤ V _{CC}		±10	μA
I _{SC}	Output Short Circuit Current	V _{CC} = 5V, V _O = 0.5V ⁹ , T _A = 25°C	-30	-100	mA
I _{CC}	V _{CC} Current	V _{IN} = 0V or 3V ^{5,11} f = 25MHz All outputs disabled.		32	mA
C _{IN} ⁷	Input Capacitance	T _A = 25°C, V _{CC} = 5.0V @ f = 1MHz		6	pF
C _{OUT} ⁷	Output Capacitance			12	pF



, INC.

I C T INC

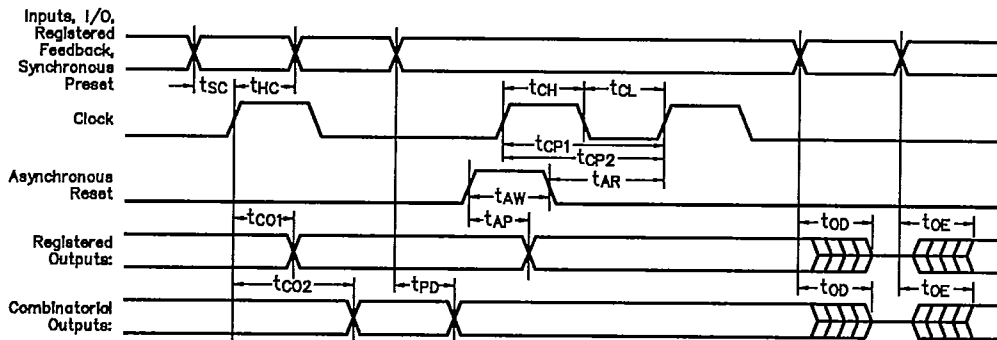
PEEL™ 18CV8L-15

A.C. Electrical Characteristics Over the Operating Range^{9,12}

T-46-19-07

Symbol	Parameter	18CV8L-15		Unit
		Min	Max	
t _{PD}	Input ⁶ or feedback to non-registered output		15	nS
t _{OE}	Input ⁶ to output enable ⁷		15	nS
t _{OD}	Input ⁶ to output disable ⁷		15	nS
t _{CO1}	Clock to output		12	nS
t _{CO2}	Clock to combinatorial output delay via internal registered feedback		25	nS
t _{SC}	Input ⁶ or feedback setup to clock	12		nS
t _{HC}	Input ⁶ hold after clock	0		nS
t _{CL,tCH}	Clock width - clk low time, clk high time ⁴	10		nS
t _{CP1}	Minimum clock period (register feedback to registered output via internal path)	20		nS
f _{max1}	Maximum clock frequency (1/t _{CP1})	50		MHz
t _{CP2}	Minimum clock period (t _{SC} + t _{CO1})	24		nS
f _{max2}	Maximum clock frequency (1/t _{CP2})	41.6		MHz
t _{AW}	Asynchronous clear pulse width	15		nS
t _{AP}	Input ⁶ to asynchronous clear		20	nS
t _{AR}	Asynchronous Reset Recovery Time		10	nS
t _{RESET}	Power-on reset time for registers in clear state ⁴		5	μS

Switching Waveforms



- Minimum DC input is -0.5V, however inputs may undershoot to -2.0V for periods less than 20ns
- Contact ICT for other operating ranges.
- V_I and V_O are not specified for program/verify operation.
- Test points for Clock and V_{CC} in t_h, t_f, t_{CL}, t_{CH}, and t_{RESET} are referenced at 10% and 90% levels.
- I/O pins are 0V or 3V.
- "Input" refers to input pin signal.
- t_{OE} is measured from input transition to V_{REF} ± 0.1V, t_{OD} is measured from input transition to V_{OH}-0.1V or V_{OL}+0.1V; V_{REF} = V_L see test loads at the end of this section.
- Capacitance are tested on a sample basis.
- Test conditions assume: signal transition times of 5ns or less from the 10% and 90% points, timing reference levels of 1.5V (unless otherwise specified).
- Test one output at a time for a duration less than 1 second.
- ICC for a typical application: This parameter is tested with the device programmed as an 8-bit counter.
- PEEL Device test loads are specified at the end of this section