Dual Channel Medium Power Differential Line Driver

The EL1527 is a very low power dual channel differentiated amplifier designed for central office and customer premise line driving for DMT ADSL solutions. This device features a high drive capability of 400mA while consuming only 7.5mA of supply current per amplifier from ±12V supplies. This driver achieves a typical distortion of less than -75dBc, at 1MHz into a 50Ω load.

The EL1527 has two control pins, C_0 and C_1, per channel. With the selection of C_0 and C_1, the device can be set into full-I_S power, 3/4-I_S power, 1/2-I_S power, and power-down disable modes. The EL1527 maintains excellent distortion and load driving capabilities even in the lowest power settings.

The EL1527 is available in the thermally-enhanced 28-pin HTSSOP package. This device is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	OUTLINE #
EL1527CRE	28-Pin HTSSOP	-	MDP0048
EL1527CRE-T7	28-Pin HTSSOP	7”	MDP0048
EL1527CRE-T13	28-Pin HTSSOP	13”	MDP0048

Features

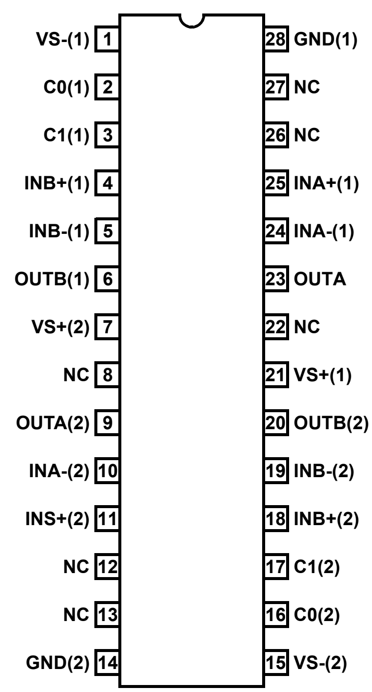
- Drives 360mA at $16V_{P-P}$ on ±12V supplies
- $40V_{P-P}$ differential output drive into 100Ω
- -75dBc typical driver output distortion driving 50Ω at 1MHz and 1/2-I_S bias current
- Low quiescent current of 3.5mA per amplifier in 1/2-I_S mode
- Power-down disable mode

Applications

- ADSL G.DMT and G.lite CO line driving
- G.SHDSL, HDSL2 line driver
- ADSL CPE line driving
- Video distribution amplifier
- Video twisted-pair line driver

Pinout

EL1527
(28-PIN HTSSOP)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

V_S+ to V_S- Supply Voltage 26.4V
V_S+ Voltage to Ground . . . . -0.3V to +26.4V
V_S- Voltage to Ground . . . . -26.4V to 0.3V
Input C_0/C_1 to Ground 7V
V_{IN}+ Voltage . . . . V_S- to V_S+
Current into any Input 8mA

Continuous Output Current 75mA
Operating Temperature Range . . . .-40°C to +85°C
Storage Temperature Range . . . .-60°C to +150°C
Operating Junction Temperature . . . .-40°C to +150°C
Power Dissipation . . . . . .See Power Supplies & Dissipation section

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = ±12V, R_F = 1.5kΩ, R_L = 75Ω to GND, T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth	A_V = +4		70		MHz
HD	Total Harmonic Distortion	f = 1MHz, V_O = 16V_{P-P}, R_L = 50Ω		-75		dBc
dG	Differential Gain	A_V = +2, R_L = 37.5Ω		0.17		%
dθ	Differential Phase	A_V = +2, R_L = 37.5Ω		0.1		°
SR	Slewrate	V_{OUT} from -4.5V to +4.5V	350	500		V/µs
DC PERFORMANCE						
V_{OS}	Offset Voltage		-17		17	mV
ΔV_{OS}	V_{OS} Mismatch		-10		10	mV
R_{OL}	Transimpedance	V_{OUT} from -4.5V to +4.5V	1	2	3.5	MΩ
INPUT CHARACTERISTICS						
I_B+	Non-Inverting Input Bias Current		-5		5	µA
I_B-	Inverting Input Bias Current		-30		30	µA
ΔI_B-	I_B- Mismatch		-20		20	µA
e_N	Input Noise Voltage			2.8		nV/√Hz
i_N+	+Input Noise Current			1.8		pA/√Hz
i_N-	-Input Noise Current			19		pA/√Hz
V_{IH}	Input High Voltage	C_0 & C_1 Inputs	2.3			V
V_{IL}	Input Low Voltage	C_0 & C_1 Inputs			1.5	V
I_{IH1}	Input High Current for C_1	C_1 = 5V	0.2		8	µA
I_{IH0}	Input High Current for C_0	C_0 = 5V	0.1		4	µA
I_{IL}	Input Low Current for C_1or C_0	C_1 = 0V, C_0 = 0V	-1		1	µA
OUTPUT CHARACTERISTICS						
V_{OUT}	Loaded Output Swing Single Ended	R_L = 100Ω to GND	±10.3	±10.9		V
V_{OUT} P	Loaded Output Swing Single Ended	R_L = 25Ω to GND	9.5	10.2		V
V_{OUT} N	Loaded Output Swing Single Ended	R_L = 25Ω to GND	-9.0	-9.8		V
I_{OUT}	Output Current	R_L = 0Ω		500		mA
SUPPLY						
V_S	Supply Voltage	Single Supply	5		24	V
I_S+ (Full Power)	Positive Supply Current per Amplifier	All Outputs at 0V, C_0 = C_1 = 0V		7.5	9	mA
I_S- (Full Power)	Negative Supply Current per Amplifier	All Outputs at 0V, C_0 = C_1 = 0V		-7	-8.5	mA

Electrical Specifications

V_S = ±12V, R_F = 1.5kΩ, R_L = 75Ω to GND, T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
I_S+ (3/4 Power)	Positive Supply Current per Amplifier	All Outputs at 0V, C_0 = 5V, C_1 = 0V		6	7.5	mA
I_S- (3/4 Power)	Negative Supply Current per Amplifier	All Outputs at 0V, C_0 = 5V, C_1 = 0V		-5.5	-7	mA
I_S+ (1/2 Power)	Positive Supply Current per Amplifier	All Outputs at 0V, C_0 = 0V, C_1 = 5V		3.9	5.1	mA
I_S- (1/2 Power)	Negative Supply Current per Amplifier	All Outputs at 0V, C_0 = 0V, C_1 = 5V		-3.3	-4.6	mA
I_S+ (Power Down)	Positive Supply Current per Amplifier	All Outputs at 0V, C_0 = C_1 = 5V		0.6	1	mA
I_S- (Power Down)	Negative Supply Current per Amplifier	All Outputs at 0V, C_0 = C_1 = 5V		0	0.75	mA
I_{GND}	GND Supply Current per Amplifier	All Outputs at 0V		0.6	1	mA

Typical Performance Curves

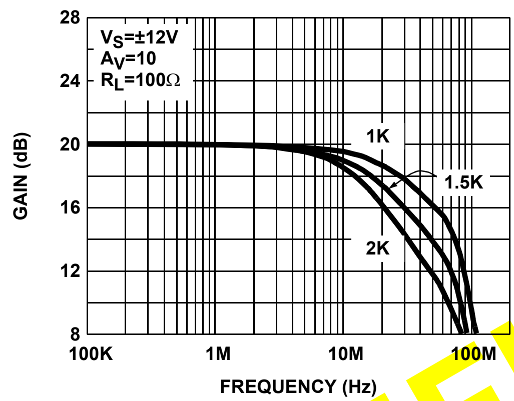


FIGURE 1. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (FULL POWER MODE)

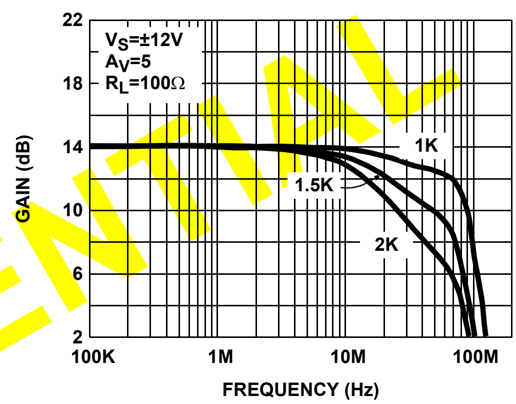


FIGURE 2. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (FULL POWER MODE)

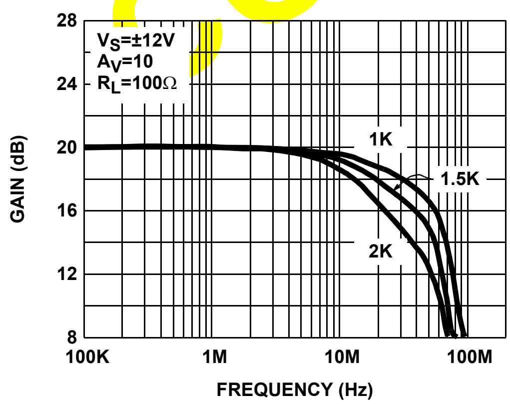


FIGURE 3. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (3/4-POWER MODE)

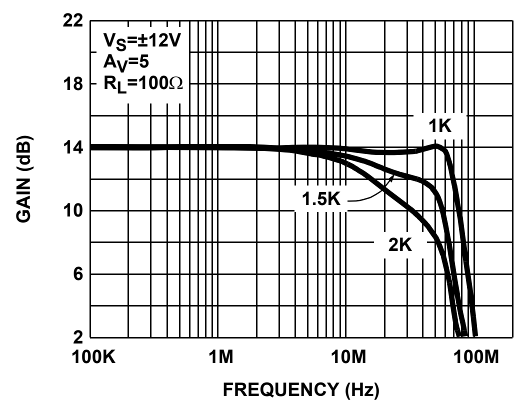


FIGURE 4. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (3/4-POWER MODE)

Typical Performance Curves

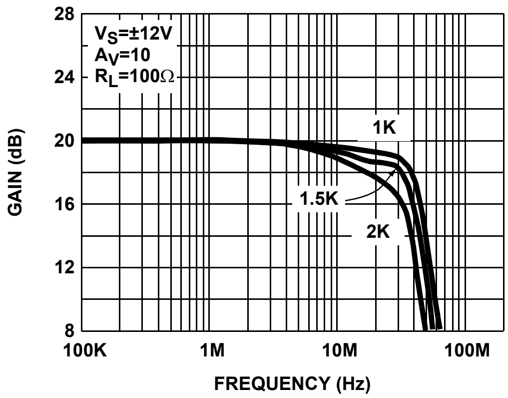


FIGURE 5. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (1/2-POWER MODE)

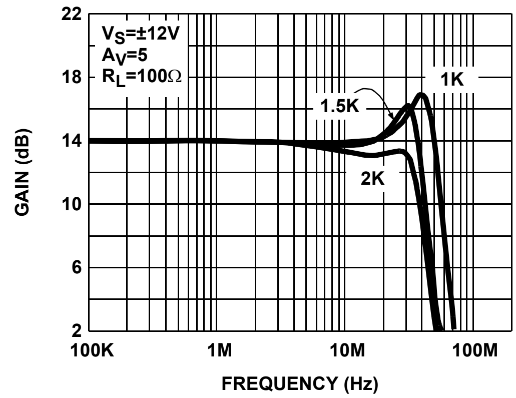


FIGURE 6. DIFFERENTIAL FREQUENCY RESPONSE vs R_F (1/2-POWER MODE)

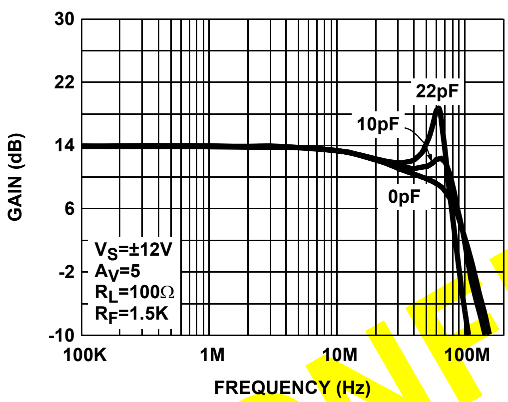


FIGURE 7. DIFFERENTIAL RESPONSE vs C_{LOAD} (FULL POWER MODE)

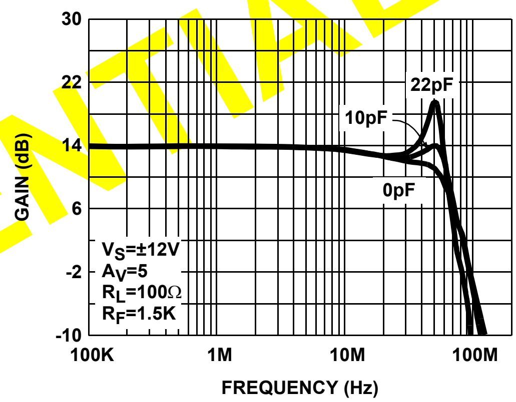


FIGURE 8. DIFFERENTIAL RESPONSE vs C_{LOAD} (3/4-POWER MODE)

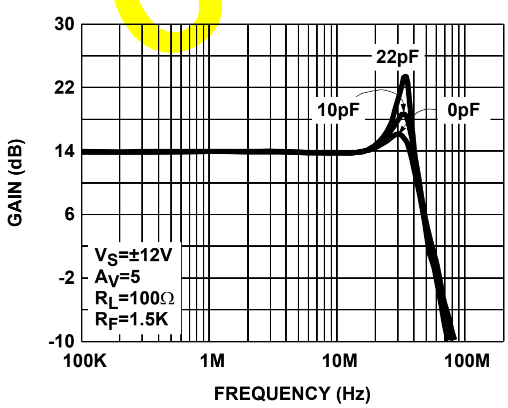


FIGURE 9. DIFFERENTIAL RESPONSE vs C_{LOAD} (1/2-POWER MODE)

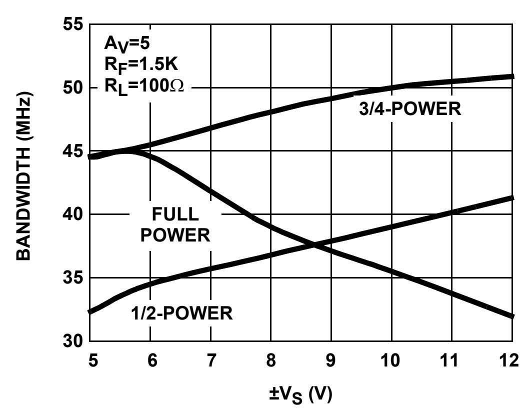


FIGURE 10. DIFFERENTIAL BANDWIDTH vs SUPPLY VOLTAGE

Typical Performance Curves

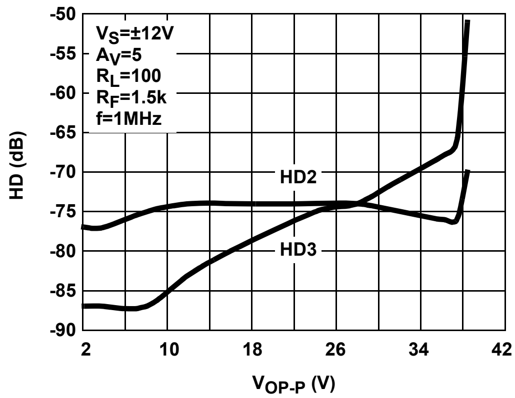


FIGURE 11. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (FULL POWER MODE)

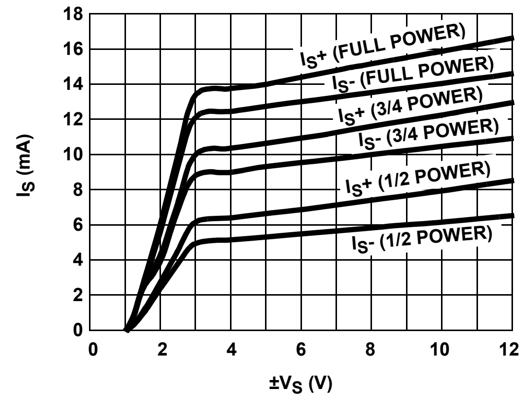


FIGURE 12. SUPPLY CURRENT VS SUPPLY VOLTAGE

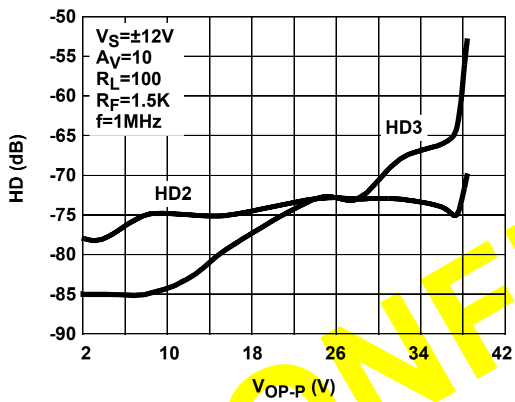


FIGURE 13. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (3/4-POWER MODE)

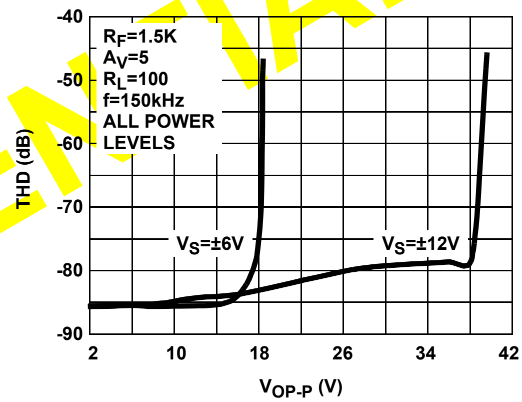


FIGURE 14. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE

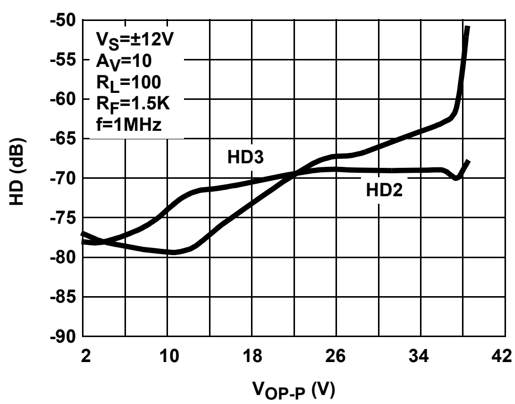


FIGURE 15. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (1/2-POWER MODE)

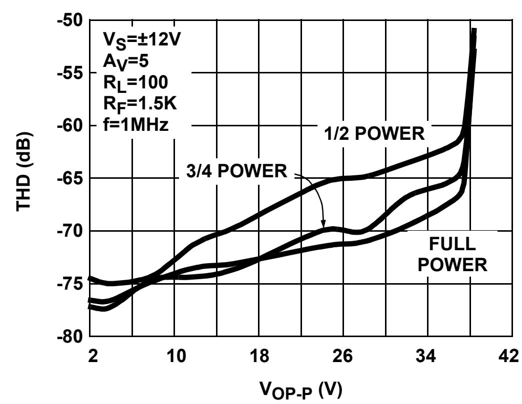


FIGURE 16. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE

Typical Performance Curves

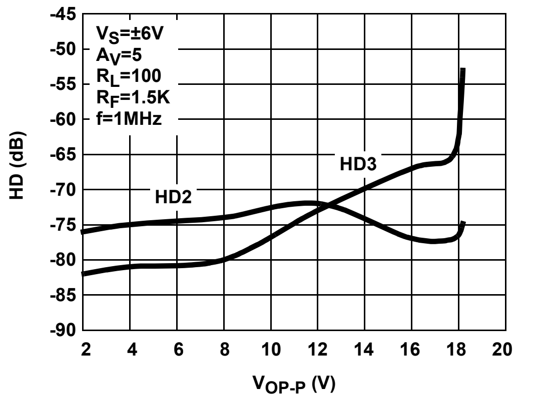


FIGURE 17. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (3/4-POWER MODE)

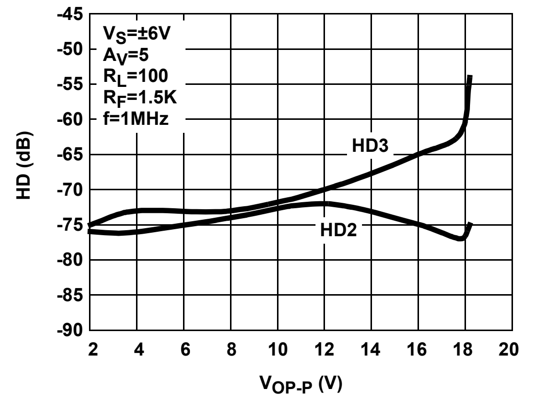


FIGURE 18. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (1/2-POWER MODE)

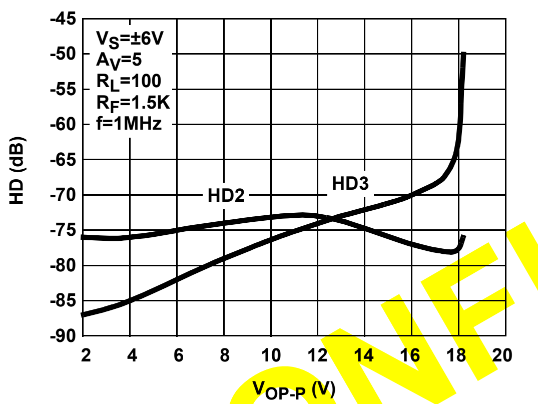


FIGURE 19. DIFFERENTIAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE (FULL POWER MODE)

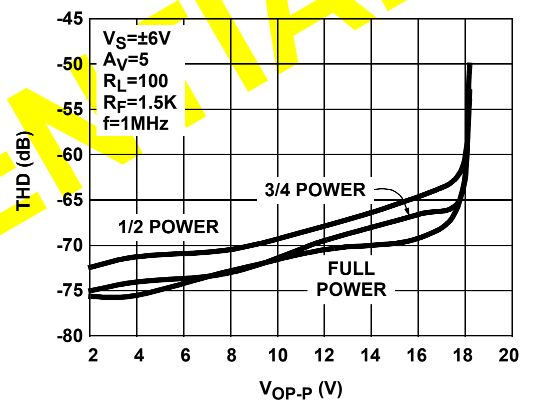


FIGURE 20. DIFFERENTIAL TOTAL HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT AMPLITUDE

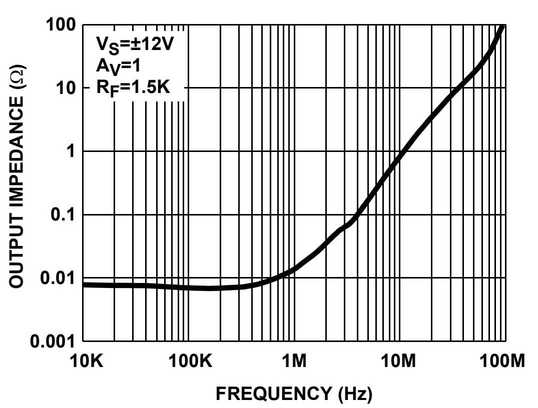


FIGURE 21. OUTPUT IMPEDANCE vs FREQUENCY (ALL POWER LEVELS)

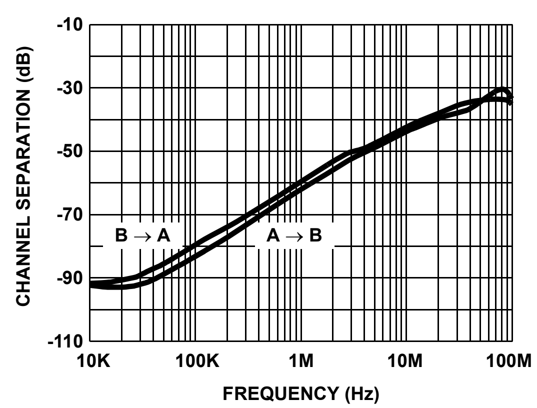


FIGURE 22. CHANNEL SEPARATION VS FREQUENCY (ALL POWER LEVELS)

Typical Performance Curves

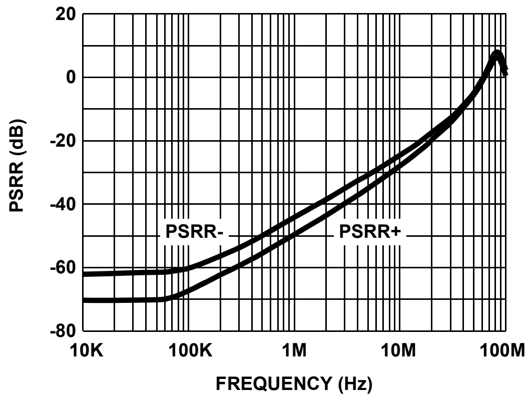


FIGURE 23. PSRR vs FREQUENCY

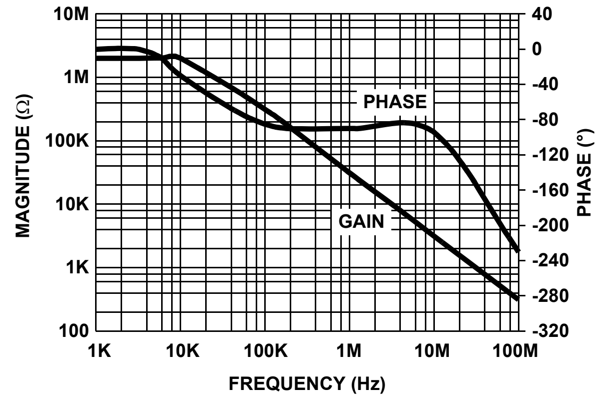


FIGURE 24. TRANSIMPEDANCE (ROL) vs FREQUENCY

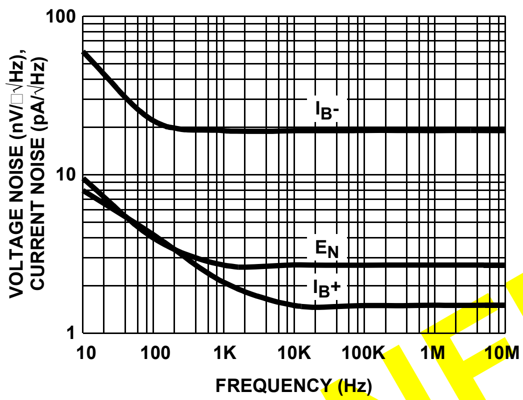


FIGURE 25. VOLTAGE AND CURRENT NOISE vs FREQUENCY

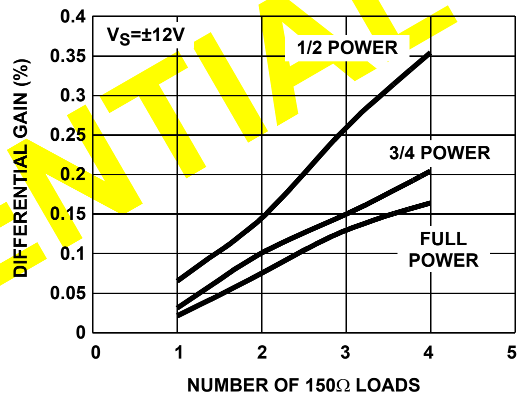


FIGURE 26. DIFFERENTIAL GAIN

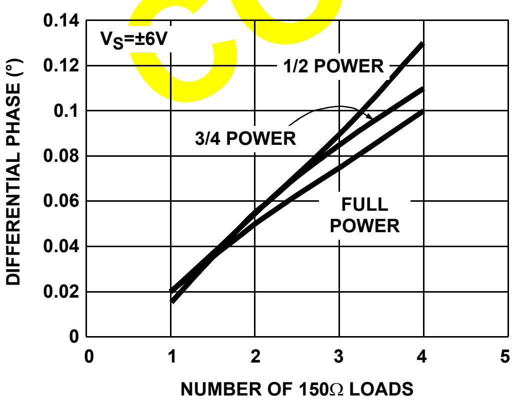


FIGURE 27. DIFFERENTIAL PHASE

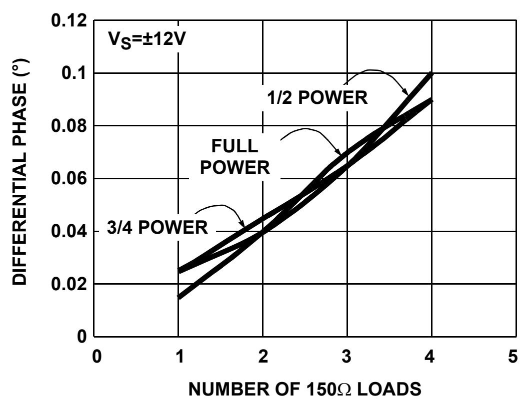


FIGURE 28. DIFFERENTIAL PHASE

Typical Performance Curves

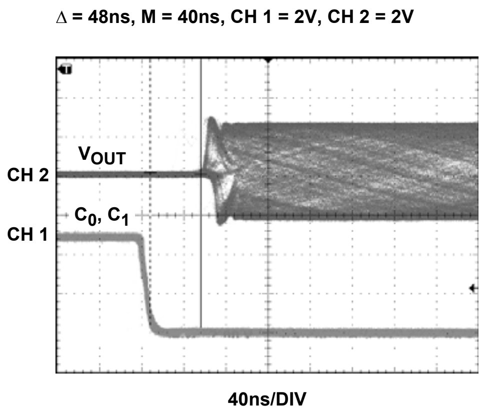


FIGURE 29. ENABLE RESPONSE

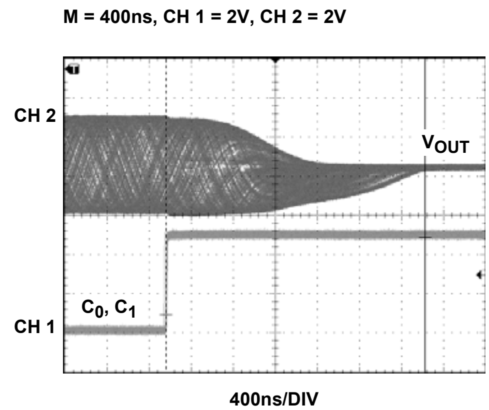


FIGURE 30. DISABLE RESPONSE

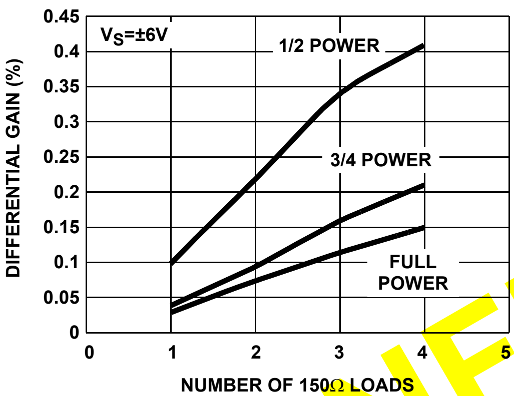


FIGURE 31. DIFFERENTIAL GAIN

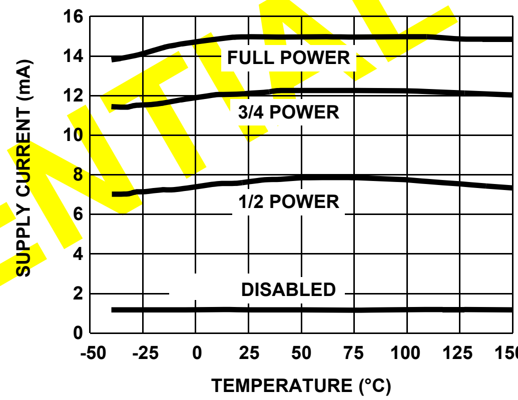


FIGURE 32. POSITIVE SUPPLY CURRENT vs TEMPERATURE

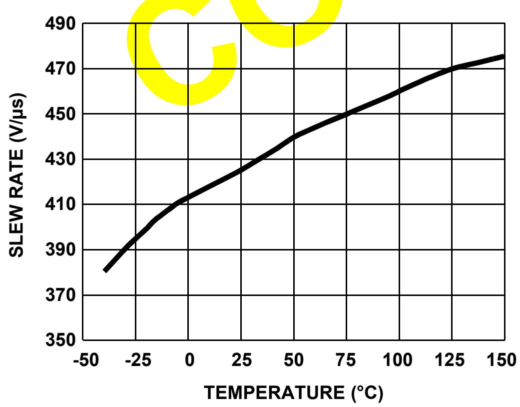


FIGURE 33. SLEW RATE vs TEMPERATURE

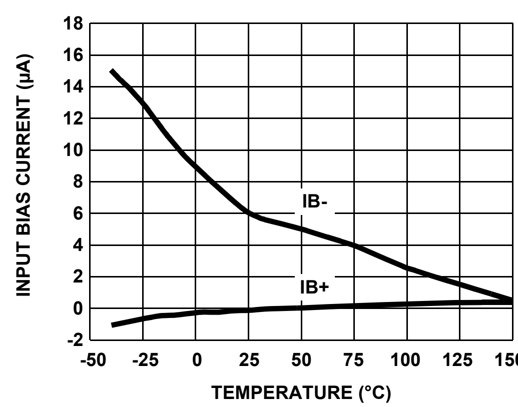


FIGURE 34. INPUT BIAS CURRENT vs TEMPERATURE

Typical Performance Curves

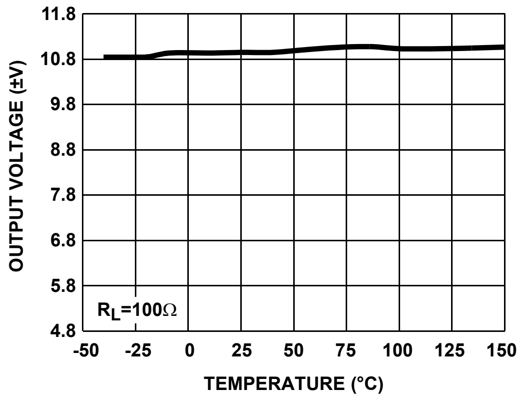


FIGURE 35. OUTPUT VOLTAGE vs TEMPERATURE

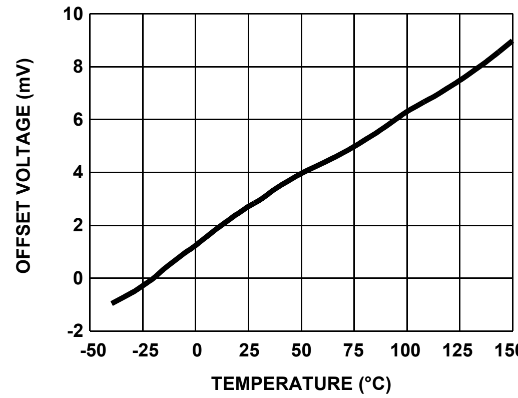


FIGURE 36. OFFSET VOLTAGE vs TEMPERATURE

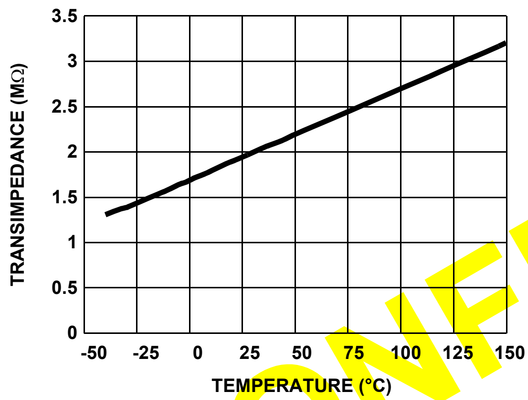


FIGURE 37. TRANSIMPEDANCE vs TEMPERATURE

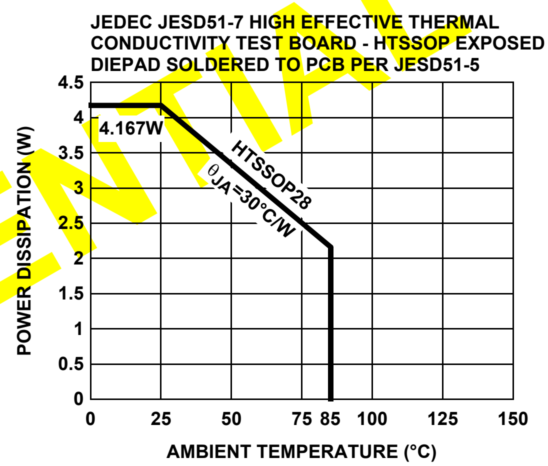


FIGURE 38. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

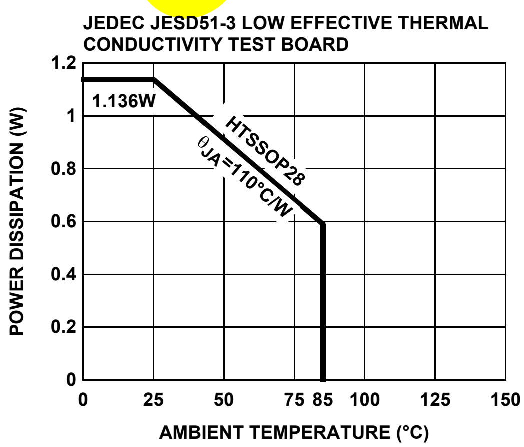


FIGURE 39. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

The EL1527 consists of two sets of high-power line driver amplifiers that can be connected for full duplex differential line transmission. The amplifiers are designed to be used with signals up to 4MHz and produce low distortion levels. A typical interface circuit is shown in Figure 40 below.

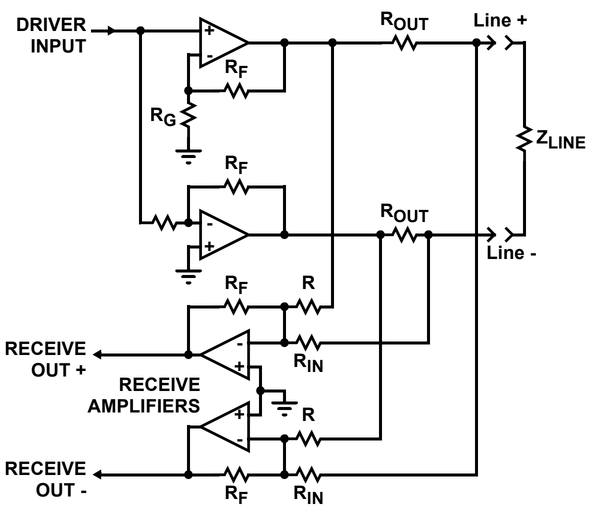


FIGURE 40. TYPICAL LINE INTERFACE CONNECTION

The amplifiers are wired with one in positive gain and the other in a negative gain configuration to generate a differential output for a single-ended input. They will exhibit very similar frequency responses for gains of three or greater and thus generate very small common-mode outputs over frequency, but for low gains the two drivers RF's need to be adjusted to give similar frequency responses. The positive-gain driver will generally exhibit more bandwidth and peaking than the negative-gain driver.

If a differential signal is available to the drive amplifiers, they may be wired so:

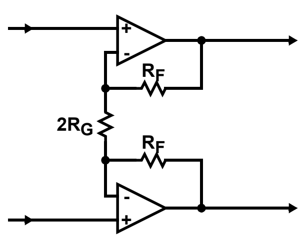


FIGURE 41. DRIVERS WIRED FOR DIFFERENTIAL INPUT

Each amplifier has identical positive gain connections, and optimum common-mode rejection occurs. Further, DC input errors are duplicated and create common-mode rather than differential line errors.

Input Connections

The EL1527 amplifiers are somewhat sensitive to source impedance. In particular, they do not like being driven by inductive sources. More than 100nH of source impedance can cause ringing or even oscillations. This inductance is equivalent to about 4" of unshielded wiring, or 6" of unterminated transmission line. Normal high-frequency construction obviates any such problem.

Power Supplies & Dissipation

Due to the high power drive capability of the EL1527, much attention needs to be paid to power dissipation. The power that needs to be dissipated in the EL1527 has two main contributors. The first is the quiescent current dissipation. The second is the dissipation of the output stage.

The quiescent power in the EL1527 is not constant with varying outputs. In reality, 7mA of the 15mA needed to power the drivers is converted in to output current. Therefore, in the equation below we should subtract the average output current, I_O, or 7mA, whichever is the lowest. We'll call this term I_X.

Therefore, we can determine a quiescent current with the equation:

$$P_{Dquiescent} = V_S \times (I_S - 2I_X)$$

where:

- V_S is the supply voltage (V_S+ to V_S-)
- I_S is the maximum quiescent supply current (I_S+ + I_S-)
- IX is the lesser of I_O or 7mA (generally I_X = 7mA)

The dissipation in the output stage has two main contributors. Firstly, we have the average voltage drop across the output transistor and secondly, the average output current. For minimal power dissipation, the user should select the supply voltage and the line transformer ratio accordingly. The supply voltage should be kept as low as possible, while the transformer ratio should be selected so that the peak voltage required from the EL1527 is close to the maximum available output swing. There is a trade off, however, with the selection of transformer ratio. As the ratio is increased, the receive signal available to the receivers is reduced.

Once the user has selected the transformer ratio, the dissipation in the output stages can be selected with the following equation:

$$P_{Dtransistors} = 2 \times \overline{I_O} \times \left(\frac{V_S}{2} - \overline{V_O}\right)$$

where:

- V_S is the supply voltage (V_S+ to V_S-)
- V_O is the average output voltage per channel
- I_O is the average output current per channel

The overall power dissipation (P_{DISS}) is obtained by adding $P_{Dquiescent}$ and $P_{Dtransistor}$.

Then, the θ_{JA} requirement needs to be calculated. This is done using the equation:

$$\theta_{JA} = \frac{(T_{JUNCT} - T_{AMB})}{P_{DISS}}$$

where:

- T_{JUNCT} is the maximum die temperature (150°C)
- T_{AMB} is the maximum ambient temperature
- P_{DISS} is the dissipation calculated above
- θ_{JA} is the junction to ambient thermal resistance for the package when mounted on the PCB

This θ_{JA} value is then used to calculate the area of copper needed on the board to dissipate the power.

The CRE power packages are designed so that heat may be conducted away from the device in an efficient manner. To disperse this heat, the bottom diepad is internally connected to the mounting platform of the die. Heat flows through the diepad into the circuit board copper, then spreads and convects to air. Thus, the ground plane on the component side of the board becomes the heatsink. This has proven to be a very effective technique. θ_{JA} of 30°C/W can be achieved.

Single Supply Operation

The EL1527 can also be powered from a single supply voltage. When operating in this mode, the GND pins can still be connected directly to GND. To calculate power dissipation, the equations in the previous section should be used, with V_S equal to half the supply rail.

Output Loading

While the drive amplifiers can output in excess of 400mA transiently, the internal metallization is not designed to carry more than 75mA of steady DC current and there is no current-limit mechanism. This allows safely driving rms sinusoidal currents of 2 x 75mA, or 150mA. This current is more than that required to drive line impedances to large output levels, but output short circuits cannot be tolerated. The series output resistor will usually limit currents to safe values in the event of line shorts. Driving lines with no series resistor is a serious hazard.

The amplifiers are sensitive to capacitive loading. More than 25pF will cause peaking of the frequency response. The same is true of badly terminated lines connected without a series matching resistor.

Power Supplies

The power supplies should be well bypassed close to the EL1527. A 3.3µF tantalum capacitor for each supply works well. Since the load currents are differential, they should not travel through the board copper and set up ground loops that can return to amplifier inputs. Due to the class AB output stage design, these currents have heavy harmonic content. If the ground terminal of the positive and negative bypass capacitors are connected to each other directly and then returned to circuit ground, no such ground loops will occur. This scheme is employed in the layout of the EL1527 demonstration board, and documentation can be obtained from the factory.

Feedback Resistor Value

The bandwidth and peaking of the amplifiers varies with supply voltage somewhat and with gain settings. The feedback resistor values can be adjusted to produce an optimal frequency response. Here is a series of resistor values that produce an optimal driver frequency response (<1dB peaking) for different supply voltages and gains:

OPTIMUM DRIVER FEEDBACK RESISTOR FOR VARIOUS GAINS AND SUPPLY VOLTAGES

SUPPLY VOLTAGE	DRIVER VOLTAGE GAIN		
	2.5	**5**	**10**
±5V	2K	1.8K	1.5K
±12V	2K	1.8K	1.5K

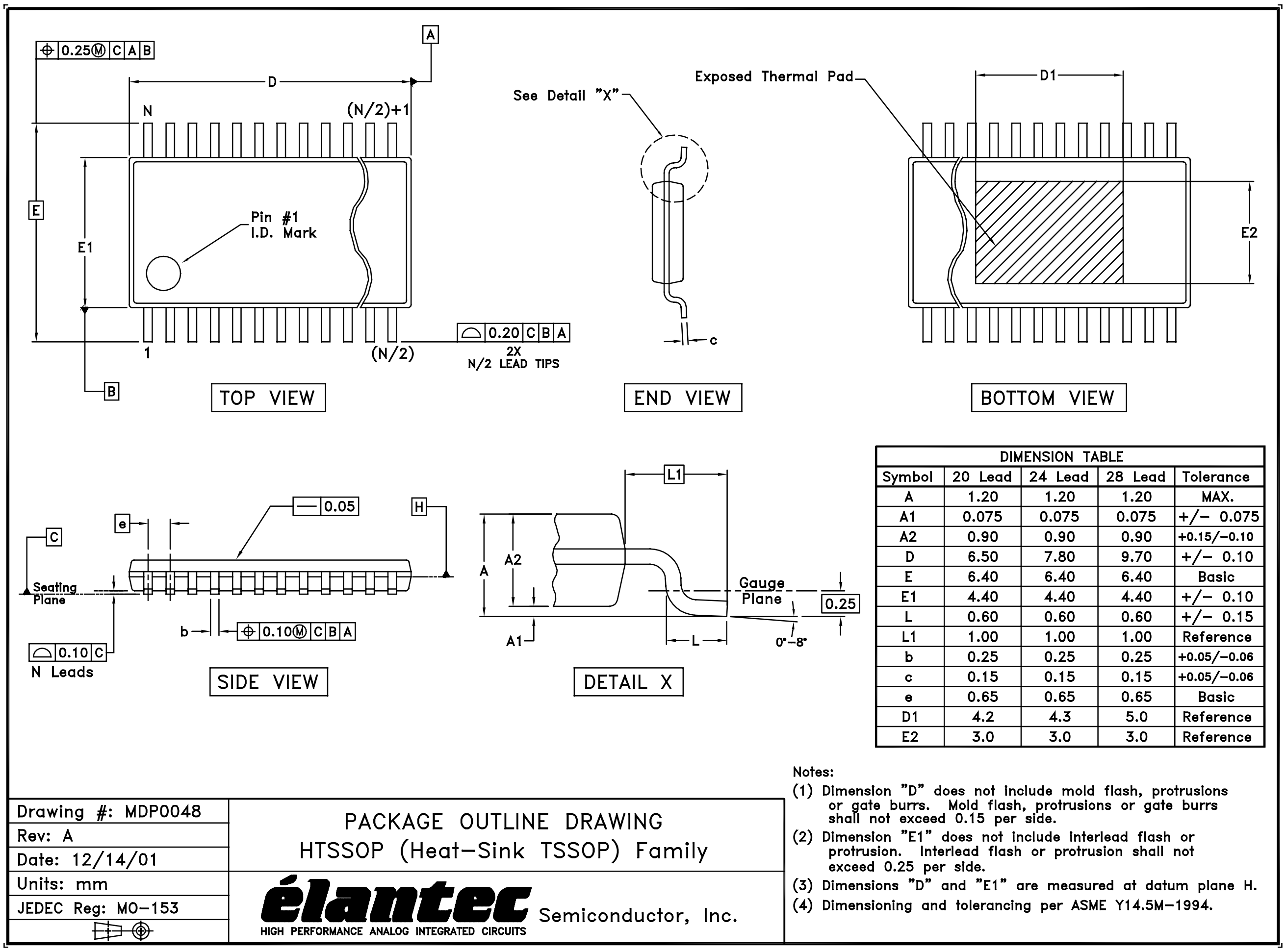
Power Control Function

The EL1527 contains two forms of power control operation. Two digital inputs, C_0 and C_1, can be used to control the supply current of the EL1527 drive amplifiers. As the supply current is reduced, the EL1527 will start to exhibit slightly higher levels of distortion and the frequency response will be limited. The four power modes of the EL1527 are set up as shown in the table below.

POWER MODES OF THE EL1527

C_1	C_0	OPERATION
0	0	I_S Full Power Mode
0	1	3/4-I_S Power Mode
1	0	1/2-I_S Power Mode
1	1	Power Down

Package Outline Diagram



DIMENSION TABLE				
Symbol	20 Lead	24 Lead	28 Lead	Tolerance
A	1.20	1.20	1.20	MAX.
A1	0.075	0.075	0.075	+/- 0.075
A2	0.90	0.90	0.90	+0.15/-0.10
D	6.50	7.80	9.70	+/- 0.10
E	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	+/- 0.10
L	0.60	0.60	0.60	+/- 0.15
L1	1.00	1.00	1.00	Reference
b	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	+0.05/-0.06
e	0.65	0.65	0.65	Basic
D1	4.2	4.3	5.0	Reference
E2	3.0	3.0	3.0	Reference

Notes:
(1) Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
(2) Dimension "E1" does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
(3) Dimensions "D" and "E1" are measured at datum plane H.
(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

Drawing #: MDP0048	PACKAGE OUTLINE DRAWING
Rev: A	HTSSOP (Heat-Sink TSSOP) Family
Date: 12/14/01	
Units: mm	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MO-153	