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74AC/ACT11898

10-bit serial-in parallel-out shift register

FEATURES

- Gated serial data inputs
- Fully buffered clock and data inputs
- Fully synchronous data transfers
- Typical shift frequency of 100MHz
- Asynchronous master reset
- Output capability: $\pm 24\text{mA}$
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11898 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11898 10-bit Serial-In Parallel-Out Shift Register is an edge-triggered shift register with serial data entry and an output from each of the 10 stages. Data is entered serially through one of two inputs (A • B); either input

(continued)

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | CONDITIONS $T_{amb} = 25^\circ\text{C}; \text{GND} = 0\text{V};$ $V_{CC} = 5.0\text{V}$ | TYPICAL | | UNIT |
|-------------------|---|---|---------|-----|------|
| | | | AC | ACT | |
| t_{PLH}/t_{PHL} | Propagation delay CP to Q_n ($\overline{MR} = \text{High}$) | $C_L = 50\text{pF}$ | 5.9 | 6.9 | ns |
| C_{PD} | Power dissipation capacitance ¹ | $f = 1\text{MHz}; C_L = 50\text{pF}$ | 122 | 117 | pF |
| C_{IN} | Input capacitance | $V_I = 0\text{V}$ or V_{CC} | 4.0 | 4.0 | pF |
| I_{LATCH} | Latch-up current | Per Jeduc JC40.2 Standard 17 | 500 | 500 | mA |
| f_{MAX} | Maximum clock frequency | $C_L = 50\text{pF}$ | 100 | 100 | MHz |

Note:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_I + \sum (C_L \times V_{CC}^2 \times f_O) \text{ where:}$$

f_I = input frequency in MHz, C_L = output load capacitance in pF,

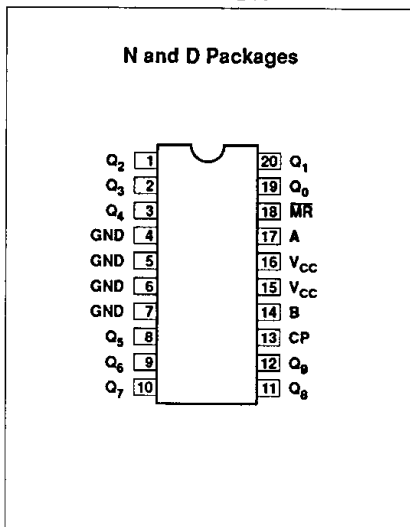
f_O = output frequency in MHz, V_{CC} = supply voltage in V,

$\sum (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

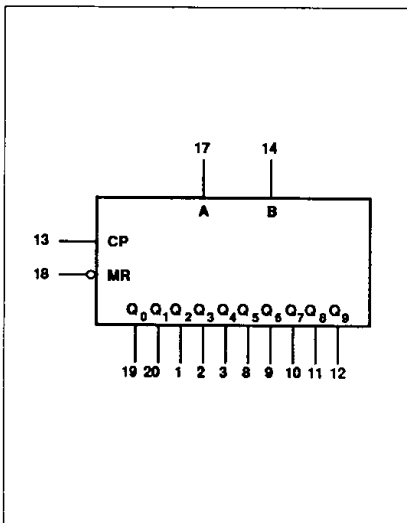
ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | ORDER CODE |
|----------------------------------|-------------------|---------------------------|
| 20-pin plastic DIP (300mil-wide) | -40°C to +85°C | 74AC11898N 74ACT11898N |
| 20-pin plastic SOL (300mil-wide) | -40°C to +85°C | 74AC11898D 74ACT11898D |

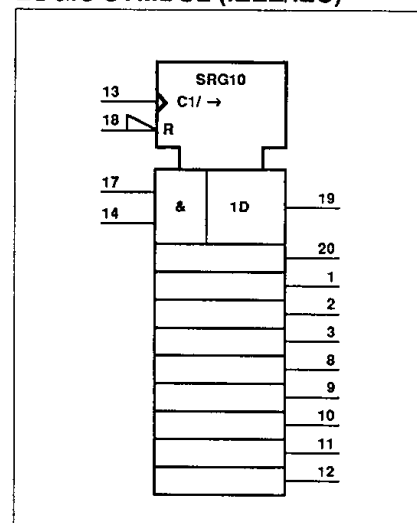
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



10-bit serial-in parallel-out shift register

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can be used as an active-High enable for data entry through the other input. Otherwise both inputs must be connected to the input data or an unused input must be tied High.

Data shifts one place to the right on each Low-to-High transition of the Clock (CP) input and enters the logical AND of the two inputs ($A \cdot B$) that existed one setup time before the rising clock edge

into Q_0 . A Low level on the Master Reset (\overline{MR}) input overrides all other inputs and clears the register asynchronously, forcing all outputs Low.

PIN DESCRIPTION

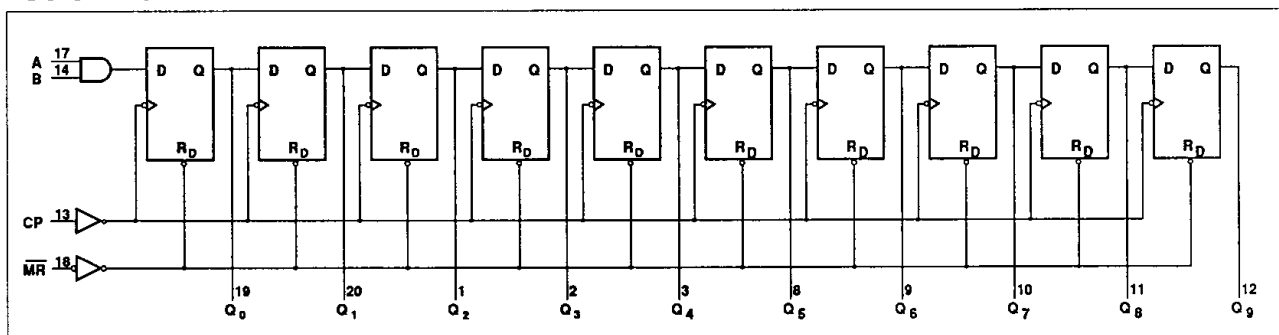
| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|-----------------------------------|-----------------|---|
| 18 | \overline{MR} | Asynchronous master reset (active Low) |
| 13 | CP | Clock input (Low-to-High, edge-triggered) |
| 17, 14 | A, B | Data inputs |
| 19, 20, 1, 2, 3, 8, 9, 10, 11, 12 | $Q_0 - Q_9$ | Parallel outputs outputs |
| 4, 5, 6, 7 | GND | Ground (0V) |
| 15, 16 | V_{CC} | Positive supply voltage |

FUNCTION TABLE

| OPERATING MODE | INPUTS | | | | OUTPUTS | | | |
|----------------|-----------------|------------|---|---|---------|-------|---|-------|
| | \overline{MR} | CP | A | B | Q_0 | Q_1 | — | Q_9 |
| Reset (clear) | L | X | X | X | L | L | — | L |
| Shift | H | \uparrow | l | l | L | q_0 | — | q_9 |
| | H | \uparrow | l | h | L | q_0 | — | q_9 |
| | H | \uparrow | h | l | L | q_0 | — | q_9 |
| | H | \uparrow | h | h | H | q_0 | — | q_9 |

H = High voltage level
 L = Low voltage level
 h = High voltage level one setup time prior to the Low-to High clock transition
 l = Low voltage level one setup time prior to the Low-to High clock transition
 X = Don't care
 q_n = State of the referenced input (or output) one setup time prior to the Low-to-High clock transition
 \uparrow = Low-to-High clock transition

LOGIC DIAGRAM



10-bit serial-in parallel-out shift register

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | 74AC11898 | | | 74ACT11898 | | | UNIT |
|---------------------|--------------------------------------|------------------|-----|----------|------------|-----|----------|------|
| | | Min | Nom | Max | Min | Nom | Max | |
| V_{CC} | DC supply voltage | 3.0 ¹ | 5.0 | 5.5 | 4.5 | 5.0 | 5.5 | V |
| V_I | Input voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| V_O | Output voltage | 0 | | V_{CC} | 0 | | V_{CC} | V |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | 0 | | 10 | 0 | | 10 | ns/V |
| T_{amb} | Operating free-air temperature range | -40 | | +85 | -40 | | +85 | °C |

NOTE:

1. No electrical or switching characteristics are specified at $V_{CC} < 3V$. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS¹

| SYMBOL | PARAMETER | TEST CONDITIONS | RATING | UNIT |
|-----------------------------|---|--------------------------------------|------------------------|------|
| V_{CC} | DC supply voltage | | -0.5 TO +7.0 | V |
| I_{IK} or V_I | DC input diode current ² | $V_I < 0$ | -20 | mA |
| | | $V_I > V_{CC}$ | 20 | |
| | DC input voltage | | -0.5 to $V_{CC} + 0.5$ | V |
| I_{OK} or V_O | DC output diode current ² | $V_O < 0$ | -50 | mA |
| | | $V_O > V_{CC}$ | 50 | |
| | DC output voltage | | -0.5 to $V_{CC} + 0.5$ | V |
| I_O | DC output source or sink current per output pin | $V_O = 0$ to V_{CC} | ±50 | mA |
| I_{CC} or I_{GND} | DC V_{CC} current | | ±250 | mA |
| | DC ground current | | ±250 | |
| T_{STG} | Storage temperature | | -65 to 150 | °C |
| P_{TOT} | Power dissipation per package | Above 70°C; derate linearly by 8mW/K | 500 | mW |
| | Power dissipation per package Plastic surface mount (SO) | Above 70°C; derate linearly by 8mW/K | 400 | mW |

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITIONS | V _{CC} | 74AC11898 | | | | 74ACT11898 | | | | UNIT | |
|--------------------------------------|--|---|-------------------------|--------------------------|------|-----------------------------------|------|--------------------------|------|-----------------------------------|------|------|------|
| | | | | T _{amb} = +25°C | | T _{amb} = -40°C to +85°C | | T _{amb} = +25°C | | T _{amb} = -40°C to +85°C | | | |
| | | | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| V _{IH} | High-level input voltage | | 3.0 | 2.10 | | 2.10 | | | | | | V | |
| | | | 4.5 | 3.15 | | 3.15 | | 2.0 | | 2.0 | | | |
| | | | 5.5 | 3.85 | | 3.85 | | 2.0 | | 2.0 | | | |
| V _{IL} | Low-level input voltage | | 3.0 | | 0.90 | | 0.90 | | | | | V | |
| | | | 4.5 | | 1.35 | | 1.35 | | 0.8 | | 0.8 | | |
| | | | 5.5 | | 1.65 | | 1.65 | | 0.8 | | 0.8 | | |
| V _{OH} | High-level output voltage | V _I = V _{IL} or V _{IH} | I _{OH} = -50μA | 3.0 | 2.9 | | 2.9 | | | | | V | |
| | | | | 4.5 | 4.4 | | 4.4 | | 4.4 | | 4.4 | | |
| | | | | 5.5 | 5.4 | | 5.4 | | 5.4 | | 5.4 | | |
| | | | I _{OH} = -4mA | 3.0 | 2.58 | | 2.48 | | | | | | |
| | | | | 4.5 | 3.94 | | 3.8 | | 3.94 | | 3.8 | | |
| | | | | 5.5 | 4.94 | | 4.8 | | 4.94 | | 4.8 | | |
| I _{OH} = -75mA ¹ | 3.0 | | | 3.85 | | | | 3.85 | | | | | |
| | 5.5 | | | | | | | | | | | | |
| V _{OL} | Low-level output voltage | V _I = V _{IL} or V _{IH} | I _{OL} = 50μA | 3.0 | | 0.1 | | 0.1 | | | | V | |
| | | | | 4.5 | | 0.1 | | 0.1 | | 0.1 | | | 0.1 |
| | | | | 5.5 | | 0.1 | | 0.1 | | 0.1 | | | 0.1 |
| | | | I _{OL} = 12mA | 3.0 | | 0.36 | | 0.44 | | | | | |
| | | | | 4.5 | | 0.36 | | 0.44 | | 0.36 | | | 0.44 |
| | | | | 5.5 | | 0.36 | | 0.44 | | 0.36 | | | 0.44 |
| I _{OL} = 75mA ¹ | 3.0 | | | | 1.65 | | | | 1.65 | | | | |
| | 5.5 | | | | | | | | | | | | |
| I _I | Input leakage current | V _I = V _{CC} or GND | 5.5 | | ±0.1 | | ±1.0 | | ±0.1 | | ±1.0 | μA | |
| I _{CC} | Quiescent supply current | V _I = V _{CC} or GND, I _O = 0mA | 5.5 | | 8.0 | | 80 | | 8.0 | | 80 | μA | |
| ΔI _{CC} | Supply current, TTL inputs High ² | One input at 3.4V, other inputs at V _{CC} or GND | 5.5 | | | | | | 0.9 | | 1.0 | mA | |

NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
- This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

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AC ELECTRICAL CHARACTERISTICS AT 3.3V $\pm 0.3V$

| SYMBOL | PARAMETER | WAVEFORM | 74AC11898 | | | | | UNIT |
|------------------------|--|----------|--------------------------|------------|-------------|--|--------------|------|
| | | | $T_{amb} = +25^{\circ}C$ | | | $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$ | | |
| | | | Min | Typ | Max | Min | Max | |
| f_{MAX} | Maximum clock frequency | 1 | 40 | 65 | | 40 | | MHz |
| t_{PLH} t_{PHL} | Propagation delay CP to Q_n | 1 | 3.3 3.9 | 8.1 8.8 | 9.8 10.5 | 3.3 3.9 | 10.8 11.5 | ns |
| t_{PHL} | Propagation delay MR to Q_n | 2 | 4.1 | 9.3 | 11.2 | 4.1 | 12.3 | ns |
| t_S | Setup time, High or Low A, B to CP | 3 | 14.0 | | | 14.0 | | ns |
| t_H | Hold time, High or Low A, B to CP | 3 | 0.0 | | | 0.0 | | ns |
| t_W | Clock pulse width (shift) High or Low | 1 | 12.5 | | | 12.5 | | ns |
| t_W | MR pulse width, Low | 2 | 4.0 | | | 4.0 | | ns |
| t_{REC} | Recovery time MR to CP | 2 | 1.5 | | | 1.5 | | ns |

AC ELECTRICAL CHARACTERISTICS AT 5.0V $\pm 0.5V$

| SYMBOL | PARAMETER | WAVEFORM | 74AC11898 | | | | | UNIT |
|------------------------|--|----------|--------------------------|------------|------------|--|------------|------|
| | | | $T_{amb} = +25^{\circ}C$ | | | $T_{amb} = -40^{\circ}C$ to $+85^{\circ}C$ | | |
| | | | Min | Typ | Max | Min | Max | |
| f_{MAX} | Maximum clock frequency | 1 | 75 | 100 | | 75 | | MHz |
| t_{PLH} t_{PHL} | Propagation delay CP to Q_n | 1 | 2.7 3.1 | 5.5 6.3 | 7.4 8.3 | 2.7 3.1 | 8.1 9.0 | ns |
| t_{PHL} | Propagation delay MR to Q_n | 2 | 3.8 | 6.7 | 8.6 | 3.8 | 9.4 | ns |
| t_S | Setup time, High or Low A, B to CP | 3 | 8.5 | | | 8.5 | | ns |
| t_H | Hold time, High or Low A, B to CP | 3 | 0.0 | | | 0.0 | | ns |
| t_W | Clock pulse width (shift) High or Low | 1 | 6.7 | | | 6.7 | | ns |
| t_W | MR pulse width, Low | 2 | 4.0 | | | 4.0 | | ns |
| t_{REC} | Recovery time MR to CP | 2 | 1.5 | | | 1.5 | | ns |

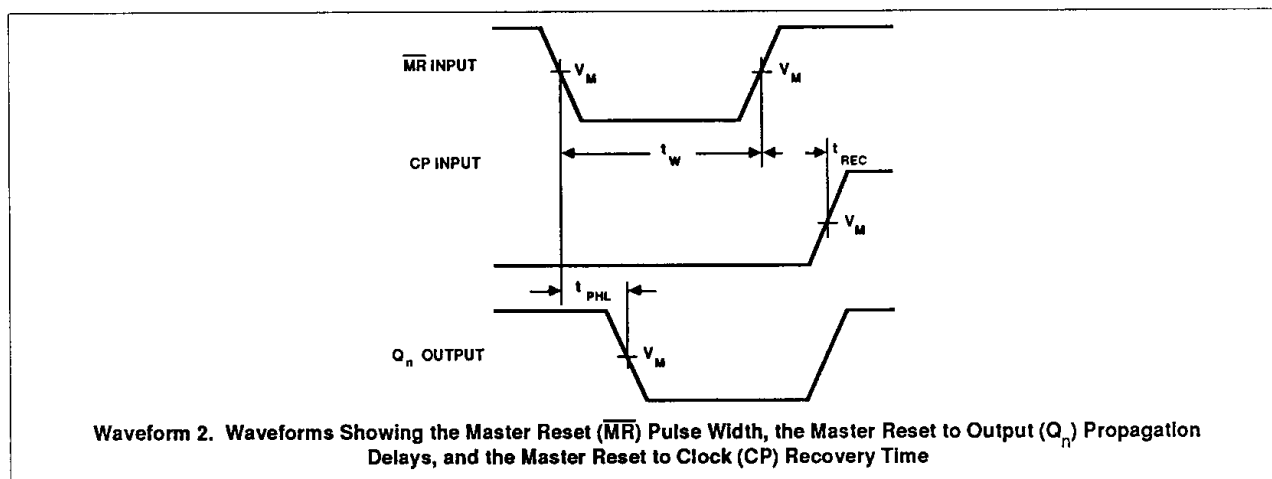
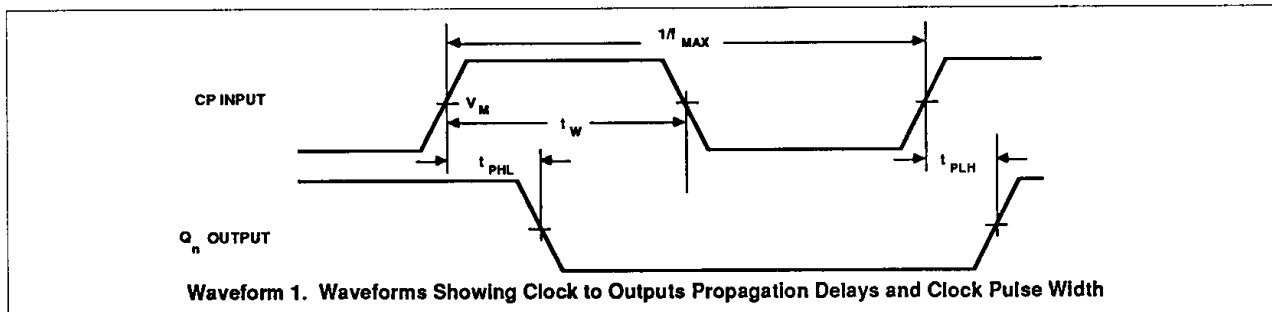
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AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

| SYMBOL | PARAMETER | WAVEFORM | 74ACT11898 | | | | | UNIT |
|--------------------------------------|---|----------|--------------------------|------------|------------|-----------------------------------|------------|------|
| | | | T _{amb} = +25°C | | | T _{amb} = -40°C to +85°C | | |
| | | | Min | Typ | Max | Min | Max | |
| f _{MAX} | Maximum clock frequency | 1 | 75 | 100 | | 75 | | MHz |
| t _{PLH} t _{PHL} | Propagation delay CP to Q _n | 1 | 4.1 4.4 | 6.5 7.2 | 8.0 8.8 | 4.1 4.4 | 8.8 9.6 | ns |
| t _{PHL} | Propagation delay MR to Q _n | 2 | 4.6 | 8.0 | 10.3 | 4.6 | 11.3 | ns |
| t _S | Setup time, High or Low A, B to CP | 3 | 9.5 | | | 9.5 | | ns |
| t _H | Hold time, High or Low A, B to CP | 3 | 0.0 | | | 0.0 | | ns |
| t _w | Clock pulse width (shift) High or Low | 1 | 6.7 | | | 6.7 | | ns |
| t _w | MR pulse width, Low | 2 | 4.5 | | | 4.5 | | ns |
| t _{REC} | Recovery time MR to CP | 2 | 1.5 | | | 1.5 | | ns |

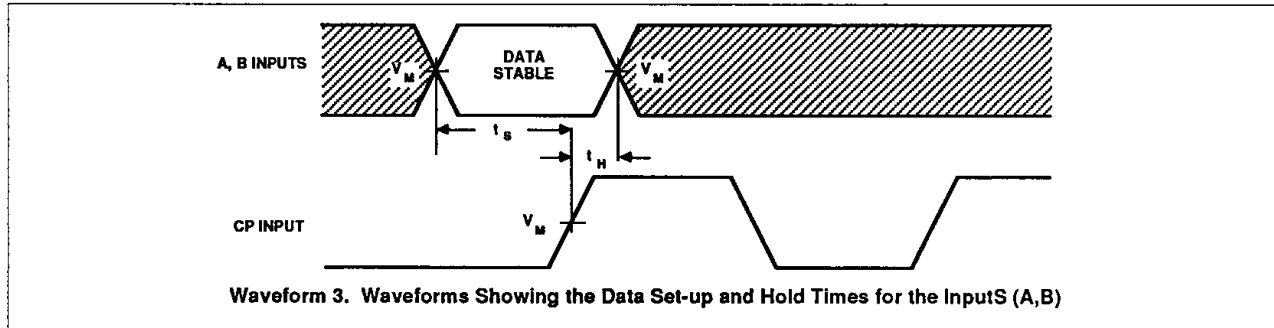
AC WAVEFORMS



10-bit serial-in parallel-out shift register

74AC/ACT11898

AC WAVEFORMS (Continued)



WAVEFORM CONDITIONS

| | INPUTS | OUTPUTS |
|-----|--|---------------------------------------|
| AC | $V_{IN} = \text{GND to } V_{CC}$ $V_M = 50\% V_{CC}$ | $V_{OUT} = V_{OL} \text{ to } V_{OH}$ |
| ACT | $V_{IN} = \text{GND to } 3.0\text{V}$ $V_M = 1.5\text{V}$ | $V_M = 50\% V_{CC}$ |

TEST CIRCUIT

