P4C215/P4C216
ULTRA HIGH-SPEED 2x8K x15 or x16 BiCameral Latched Cache RAMs

PRELIMINARY

FEATURES

- **High Performance R3000A Caches**

Processor Frequency	Access Time	Output Enable
40 MHz	13 ns	4.5 ns
33 MHz	17 ns	7 ns
25 MHz	23 ns	9 ns

- **Instruction & Data Cache on One Chip**
- **On-chip Address Latches**
- **Depth expansion to 64KB caches (16K deep) without decoding delays.**
- **Uses Performance's PACE III 5V Technology**
- **Single 5V ± 10% Power Supply**
- **TTL Compatible Inputs and Outputs**
- **Common Data I/O**
- **Three-state Outputs**
- **CMOS for Low Power Dissipation**
- **Package Options**
  52-pin PLCC; 52-pin Quad Cerpack

DESCRIPTION

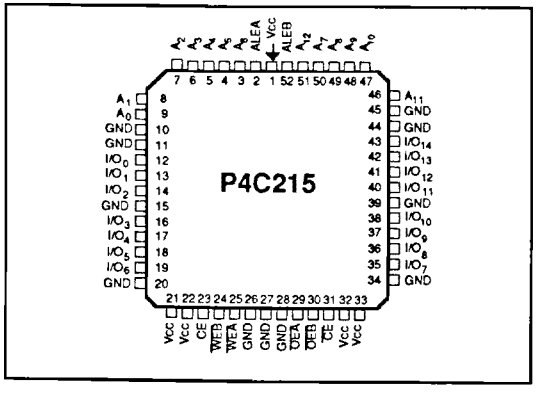
The P4C215 and P4C216 are 245,760 and 262,144-bit ultra high-speed CMOS cache SCRAMs. Organized as 2 x 8192 x 15 and 2 x 8192 x16, these static RAMs are ideally suited for PACEMIPS R3000, PACEMIPS R3000A and PACEMIPS 3400 RISC processor cache RAM applications. For ease of use, the SCRAMs feature TTL-compatible I/O and operate from a 5V ±10% tolerance power supply.

On-chip address latches permit a 13ns SCRAM, which has an output enable time of 4.5ns, to support 40 MHz processors. The P4C215 and P4C216 SCRAMs significantly reduce system part count, power dissipation, trace line length, capacitance and board area, resulting in improved system margin and packing density. When using the P4C215, 60-bit-wide 32K byte instruction and data caches can be obtained with only four chips. For applications requiring a maximum of 16M DRAM, a 48-bit-wide 32K byte instruction and data cache can be obtained with only three chips when using the P4C216. The P4C215 and P4C216 are members of the PACE RAM family of products offering super fast access times.

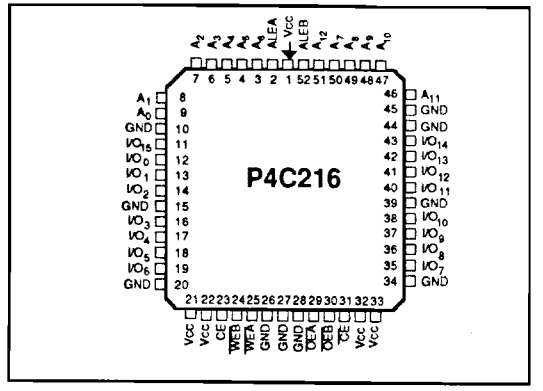
P4C215/P4C216 is manufactured using PACE III 5V technology and supported by a six-inch wafer fabrication production facility.

Package options for the P4C215 & P4C216 include 52-pin PLCC and 52-pin Quad Cerpack surface mount packages; each provides excellent board-level density.

PIN CONFIGURATION (2x8Kx15)



PIN CONFIGURATION (2x8Kx16)



PIN DESCRIPTIONS

PLCC Pin Number(s)	Symbol	Type	Description
3, 4, 5, 6, 7, 8, 9, 46, 47, 48, 49, 50, 51	A_0–A_{12}	Input	Address Inputs: These signals are latched on the negative edge of ALE.
2, 52	ALEA,ALEB	Input	Address Latch Enable: When ALEA/ALEB is high the respective latch is transparent. The negative edge latches the current address inputs (A_0–A_{12}) for side A or B.
23, 31	CE,CE	Input	Chip Enables: These are global control signals that activate sides A and B of the array. They also facilitate depth expansion. Both inputs are latched.
29, 30	$\overline{OEA}$,$\overline{OEB}$	Input	Output Enables: Active LOW enables cache bank A or B to drive data bus. Simultaneous activation is not possible in MIPS R3000 application, but if so, then data from bank B is on the output.
25, 24	$\overline{WEA}$,$\overline{WEB}$	Input	Write Enables: These active LOW signals enable bank A or B. Simultaneous activation is not possible in MIPS R3000 application, even though $\overline{WEA}$ and $\overline{WEB}$ work independently and asynchronously.
12, 13, 14, 16, 17, 18, 19, 35 36, 37, 38, 40, 41, 42, 43	I/O_0–I/O_{14}	I/O	I/O: Data inputs and outputs for P4C215 and P4C216.
11	I/O_{15} GND	I/O GND	I/O: Data input and output P4C216 Ground for P4C215
1, 21, 22, 32, 33	V_{CC}	Supply	5V ±10%
10, 15, 20, 26, 27, 28, 34, 39, 44, 45	GND	GND	Ground

FUNCTIONAL BLOCK DIAGRAM

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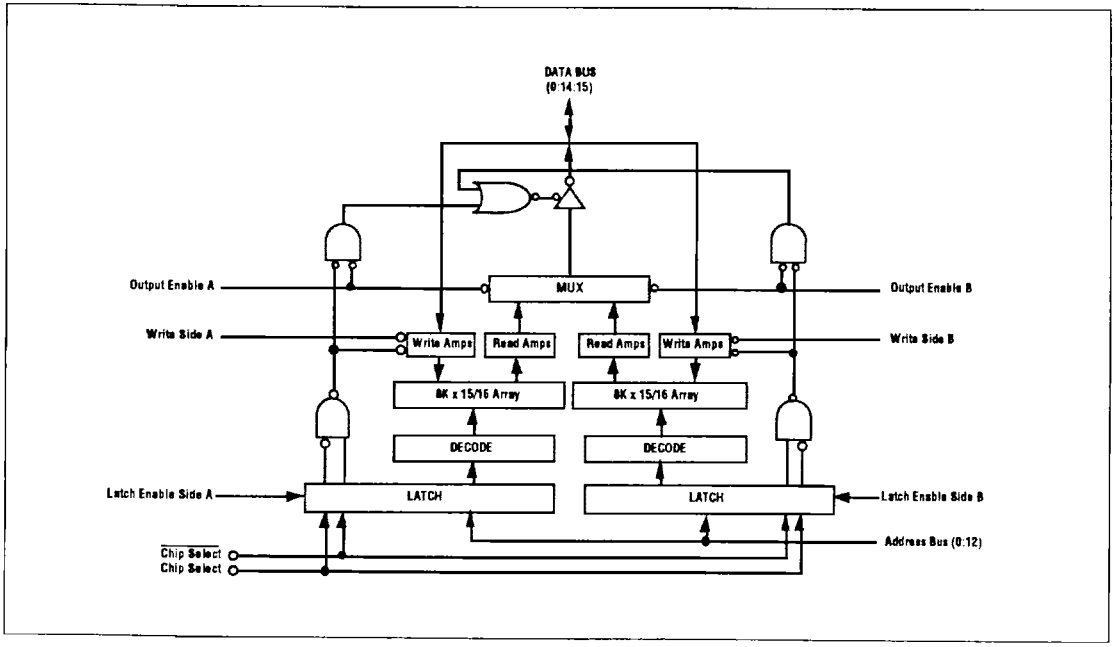

ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	–0.5 to +7.0	V
V_{IN}	DC Input Voltage	–0.5 to +7.0	V
$V_{I/O}$	DC Input Voltage Applied to Output in High-Z	–0.5 to V_{CC}+0.5	V
P_D	Power Dissipation	1.5	W
T_{OPR}	Operating Temperature	–55 to +125	°C

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C

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RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade[2]	Ambient Temperature	GND	V_{CC}
Military	–55 to +125°C	0V	5.0V ± 10%

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Grade[2]	Ambient Temperature	GND	V_{CC}
Commercial	0°C to +70°C	0V	5.0V ± 5%

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating temperature and supply voltage

Symbol	Parameter	Test Conditions	P4C215/16		Unit
			Min	Max	
V_{IH}	Input High Voltage		2.2	V_{CC}+0.5	V
V_{IL}	Input Low Voltage		–0.5[2]	0.8	V
I_{LI}	Input Leakage Current	GND < V_{IN} < V_{CC}	–10	+10	µA
I_{LO}	Output Leakage Current	GND < V_O < V_{CC}, Output Disabled	–10	+10	µA
I_{CC}	VCC Operating Current	V_{CC} = Max., I_{OUT} = 0 mA, f = max. (Note 4)		360	mA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8 mA		0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = –4 mA	2.4		V
I_{OS}	Output Short Circuit Current	V_{CC} = Max., I_{OUT} = GND		–350	mA

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CAPACITANCES[3]

(V_{CC} = 5.0V, T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	5	pF

Symbol	Parameter	Conditions	Typ.	Unit
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	pF

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Notes:

1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Transient inputs with V_I & I_I not more negative than –3.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
3. This parameter is sampled and not 100% tested.
4. I_{CC} is measured with input levels at 0.0V and 3.0V except $\overline{OE}_A$ & $\overline{OE}_B \geq$ 3.0V.

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

(V_{CC} = 5V ± 5%, Commercial Temperature Range/ 5V ±10%, Military Temperature Range)

Symbol	Parameter	40 MHz -13		33 MHz -17		25 MHz -23		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	13		17		23		ns
t_{AA}	Address Access Time		13		17		23	ns
t_{OE}	Output Enable Low to Output Valid		4.5		7		9	ns
t_{OH}	Output Hold from Address Change	2		3		3		ns
t_{OLZ}	Output Enable Low to Low-Z	2		2		2		ns
t_{OHZ}	Output Enable High to High-Z		5		6		8	ns
t_{PALE}	ALE Pulse Width	6		6		6		ns
t_{SALE}	Address Setup to ALE Low	2		2		2		ns
t_{HALE}	Address Hold from ALE Low	2		2		2		ns

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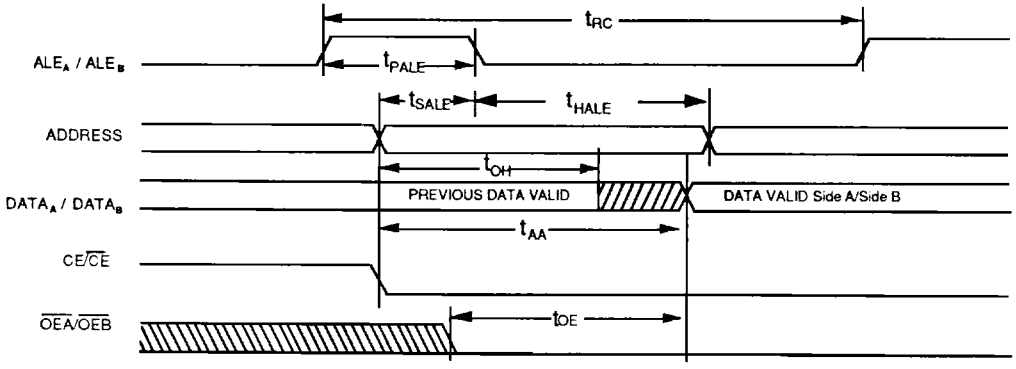
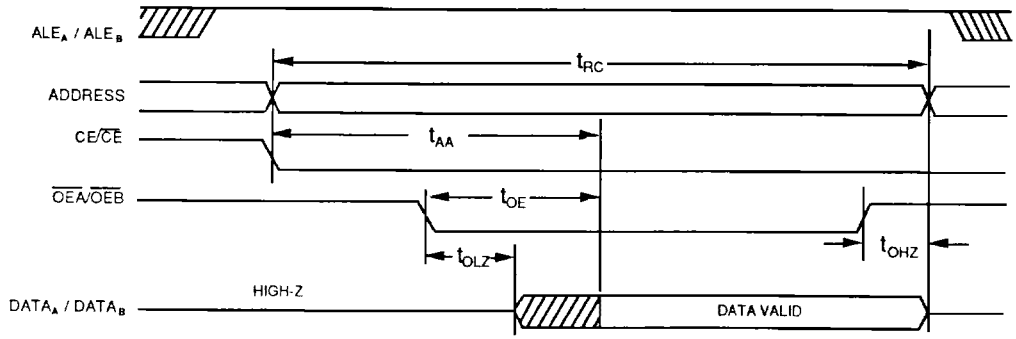
☐ Advance Information

Notes: t_{OLZ}, t_{OHZ} are measured at ±200mV from steady state high impedance level.
Simultaneous switching of $\overline{OE}_A$, $\overline{OE}_B$ to swap Banks A & B at the output does not occur in PR3000A/PR3400 cache applications.
So t_{OE} is specified with $\overline{OE}_A$ HIGH and $\overline{OE}_B$ transitioning LOW, and vice versa.

READ CYCLE NO.1 (ALE Controlled)



READ CYCLE NO.2 (Address/CE Controlled)



AC ELECTRICAL CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 5%, Commercial Temperature Range/ 5V ±10%, Military Temperature Range)

Symbol	Parameter	40 MHz -13		33 MHz -17		25 MHz -23		Unit
		Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	13		17		23		ns
t_{AW}/t_{CW}	Address/Chip Enable To End of Write	13		17		23		ns
t_{AS}	Address Setup to Write Enable	0		0		0		ns
t_{DS}	Data Setup to End of Write	5.5		8		10		ns
t_{WP}	Write Enable Pulse Width	8		12		15		ns
t_{AH}	Address Hold from Write Enable	0		0		0		ns
t_{DH}	Data Hold from Write End	0		0		0		ns
t_{PALE}	ALE Pulse Width	6		6		6		ns
t_{SALE}	Address/Chip Enable Setup to ALE Low	2		2		2		ns
t_{HALE}	Address/Chip Hold from ALE Low	2		2		2		ns

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☐ Advance Information

Notes:

1. CE controlled WRITE operation is not possible.
2. ALE can go HIGH only after WE goes HIGH [i.e., there is a hold time for ALE (LOW) from WE (HIGH) of at least 0ns].
3. Since Chip Enable controlled WRITE operation is not possible in PACEMIPS PR3000A/PR3400 applications, Address Valid to End of WRITE (t_{AW}) and Chip Enable to End of Write (t_{CW}) are equal and merged together.

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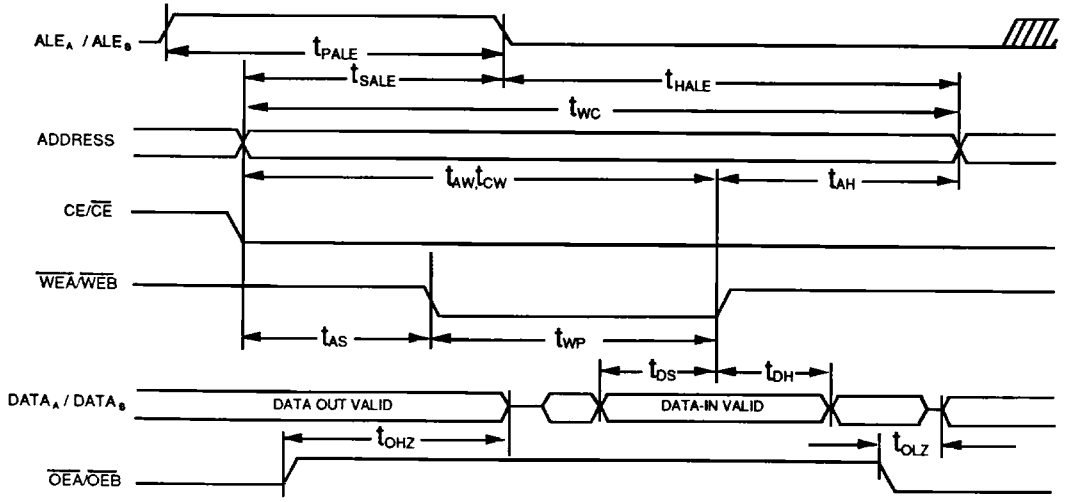
WRITE CYCLE



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Figures 1 & 2

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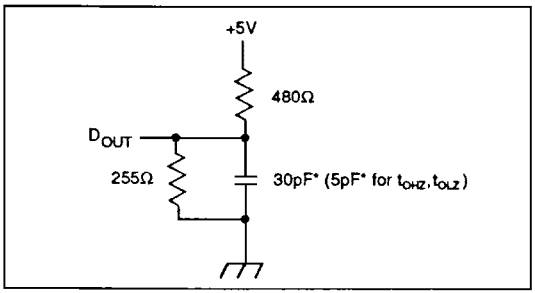

Figure 1. Output Load

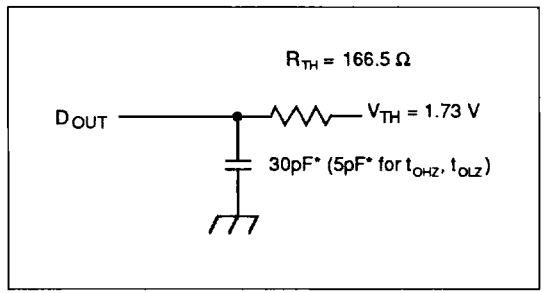

Figure 2. Thevenin Equivalent

* Including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C215/216, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

TRUTH TABLE

Mode	$\overline{CE}$	CE	$\overline{OEA}$	$\overline{OEB}$	$\overline{WEA}$	$\overline{WEB}$	I/O
Deselected	H	L	X	X	X	X	High Z
Output Inhibit	L	H	H	H	H	H	High Z
Read-Side A	L	H	L	H	H	H	D_{OUT}-Side A
Read-Side B	L	H	H	L	H	H	D_{OUT}-Side B
(Invalid Operation)	L	H	L	L	H	H	D_{OUT}-Side B
Write-Side A	L	H	H	H	L	H	D_{IN}-Side A
Write-Side B	L	H	H	H	H	L	D_{IN}-Side B

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Notes:
Even though $\overline{WEA}$ & $\overline{WEB}$ may work independently and asynchronously, simultaneous activation is not possible in PaceMips PR3000A and PR3400 applications.

This truth table applies to the latched versions of CE and $\overline{CE}$ on Side A and Side B.

DEPTH EXPANSION MODE

In applications where 64K byte instruction and data caches are required, the P4C215/16 can be expanded to 16K depth (64K byte) as shown in Figure 3. By connecting CE and $\overline{CE}$ to higher order address bit A13, only one of the upper and lower sets of SCRAMs is on at any given time, thus permitting depth expansion to 16K without incurring a speed penalty.

APPLICATION DIAGRAM

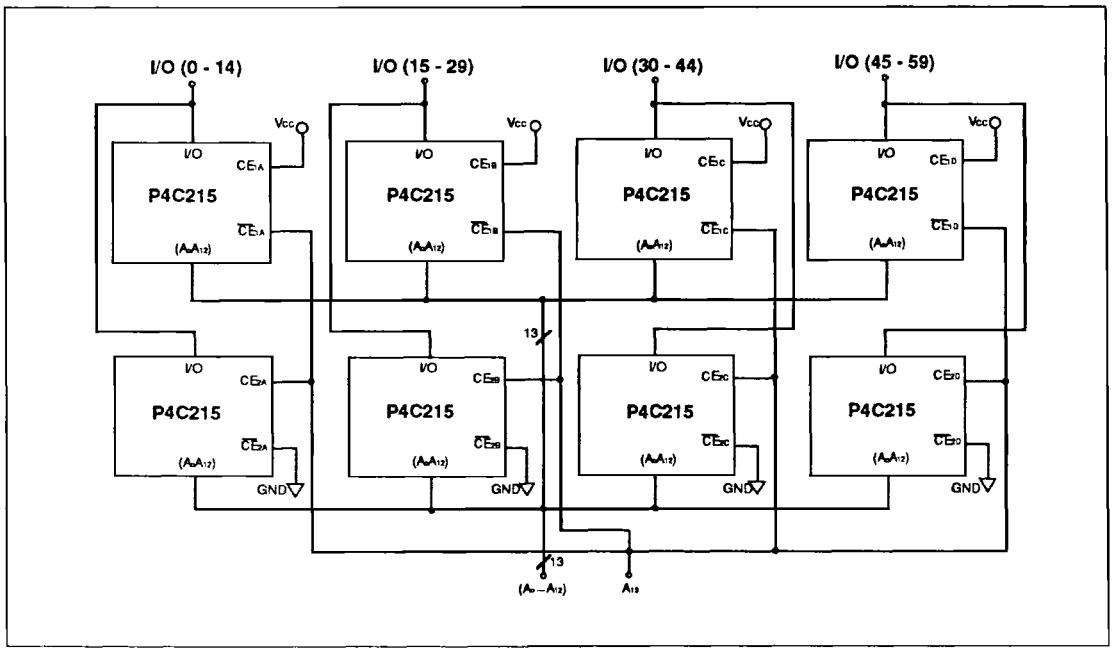

Figure 3. PACEMIPs PR3000 Cache RAM (16Kx60 I - Cache & 16Kx60 D - Cache)

TRUTH TABLE FOR DEPTH EXPANSION

CE_{1X}	A13 ($\overline{CE}_{1X}$/CE_{2X})	$\overline{CE}_{2X}$	UPPER SCRAM SET	LOWER SCRAM SET
H	H	L	OFF	ON
H	L	L	ON	OFF

PACKAGE SUFFIX

Package Suffix	Description
PP	Plastic Leaded Chip Carrier (PLCC)
SR	Leaded Ceramic Chip Carrier

TEMPERATURE RANGE SUFFIX

Temperature Range Suffix	Description
C	Commercial Temperature Range, 0°C to +70°C.
B	–55°C to +125°C with MIL-STD-883D Class B compliance

SELECTION GUIDE

The P4C215 and P4C216 are available in the following temperature, speed and package options.

Temperature Range	Package	13ns	17ns	23ns
Commercial	PLCC	-13 PP52C	-17 PP52C	-23 PP52C
Military Processed*	Leaded Ceramic Chip Carrier	N/A	-17 SR52B	-23 SR52B

* Military temperature range with MIL-STD-883 Revision D, Class B processing.
N/A = Not available

ORDERING INFORMATION

The following part numbering scheme is used for