Low Power First-In First-Out (FIFO) 64x4 Memory
67L401

Features/Benefits

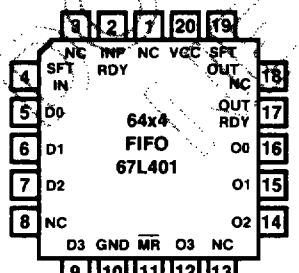
- Guaranteed 5 MHz shift-out/shift-in rates
- Low Power Consumption
- TTL inputs and outputs
- Readily expandable in the bit dimensions
- Structured pinouts. Output pins directly opposite corresponding input pins
- Asynchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and much faster

Description

The 67L401 is a low-power First-In First-Out (FIFO) memory device with TTL speed. This device is organized in a 64x4-bit structure and easily expandable to any width. A 5 MHz data rate with fast "fall through" time allows usage in tape and disc controllers, printers and communications buffer applications. This data rate is much faster than a comparable MOS device. The FIFO is a register-based device. Data entered at the inputs "falls through" to the empty space closest to the output. Data is shifted out in the same sequence it is shifted in. Also, the width can be increased by putting the Input Ready signals through an AND gate to give a composite Input Ready. Similarly, the Output Ready signals should be gated to form a composite Output Ready.

Generally, FIFOs are used in digital systems performing data transfers when source and receiver are not operating at the same data rate. FIFOs are also used as data buffers where the source and receiver are not operating at the same time. The 67L401 is particularly useful where low-power consumption is critical.

Pin Configurations



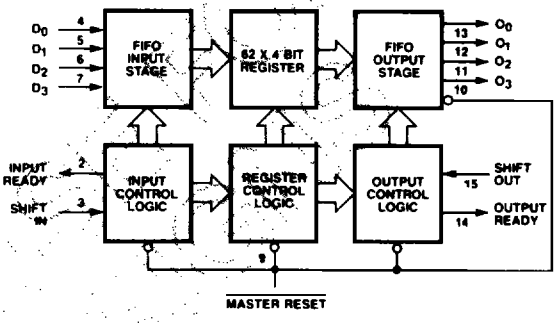
Plastic Chip Carrier

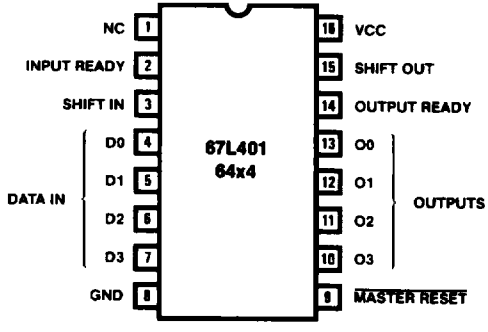
Ordering Information

PART NUMBER	PKG	TEMP	DESCRIPTION
67L401	N, NL	COM	5 MHz 64x4 FIFO
67L401	J, NL	COM	5 MHz 64x4 FIFO

Block Diagram

67L401 64x4





Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
t_{SIH}†	Shift in HIGH time	1	55			ns
t_{SIL}	Shift in LOW time	1	55			ns
t_{IDS}	Input data setup	1	10			ns
t_{IDH}	Input data hold time	1	80			ns
t_{SOH}†	Shift Out HIGH time	5	55			ns
t_{SOL}	Shift Out LOW time	5	55			ns
t_{MRW}	Master Reset pulse	10	40			ns
t_{MRS}	Master Reset to SI	10	35			ns

Switching Characteristics Over Operating Conditions

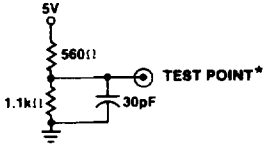
SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
f_{IN}	Shift in rate	1	5			MHz
t_{IRL}†	Shift in to Input Ready LOW	1			75	ns
t_{IRH}†	Shift in to Input Ready HIGH	1			75	ns
f_{OUT}	Shift Out rate	5	5			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			75	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			80	ns
t_{ODH}	Output Data Hold (previous word)	5	8			ns
t_{ODS}	Output Data Shift (next word)	5			70	ns
t_{PT}	Data throughput or "fall-through"	4, 8			4	μs
t_{MRORL}	Master Reset to OR LOW	10			85	ns
t_{MRIRH}	Master Reset to IR HIGH	10			85	ns
t_{IPH}*	Input Ready pulse HIGH	4	20			ns
t_{OPH}*	Output Ready pulse HIGH	8	20			ns

† See AC test and application note.

* This parameter applies to FIFOs communicating with each other in a cascade mode.

Test Load

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.



Input Pulse 0 to 3 V
Input Rise and Fall Time (10% - 90%)
5 ns minimum
Measurements made at 1.5 V

2

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = -18mA			-1.5	V
I_{IL1}	Low-level	D_0-D_3 MR	V_{CC} = MAX	V_I = 0.45V			-0.8	mA
I_{IL2}	input current	SI, SO					-1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		V_{CC} = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = -0.9mA	2.4			V
I_{OS}	Output short-circuit current*		V_{CC} = MAX	V_O = 0V	-20		-90	mA
I_{CC}	Supply Current		V_{CC} = MAX	Inputs Low, Outputs Open		95	110	mA

* Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
† This is an absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment.

Functional Description

Data Input

After power up the Master Reset is pulsed low (Fig. 11) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty).

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC Test and Application Note

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing. Though the external data rate is 5 MHz internally the device is several times as fast. Device grounding and decoupling is crucial to correct operation, as the FIFO will respond to very small glitches caused by long reflective lines, high capacitances and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in timing set up and measurement of parameters. For example, since an AND gate function is associated with both the Shift In-Input Ready Combination, as well as the Shift Out-Output Ready Combination, timing measurements may be misleading, i.e., rising edge of the Shift-In pulse is not recognized until Input-Ready is High.If Input-Ready is not high due to too high a frequency, or the FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High.

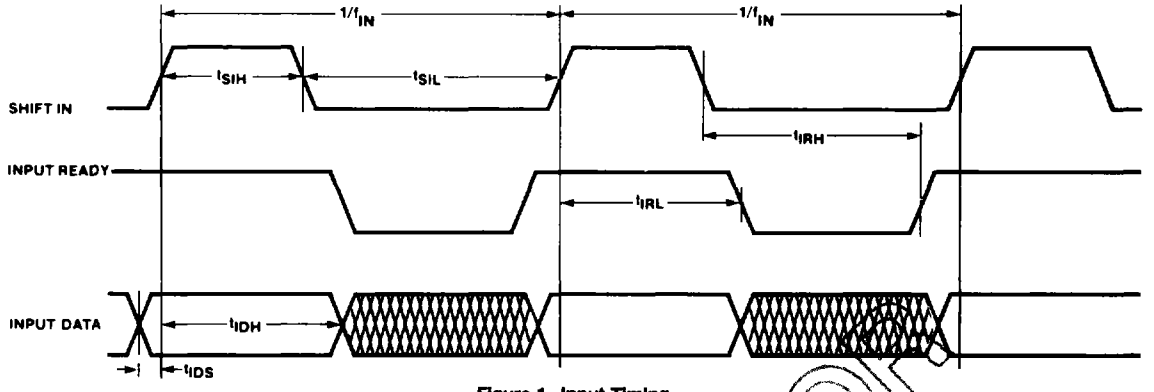


Figure 1. Input Timing

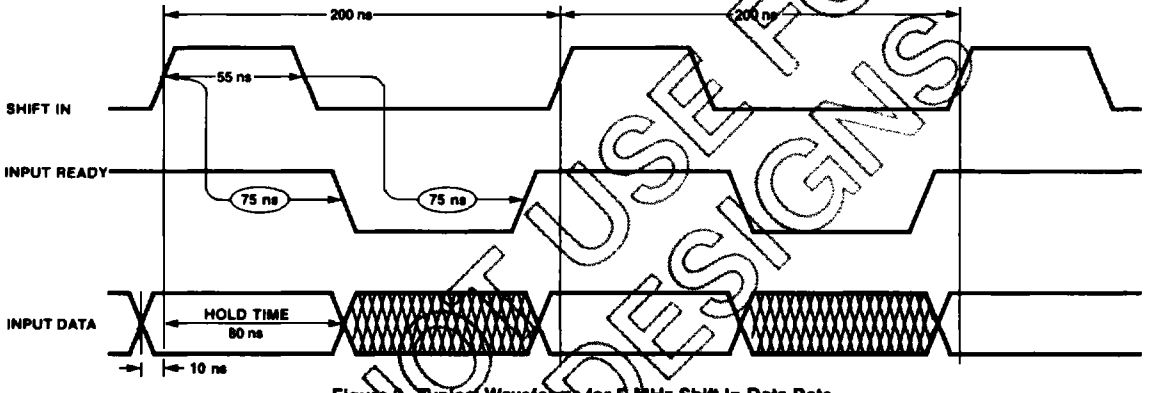


Figure 2. Typical Waveforms for 5 MHz Shift In Data Rate

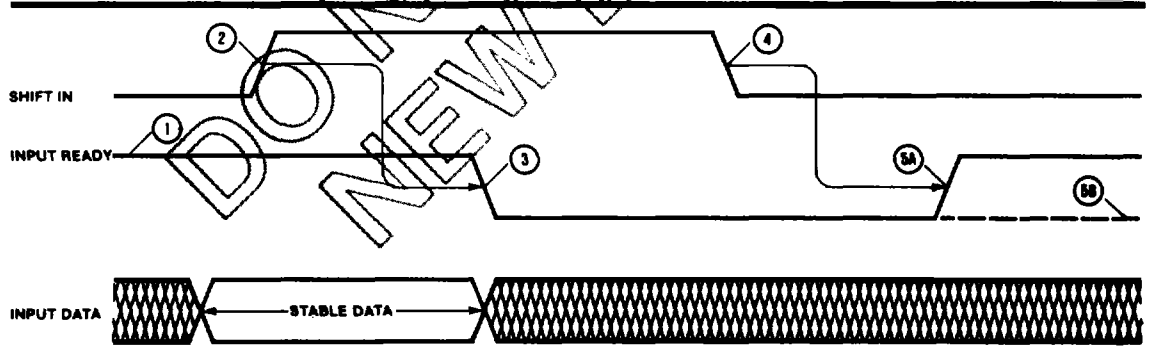


Figure 3. The Mechanism of Shifting Data Into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full

(4) The Data from the first word is released for "fall-through" to second word

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 5).

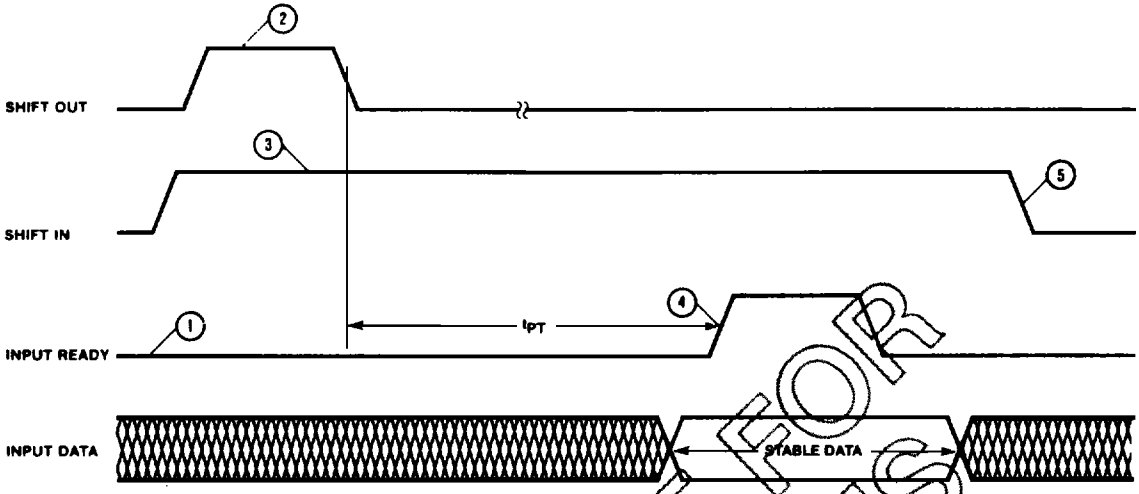


Figure 4. Data is Shifted In Whenever Shift In and Input Ready are Both HIGH

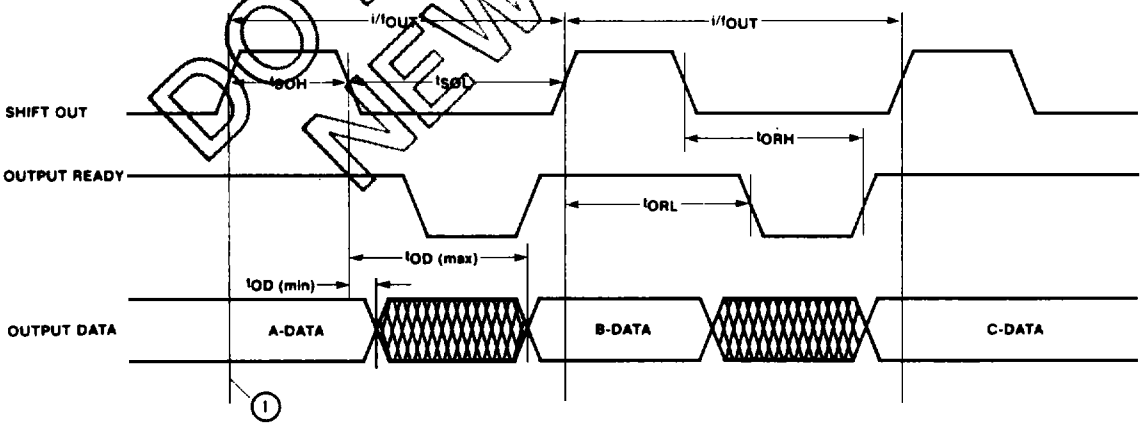
(1) FIFO is initially full

(2) Shift Out pulse is applied. An empty location start "bubbling" to the front

(3) Shift In is held HIGH

(4) As soon as Input Ready becomes HIGH the Input Data is loaded into the first word

(5) The Data from the first word is released for "fall through" to second word



(1) The diagram assumes that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively

Figure 5. Output Timing

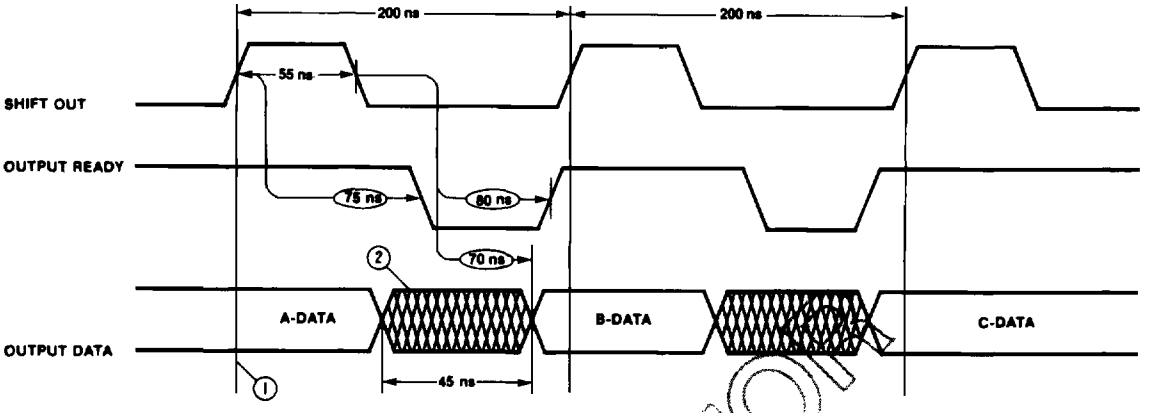


Figure 6. Typical Waveform for 5 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time words 63, 62, 61 are loaded with A, B, C Data respectively

(2) Data in the crosshatched region may be A or B Data

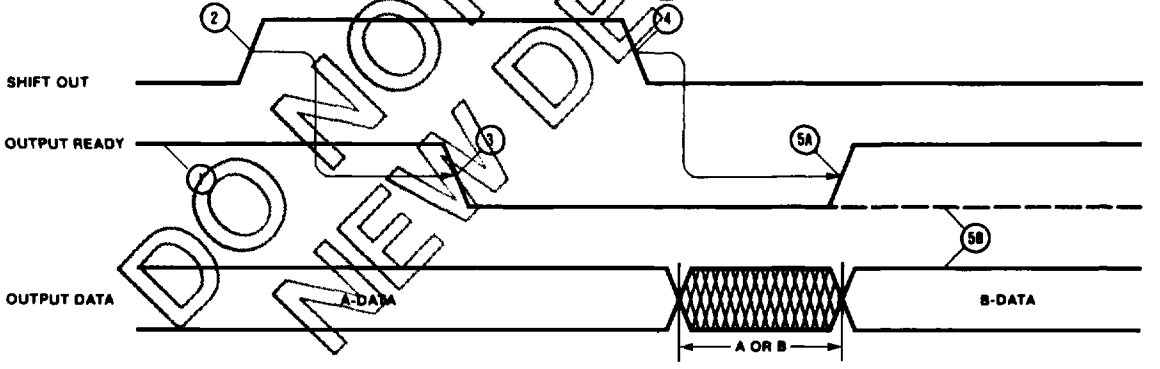


Figure 7. The Mechanism of Shifting Data Out of the FIFO

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

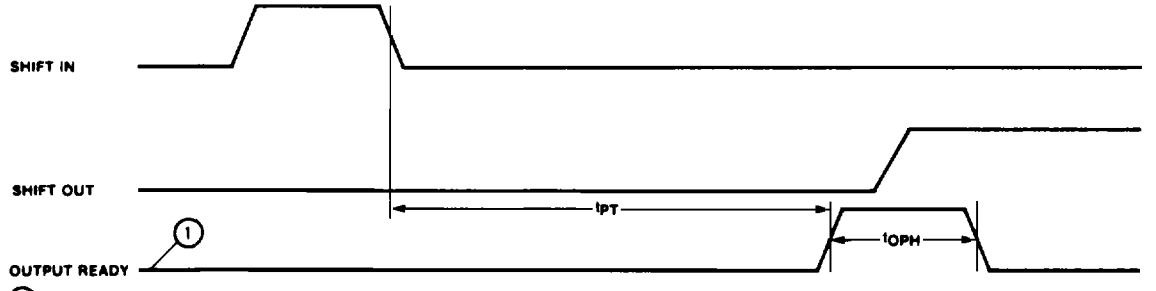
(2) Shift Out goes HIGH causing the next step.

(3) Output Ready goes LOW

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs



1 FIFO initially empty

Figure 8. t_{PT} and t_{OPH} Specification

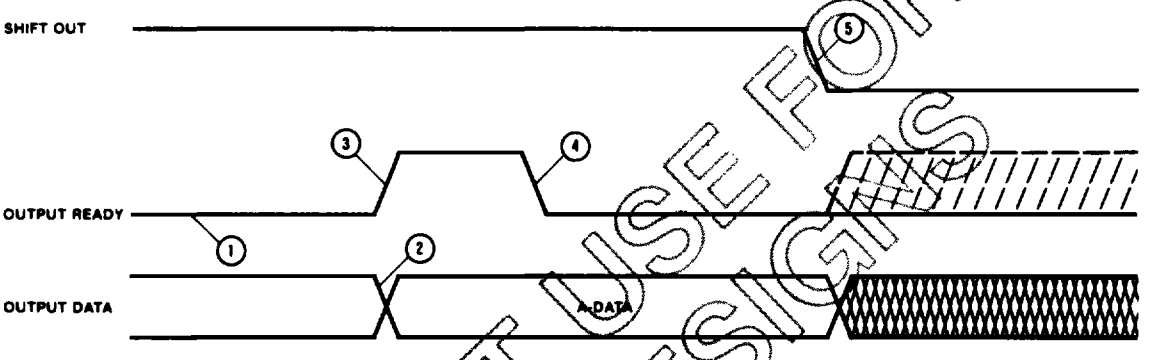
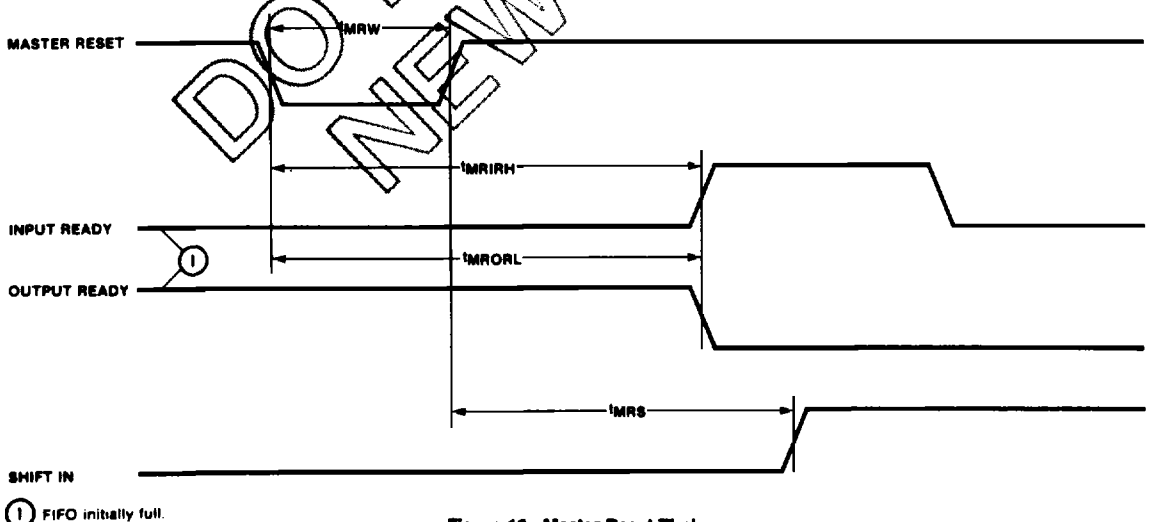


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH

1. Word 63 is empty
2. New data (A) arrives at the outputs (word 63)
3. Output Ready goes HIGH indicating the arrival of the new data
4. Since Shift Out is held HIGH, Output Ready goes immediately LOW
5. As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready



1 FIFO initially full.

Figure 10. Master Reset Timing

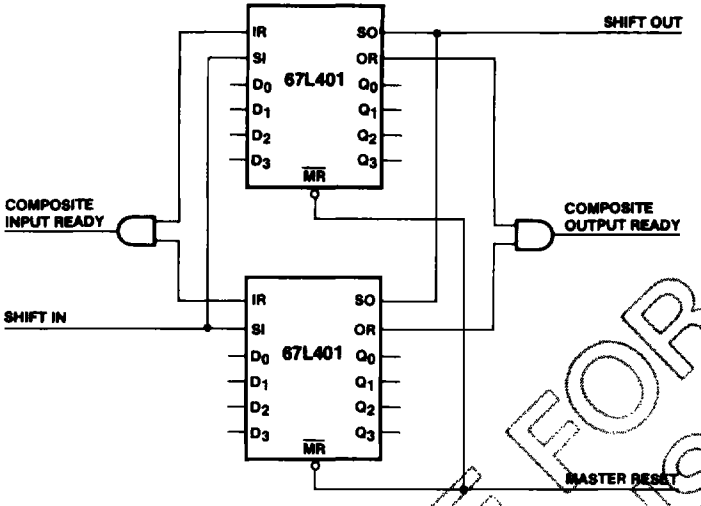


Figure 12. 64x8 FIFO With Two 67L401's

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FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall through times of the FIFOs.

Applications

FIFOs are typically used as temporary data buffers between mismatching data rates. Such an application is shown in Figure 13.

The 67L401 can also be used in a bidirectional operation as shown in Figure 14.

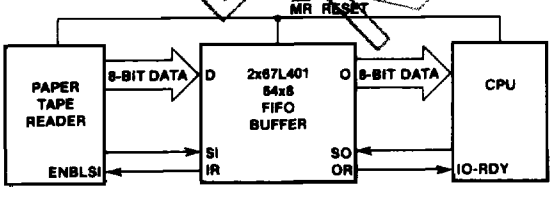
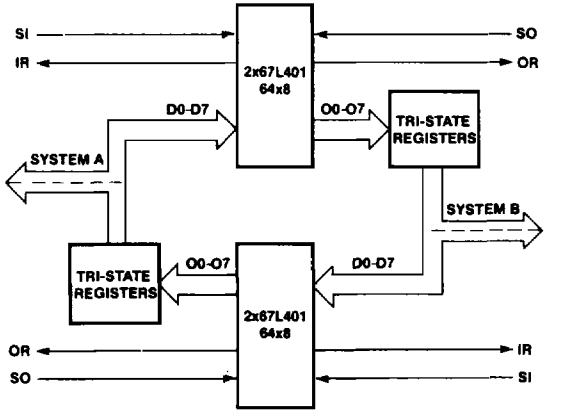


Figure 13. FIFO As Data Buffer Between Slow Steady Rate and Fast 'Burst' Rate



NOTE: Both depth and width expansion can be used in this mode.

Figure 14. Bidirectional FIFO Application