NEC

Phase-out/Discontinued

MOS INTEGRATED CIRCUIT

μPD70F3008

V854™

32-/16-BIT SINGLE-CHIP MICROCONTROLLER

The μPD70F3008 has a flash memory instead of the internal mask ROM of the μPD703008. Because this device can be programmed by users while mounted on a board, it is ideally suited for applications involving the evaluation of systems in the development stage, small-scale production of many different products, and rapid development and time-to-market of new products.

Functions are described in detail in the following user's manuals. Be sure to read these manuals during system design.

V854 User's Manual Hardware : U11969E
V850 Family™ User's Manual Architecture : U10243E

FEATURES

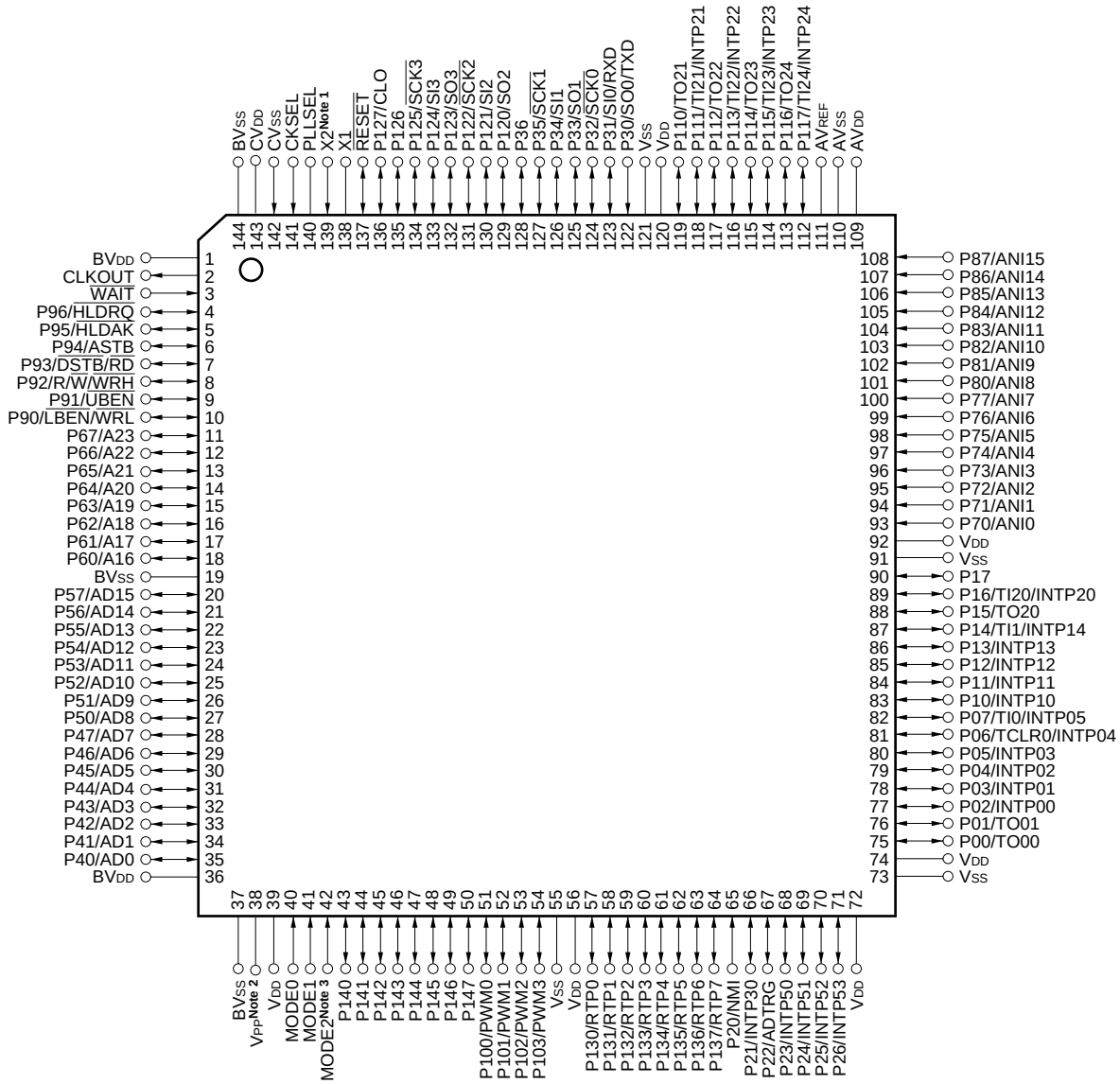
- Compatible with μPD703008
  - Can be replaced with mask ROM version μPD703008 for mass production of application set
- Internal flash memory: 128 Kbytes

ORDERING INFORMATION

Part Number	Package
μPD70F3008GJ-33-8EU	144-pin plastic LQFP (fine pitch) (20 × 20 mm)

Document No. U12756EJ1V0DS00 (1st edition)
Date Published August 1997 N
Printed in Japan

PIN CONFIGURATION (Top View)



Notes **1.** Leave open when external clock is connected to the X1 pin.

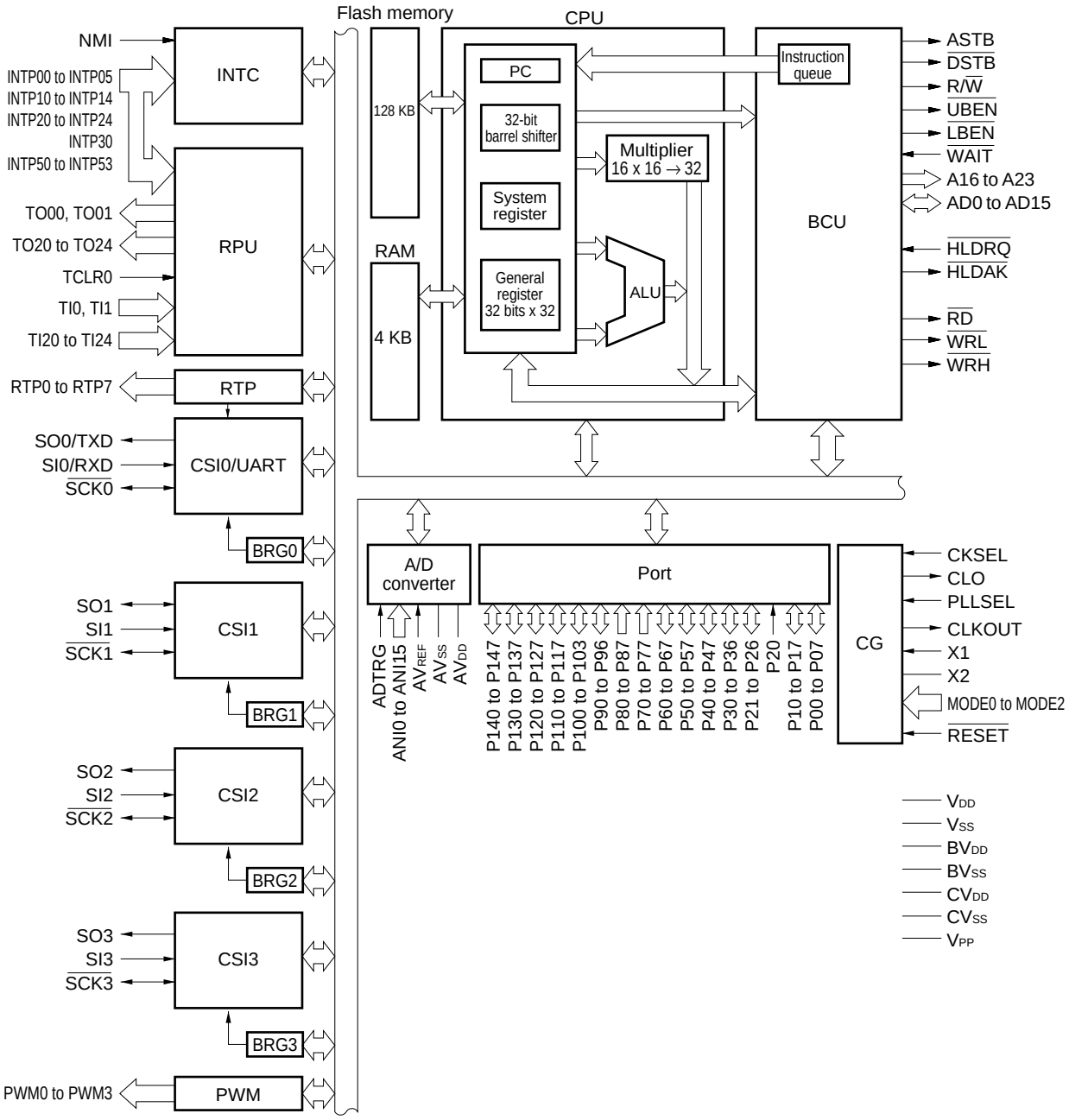
2. Connect to V_{SS} via a resistor (R_{VPP}) during normal operation mode.

3. Connect directly to V_{SS} in normal operation mode.

PIN IDENTIFICATION

A16 to A23 : Address Bus
AD0 to AD15 : Address/Data Bus
ADTRG : AD Trigger Input
ANI0 to ANI15 : Analog Input
ASTB : Address Strobe
AV_{DD} : Analog V_{DD}
AV_{REF} : Analog Reference Voltage
AV_{SS} : Analog V_{SS}
BV_{DD} : Power Supply for Bus Interface
BV_{SS} : Ground for Bus Interface
CKSEL : Clock Select
CLKOUT : Clock Output
CLO : Clock Output (Divided)
CV_{DD} : Power Supply for Clock Generator
CV_{SS} : Ground for Clock Generator
$\overline{DSTB}$: Data Strobe
$\overline{HLDAK}$: Hold Acknowledge
$\overline{HLDRQ}$: Hold Request
INTP00 to INTP05, INTP10 to INTP14, INTP20 to INTP24, INTP30, INTP50 to INTP53 : Interrupt Request from Peripherals
$\overline{LBEN}$: Lower Byte Enable
MODE0 to MODE2 : Mode
NMI : Non-maskable Interrupt Request
P00 to P07 : Port0
P10 to P17 : Port1
P20 to P26 : Port2
P30 to P36 : Port3
P40 to P47 : Port4
P50 to P57 : Port5
P60 to P63 : Port6
P70 to P77 : Port7
P80 to P87 : Port8
P90 to P96 : Port9
P100 to P103 : Port10
P110 to P117 : Port11
P120 to P127 : Port12
P130 to P137 : Port13
P140 to P147 : Port14
PLLSEL : PLL Select
PWM0 to PWM3 : Pulse Width Modulation
$\overline{RD}$: Read
$\overline{RESET}$: Reset
RTP0 to RTP7 : Real-time Port
R/$\overline{W}$: Read/Write Status
RXD : Receive Data
$\overline{SCK0}$ to $\overline{SCK3}$: Serial Clock
SI0 to SI3 : Serial Input
SO0 to SO3 : Serial Output
TCLR0 : Timer Clear
TI0, TI1, TI20 to TI24 : Timer Input
TO00, TO01, TO20 to TO24 : Timer Output
TXD : Transmit Data
$\overline{UBEN}$: Upper Byte Enable
V_{DD} : Power Supply
V_{PP} : Programming Power Supply
V_{SS} : Ground
$\overline{WAIT}$: Wait
$\overline{WRH}$: Write Strobe High Level Data
$\overline{WRL}$: Write Strobe Low Level Data
X1, X2 : Crystal

INTERNAL BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD703008 AND μPD70F3008

Parameter \ Part Number	μPD703008	μPD70F3008
Internal ROM	Mask ROM	Flash memory
Flash memory programming pin	None	Provided (V_{PP})
Flash memory programming mode	None	Provided (V_{PP} = 7.5 V, Mode0 to Mode2 = High-level)
Electrical specifications	Current consumption, etc. differ. (Refer to each product data sheet.)	
Others	Nose immunity and noise radiation are different because products differ in circuit size and mask layout.	

Cautions 1. There are differences in noise immunity and noise radiation between the PROM version and mask ROM version. When pre-producing an application set with the PROM version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluations for the set using consumer samples (not engineering samples) of the mask ROM version.

2. When replacing a flash memory version with a mask ROM version, be sure to write the same code into the internal ROM's reserved area.

2. PIN FUNCTIONS

2.1 Port Pins

(1/2)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0.	TO00
P01		8-bit I/O port.	TO01
P02		Input/output can be specified in 1-bit units.	INTP00
P03			INTP01
P04			INTP02
P05			INTP03
P06			TCLR0/INTP04
P07			TI0/INTP05
P10	I/O	Port 1.	INTP10
P11		8-bit I/O port.	INTP11
P12		Input/output can be specified in 1-bit units.	INTP12
P13			INTP13
P14			TI1/INTP14
P15			TO20
P16			TI20/INTP20
P17			–
P20	Input	Port 2.	NMI
P21	I/O	P20 is an input-only port.	INTP30
P22		• P20 functions as an NMI input after a valid edge is input.	ADTRG
P23		• Bit 0 of P2 register indicates the NMI input status.	INTP50
P24		P21 to P26 are a 6-bit I/O port.	INTP51
P25		• Input/output can be specified in 1-bit units.	INTP52
P26			INTP53
P30	I/O	Port 3.	SO0/TXD
P31		7-bit I/O port.	SI0/RXD
P32		Input/output can be specified in 1-bit units.	$\overline{\text{SCK0}}$
P33			SO1
P34			SI1
P35			$\overline{\text{SCK1}}$
P36			–
P40 to P47	I/O	Port 4. 8-bit I/O port. Input/output can be specified in 1-bit units.	AD0 to AD7
P50 to P57	I/O	Port 5. 8-bit I/O port. Input/output can be specified in 1-bit units.	AD8 to AD15

(2/2)

Pin Name	I/O	Function	Alternate Function
P60 to P67	I/O	Port 6. 8-bit I/O port. Input/output can be specified in 1-bit units.	A16 to A23
P70 to P77	Input	Port 7. 8-bit input-only port.	ANI0 to ANI7
P80 to P87	Input	Port 8. 8-bit input-only port.	ANI8 to ANI15
P90	I/O	Port 9. 7-bit I/O port. Input/output can be specified in 1-bit units.	$\overline{\text{LBEN}}$/$\overline{\text{WRL}}$
P91			$\overline{\text{UBEN}}$
P92			R/$\overline{\text{W}}$/$\overline{\text{WRH}}$
P93			$\overline{\text{DSTB}}$/$\overline{\text{RD}}$
P94			ASTB
P95			$\overline{\text{HLDAK}}$
P96			$\overline{\text{HLDRQ}}$
P100 to P103	I/O	Port 10. 4-bit I/O port. Input/output can be specified in 1-bit units.	PWM0 to PMW3
P110	I/O	Port 11. 8-bit I/O port. Input/output can be specified in 1-bit units.	TO21
P111			TI21/INTP21
P112			TO22
P113			TI22/INTP22
P114			TO23
P115			TI23/INTP23
P116			TO24
P117			TI24/INTP24
P120	I/O	Port 12. 8-bit I/O port. Input/output can be specified in 1-bit units.	SO2
P121			SI2
P122			$\overline{\text{SCK2}}$
P123			SO3
P124			SI3
P125			$\overline{\text{SCK3}}$
P126			–
P127			CLO
P130 to P137	I/O	Port 13. 8-bit I/O port. Input/output can be specified in 1-bit units.	RTP0 to RTP7
P140 to P147	I/O	Port 14. 8-bit I/O port. Input/output can be specified in 1-bit units.	–

2.2 Non-port Pins

(1/3)

Pin Name	I/O	Function	Alternate Function
TO00	Output	Pulse signal output from timers 0 and 2.	P00
TO01			P01
TO20			P15
TO21			P110
TO22			P112
TO23			P114
TO24			P116
TCLR0	Input	External clear signal input to timer 0.	P06/INTP04
TI0	Input	External count clock input to timers 0, 1, and 2.	P07/INTP05
TI1			P14/INTP14
TI20			P16/INTP20
TI21			P111/INTP21
TI22			P113/INTP22
TI23			P115/INTP23
TI24			P117/INTP24
INTP00 to INTP03	Input	External capture trigger input to timer 0. Also used to input external maskable interrupt request.	P02 to P05
INTP04	Input	External maskable interrupt request input.	P06/TCLR0
INTP05			P07/TI0
INTP10 to INTP13	Input	External capture trigger input to timer 1. Also used to input external maskable interrupt request.	P10 to P13
INTP14	Input	External maskable interrupt request input.	P14/TI1
INTP20	Input	External maskable interrupt request input.	P16/TI20
INTP21			P111/TI21
INTP22			P113/TI22
INTP23			P115/TI23
INTP24			P117/TI24
INTP30	Input	External capture trigger input to timer 3. Also used to input external maskable interrupt request.	P21
INTP50 to INTP53	Input	External maskable interrupt request input.	P23 to P26
NMI	Input	Non-maskable interrupt request input.	P20
AD0 to AD7	I/O	16-bit multiplexed address/data bus when external memory is used.	P40 to P47
AD8 to AD15			P50 to P57
A16 to A23	Output	Higher address bus when external memory is used.	P60 to P67
$\overline{\text{LBEN}}$	Output	Lower byte enable signal output of external data bus.	P90/$\overline{\text{WRL}}$
$\overline{\text{UBEN}}$		Higher byte enable signal output of external data bus.	P91
R/$\overline{\text{W}}$		External read/write status output.	P92/$\overline{\text{WRH}}$
$\overline{\text{DSTB}}$		External data strobe signal output.	P93/$\overline{\text{RD}}$
ASTB		External address strobe signal output.	P94

(2/3)

Pin Name	I/O	Function	Alternate Function
$\overline{\text{HLDAK}}$	Output	Bus hold acknowledge output.	P95
$\overline{\text{HLDRQ}}$	Input	Bus hold request input.	P96
SO0	Input	Serial transmit data output from CSI0 to CSI3 (3-wire).	P30/TXD
SO1			P33
SO2			P120
SO3			P123
SI0	Input	Serial receive data input to CSI0 to CSI3 (3-wire).	P31/RXD
SI1			P34
SI2			P121
SI3			P124
$\overline{\text{SCK0}}$	I/O	Serial clock I/O from/to CSI0 to CSI3 (3-wire).	P32
$\overline{\text{SCK1}}$			P35
$\overline{\text{SCK2}}$			P122
$\overline{\text{SCK3}}$			P125
TXD	Output	Serial transmit data output from UART.	P30/SO0
RXD	Input	Serial receive data input to UART.	P31/SI0
PWM0 to PWM3	Output	Pulse signal output from PWM.	P100 to P103
$\overline{\text{WRL}}$	Output	Lower byte of external data bus write strobe signal output.	P90/$\overline{\text{LBEN}}$
$\overline{\text{WRH}}$		Higher byte of external data bus write strobe signal output.	P92/R/$\overline{\text{W}}$
$\overline{\text{RD}}$	Output	External data bus read strobe signal output.	P93/$\overline{\text{DSTB}}$
ANI0 to ANI7	Input	Analog input to A/D converter.	P70 to P77
ANI8 to ANI15			P80 to P87
RTP0 to RTP7	Output	Real time output port.	P130 to P137
CLO	Output	System clock output (with frequency division function).	P127
CKSEL	Input	Input to specify clock generator operation mode.	–
PLLSEL	Input	Input to specify the number of PLL multiplication.	–
CLKOUT	Output	System clock output.	–
$\overline{\text{WAIT}}$	Input	Control signal input inserting wait state to bus cycle.	–
MODE0 to MODE2	Input	Specifies operation mode.	–
$\overline{\text{RESET}}$	Input	System reset input.	–
X1	Input	System clock oscillator connecting pins. Supply external clock to X1.	–
X2	–		–

(3/3)

Pin Name	I/O	Function	Alternate Function
ADTRG	Input	A/D converter external trigger input.	P22
AV_{REF}	Input	Reference voltage input for A/D converter.	–
AV_{DD}	–	Positive power supply for A/D converter.	–
AV_{SS}	–	Ground for A/D converter.	–
BV_{DD}	–	Positive power supply for bus interface.	–
BV_{SS}	–	Ground for bus interface.	–
CV_{DD}	–	Positive power supply for clock generator.	–
CV_{SS}	–	Ground for clock generator.	–
V_{DD}	–	Positive power supply.	–
V_{SS}	–	Ground.	–
V_{PP}	–	High-voltage pin for program write/verify.	–

2.3 I/O Circuit of Pins and Recommended Connections of Unused Pins

Table 2-1 shows the I/O circuit type for each pin and the recommended connections for all unused pins. Figure 2-1 shows partially simplified pin I/O circuits.

When connecting a pin to V_{DD} or V_{SS} via a resistor, use of a resistor of 1 to 10 kΩ is recommended.

Table 2-1. I/O Circuit Type of Each Pin and Recommended Connections of Unused Pins (1/2)

Pin	I/O Circuit Type	Recommended Connections
P00/TO00, P01/TO01	5	Individually connect to V_{DD} or V_{SS} via resistor.
P02/INTP00 to P05/INTP03, P06/TCLR0/INTP04, P07/TI0/INTP05	5-K	
P10/INTP10 to P13/INTP13, P14/TI1/INTP14, P16/TI20/INTP20		
P15/TO20, P17	5	
P20/NMI	2	Connect directly to V_{SS}.
P21/INTP30, P22/ADTRG, P23/INTP50 to P26/INTP53	5-K	Individually connect to V_{DD} or V_{SS} via resistor.
P30/TXD/SO0	5	
P31/RXD/SI0, P32/$\overline{SCK0}$, P34/SI1	5-K	
P33/SO1, P35/$\overline{SCK1}$	13-G	
P36	5	
P40/AD0 to P47/AD7	5[Note]	Individually connect to BV_{DD} or BV_{SS} via resistor.
P50/AD8 to P57/AD15		
P60/A16 to P67/A23		
P70/ANI0 to P77/ANI7	9	Connect directly to V_{SS}.
P80/ANI8 to P87/ANI15		
P90/$\overline{LBEN}$/$\overline{WRL}$, P91/$\overline{UBEN}$, P92/R/$\overline{W}$/$\overline{WRH}$, P93/$\overline{DSTB}$/$\overline{RD}$, P94/ASTB, P95/$\overline{HLDAK}$, P96/$\overline{HLDRQ}$	5[Note]	Individually connect to BV_{DD} or BV_{SS} via resistor.
P100/PWM0 to P103/PWM3	5	Individually connect to V_{DD} or V_{SS} via resistor.
P110/TO21, P112/TO22, P114/TO23, P116/TO24		
P111/TI21/INTP21, P113/TI22/INTP22, P115/TI23/INTP23, P117/TI24/INTP24	5-K	
P120/SO2	5	
P121/SI2, P122/$\overline{SCK2}$	5-K	
P123/SO3	5	
P124/SI3, P125/$\overline{SCK3}$	5-K	
P126, P127/CLO	5	
P130/RTP0 to P137/RTP7		
P140 to P147		

Remark Open input is possible for I/O circuit types 5, 5-K. and 13-G pins.

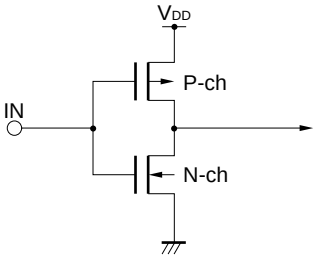
Table 2-1. I/O Circuit Type of Each Pin and Recommended Connections of Unused Pins (2/2)

Pin	I/O Circuit Type	Recommended Connections
$\overline{WAIT}$	1[Note]	Connect directly to BV_{DD}.
CLKOUT	3[Note]	Open.
MODE0 to MODE2	2	Individually connect to V_{DD} or V_{SS} via resistor.
$\overline{RESET}$		–
AV_{REF}, AV_{SS}, CV_{SS}	–	Connect directly to V_{SS}.
AV_{DD}, CV_{DD}	–	Connect directly to V_{DD}.
PLLSEL	1	Connect directly to V_{DD} or V_{SS}.
CKSEL	1	
V_{PP}	–	Individually connect to V_{SS} via resistor (R_{VPP}).

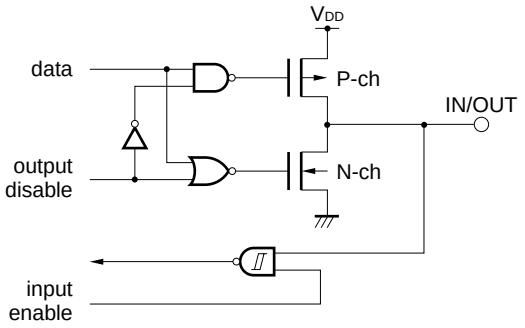
Note Read V_{DD} as BV_{DD} when referring to the I/O circuit diagram.

Figure 2-1. Pin I/O Circuits

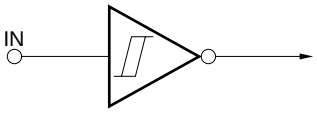
Type 1



Type 5-K

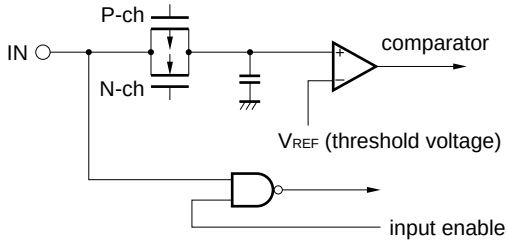


Type 2

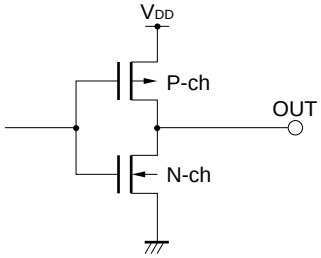


Schmitt trigger input with hysteresis characteristics

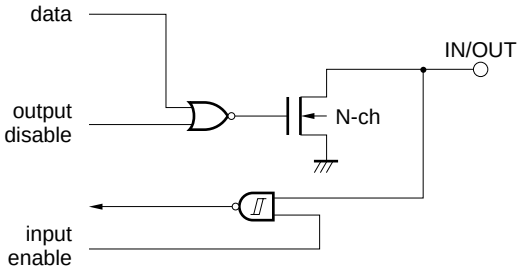
Type 9



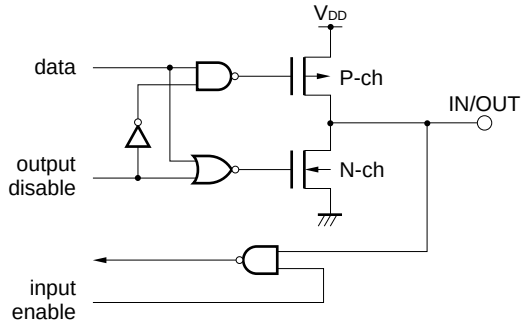
Type 3



Type 13-G



Type 5



3. FLASH MEMORY PROGRAMMING

There are the following two methods for writing a program to the flash memory.

(1) On-board programming

Write a program to the flash memory using a dedicated flash programmer after the μPD70F3008 has been mounted on the target board. Also mount a connector, etc. on the target board to communicate with the dedicated flash programmer.

(2) Off-board programming

Write a program using a dedicated adapter before the μPD70F3008 has been mounted on the target board.

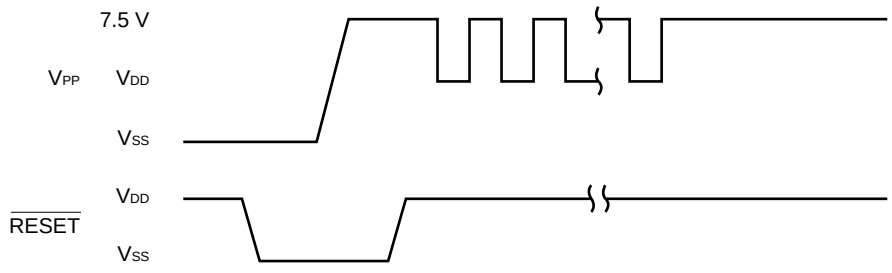
3.1 Selecting Communication Mode

To write the flash memory, use a dedicated flash programmer and serial communication. Select a serial communication mode from those listed in Table 3-1 in the format shown in Figure 3-1. Each communication mode is selected by the number of V_{PP} pulses shown in Table 3-1.

Table 3-1. Communication Modes

Communication Mode	Pins Used	Number of V_{PP} Pulses
CSI0	$\overline{SCK0}$ (serial clock input) SO0 (serial data output) SI0 (serial data input)	0
CSI2	$\overline{SCK2}$ (serial clock input) SO2 (serial data output) SI2 (serial data input)	2
UART	TXD (serial data output) RXD (serial data input)	8

Figure 3-1. Communication Mode Selecting Format



3.2 Flash Memory Programming Function

The flash memory is written by transmitting or receiving commands and data in a selected communication mode. The major functions of flush memory programming are listed in Table 3-2.

Table 3-2. Major Functions of Flash Memory Programming

Function	Description
Batch erasure	Erases all contents of memory.
Block erasure	Erases contents of memory in 4 Kbytes.
Batch blank check	Checks erased status of entire memory.
Data write	Writes flash memory based on write start address and number of data to be written (in bytes).
Batch verify	Compares all contents of memory with input data.

3.3 Connecting Dedicated Flash Programmer

The dedicated flash programmer and μPD70F3008 are connected differently depending on the selected communication mode. Figures 3-2 and 3-3 show the connections in the respective communication modes.

Figure 3-2. Connection of Dedicated Flash Programmer in UART Mode

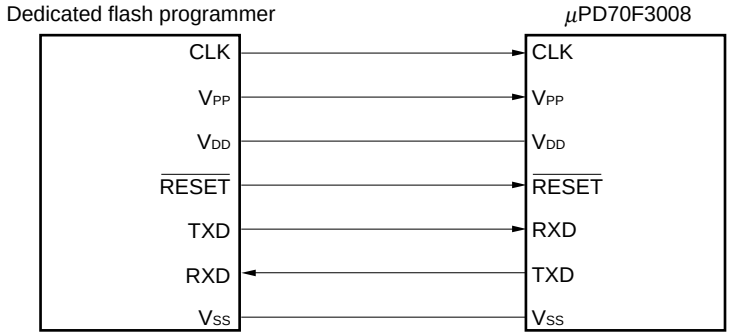
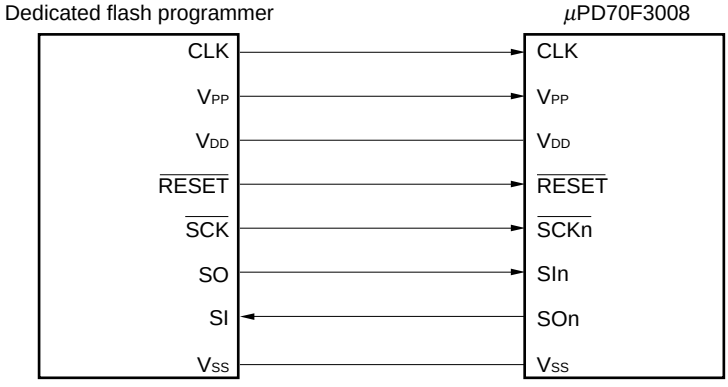


Figure 3-3. Connection of Dedicated Flash Programmer in CSI Mode



Remark n = 0, 2

4. ELECTRICAL SPECIFICATIONS

4.1 Normal Operating Mode

Absolute Maximum Ratings (T_A = 25°C)

Parameter	Symbol	Condition	Ratings	Unit
Supply voltage	V_{DD}	V_{DD} pin	–0.5 to +4.6	V
	AV_{DD}	AV_{DD} pin	–0.5 to +4.6	V
	BV_{DD}	BV_{DD} pin	–0.5 to +4.6	V
	CV_{DD}	CV_{DD} pin	–0.5 to +4.6	V
	V_{SS}	V_{SS} pin	–0.5 to +0.5	V
	AV_{SS}	AV_{SS} pin	–0.5 to +0.5	V
	BV_{SS}	BV_{SS} pin	–0.5 to +0.5	V
	CV_{SS}	CV_{SS} pin	–0.5 to +0.5	V
Input voltage	V_{I1}	Except for X1 pin, V_{DD} = 2.7 to 3.6 V	–0.5 to V_{DD} + 0.5	V
	V_{I2}	V_{PP} pin in flash memory programming mode	–0.5 to +10.0	V
Clock input voltage	V_K	X1 pin, V_{DD} = 2.7 to 3.6 V	–0.5 to V_{DD} + 1.0	V
Output current, low	I_{OL}	1 pin	4.0	mA
		Total of all pins	100	mA
Output current, high	I_{OH}	1 pin	–4.0	mA
		Total of all pins	–100	mA
Output voltage	V_O	V_{DD} = 2.7 to 3.6 V	–0.5 to V_{DD} + 0.5	V
Operating ambient temperature	T_A		–40 to +85	°C
Storage temperature	T_{stg}		–65 to +150	°C

Cautions 1. Do not directly connect the output (or I/O) pins of two or more IC products, and do not directly connect them to V_{DD}, V_{CC}, or GND pin. Open-drain pins and open-collector pins may be directly connected to one another however. Moreover, an external circuit that is designed to prevent contention of output can be connected to pins that go into a high-impedance state.

2. Should the absolute maximum rating of even one of the above parameters be exceeded even momentarily, the quality of the program may be degraded. The absolute maximum ratings are, therefore, the values exceeding which the product may be physically damaged. Use the product so that these values are never exceeded.

The normal operating ranges of ratings and conditions in which the quality of the product is guaranteed are specified in the following DC Characteristics and AC Characteristics.

Capacitance (T_A = 25°C, V_{DD} = V_{SS} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fc = 1 MHz			15	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V.			15	pF
Output capacitance	C_O				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (ϕ)	Operating Ambient Temperature (T_A)	Supply Voltage (V_{DD})
Direct mode	0 to 33 MHz	–40 to +85°C	2.7 to 3.6 V
PLL mode	Free-running oscillation frequency to 33 MHz	–40 to +85°C	2.7 to 3.6 V

DC Characteristics [Note 1] **(T_A = –40 to +85°C, V_{DD} = CV_{DD} = 2.7 to 3.6 V, V_{SS} = AV_{SS} = BV_{SS} = CV_{SS} = 0 V)**

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage, high		V_{IH}		$0.7V_{DD}$		V_{DD} + 0.3	V
Input voltage, low		V_{IL}		–0.3		$0.2V_{DD}$	V
Clock input voltage, high		V_{KH}	X1	$0.8V_{DD}$		V_{DD} + 0.3	V
Clock input voltage, low		V_{KL}	X1	–0.3		$0.15V_{DD}$	V
Schmitt trigger input threshold voltage		V_{T^+}	**Note 2**, rising		**Note 3**		V
		V_{T^-}	**Note 2**, falling		**Note 3**		V
Schmitt trigger input hysteresis width		$V_{T^+} – V_{T^-}$	**Note 2**	**Note 3**			V
Output voltage, high		V_{OH}	I_{OH} = –2.5 mA	$0.8V_{DD}$			V
Output voltage, low		V_{OL}	I_{OL} = 2.5 mA			$0.15V_{DD}$	V
Input leakage current, high		I_{LIH}	$V_I = V_{DD}$			5	μA
Input leakage current, low		I_{LIL}	V_I = 0 V			–5	μA
Output leakage current, high		I_{LOH}	$V_O = V_{DD}$			5	μA
Output leakage current, low		I_{LOL}	V_O = 0 V			–5	μA
Supply current	Operating	I_{DD}			**Note 3**	**Note 3**	mA
	In HALT mode				**Note 3**	**Note 3**	mA
	In IDLE mode				**Note 3**	**Note 3**	μA
	In STOP mode				**Note 3**	**Note 3**	μA

Notes 1. For the following pins, the parameter V_{DD} in the above table should be read and referred to as BV_{DD} (on condition of 2.0 V ≤ BV_{DD} ≤ V_{DD}).
P40/AD0 to P47/AD7, P50/AD8 to P57/AD15, P60/A16 to P67/A23. P90/$\overline{LBE}$/$\overline{WRL}$, P91/$\overline{UBE}$, P92/R/$\overline{W}$/$\overline{WRH}$, P93/$\overline{DSTB}$/$\overline{RD}$, P94/ASTB, P95/$\overline{HLDAK}$, P96/$\overline{HLDRQ}$, CLKOUT, $\overline{WAIT}$

2. P02/INTP00 to P05/INTP03, P06/TCLR0/INTP04, P07/TI0/INTP05, P10/INTP10, P11/INTP11, P12/INTP12, P13/INTP13, P14/TI1/INTP14, P16/TI20/INTP20, P111/TI21/INTP21, P113/TI22/INTP22, P115/TI23/INTP23, P117/TI24/INTP24, P21/INTP30, P22/ADTRG, P23/INTP50, P24/INTP51, P25/INTP52, P26/INTP53, P31/RXD/SI0, P32/$\overline{SCK0}$, P33/SO1, P34/SI1, P35/$\overline{SCK1}$, P121/SI2, P122/$\overline{SCK2}$, P124/SI3, P125/$\overline{SCK3}$, MODE0 to MODE2, $\overline{RESET}$, P20/NMI

3. Under evaluation

Remarks 1. TYP. value is a value for your reference at T_A = 25°C and V_{DD} = 3.0 V.

2. ϕ : Internal operating clock frequency

Data Retention Characteristics (T_A = –40 to +85°C)

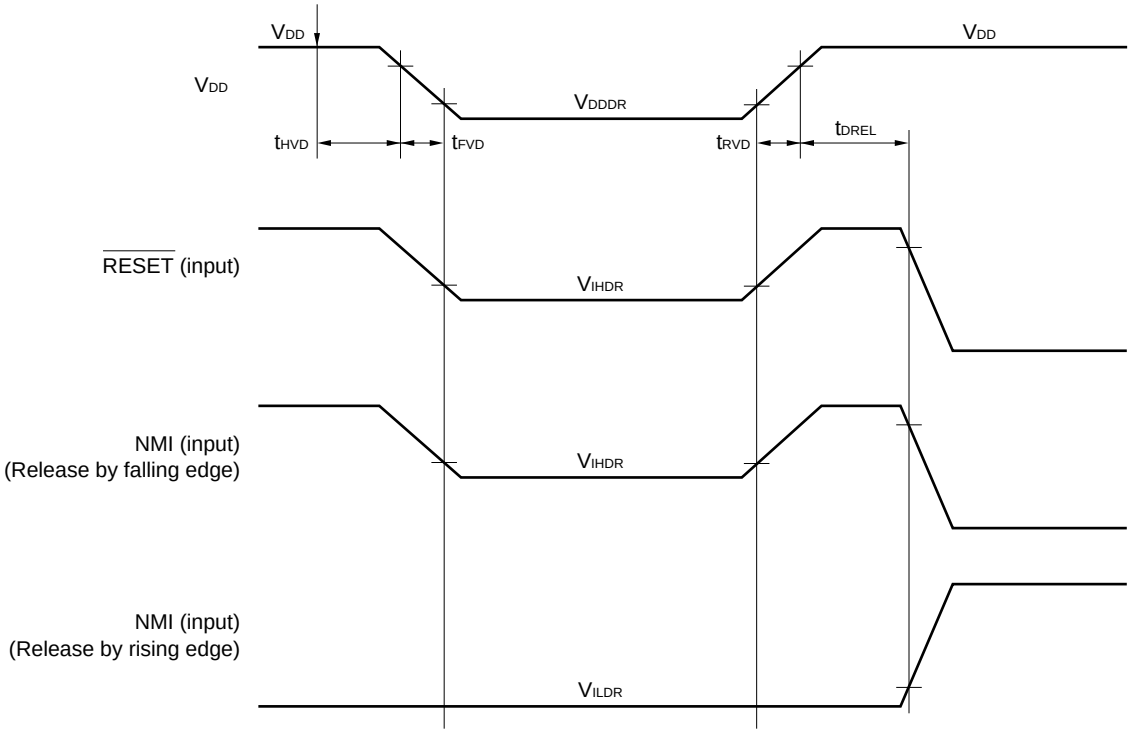
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Data hold voltage	V_{DDDR}	STOP mode	1.5		3.6	V
Data hold current	I_{DDDR}	$V_{DD} = V_{DDDR}$		**Note 1**	**Note 1**	μA
Supply voltage rise time	t_{RVD}		200			μs
Supply voltage fall time	t_{FVD}		200			μs
Supply voltage hold time (from STOP mode setting)	t_{HVD}		0			ms
STOP mode release signal input time	t_{DREL}		0			ns
Data hold input high-level voltage	V_{IHDR}	**Note 2**	$0.9V_{DDDR}$		V_{DDDR}	V
Data hold input low-level voltage	V_{ILDR}	**Note 2**	0		$0.1V_{DDDR}$	V

Notes 1. Under evaluation

2. P02/INTP00 to P05/INTP03, P06/TCLR0/INTP04, P07/TI0/INTP05, P10/INTP10, P11/INTP11, P12/INTP12, P13/INTP13, P14/TI1/INTP14, P16/TI20/INTP20, P111/TI21/INTP21, P113/TI22/INTP22, P115/TI23/INTP23, P117/TI24/INTP24, P21/INTP30, P22/ADTRG, P23/INTP50, P24/INTP51, P25/INTP52, P26/INTP53, P31/RXD/SI0, P32/$\overline{SCK0}$, P33/SO1, P34/SI1, P35/$\overline{SCK1}$, P121/SI2, P122/$\overline{SCK2}$, P124/SI3, P125/$\overline{SCK3}$, MODE0 to MODE2, $\overline{RESET}$, P20/NMI

Remark TYP. value is a value for your reference at T_A = 25°C.

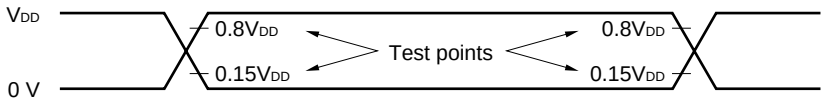
STOP mode is set (at fifth clock after PSC register has been set).



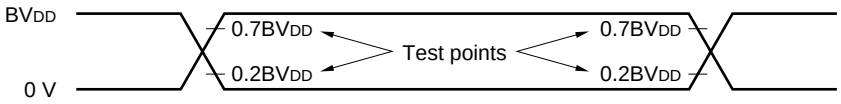
AC Characteristics (T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = CV_{DD} = 2.7 to 3.6V, V_{SS} = AV_{SS} = BV_{SS} = CV_{SS} = 0 V)

AC test input wave

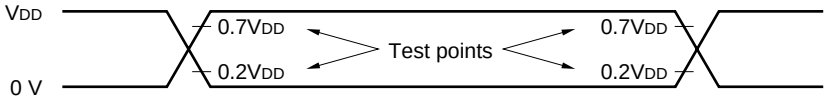
(a) P02/INTP00 to P05/INTP03, P06/TCLR0/INTP04, P07/TI0/INTP05, P10/INTP10, P11/INTP11, P12/INTP12, P13/INTP13, P14/TI1/INTP14, P16/TI20/INTP20, P111/TI21/INTP21, P113/TI22/INTP22, P115/TI23/INTP23, P117/TI24/INTP24, P21/INTP30, P22/ADTRG, P23/INTP50, P24/INTP51, P25/INTP52, P26/INTP53, P31/RXD/SI0, P32/$\overline{\text{SCK0}}$, P33/SO1, P34/SI1, P35/$\overline{\text{SCK1}}$, P121/SI2, P122/$\overline{\text{SCK2}}$, P124/SI3, P125/$\overline{\text{SCK3}}$, MODE0 to MODE2, $\overline{\text{RESET}}$, P20/NMI



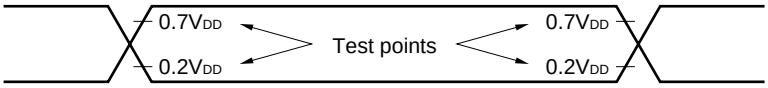
(b) P40/AD0 to P47/AD7, P50/AD8 to P57/AD15, P60/A16 to P67/A23, P90/$\overline{\text{LBE}}$/$\overline{\text{WRL}}$, P91/$\overline{\text{UBE}}$, P92/R/$\overline{\text{W}}$/$\overline{\text{WRH}}$, P93/$\overline{\text{DSTB}}$/$\overline{\text{RD}}$, P94/ASTB, P95/$\overline{\text{HLDAK}}$, P96/$\overline{\text{HLDRQ}}$, CLKOUT, $\overline{\text{WAIT}}$



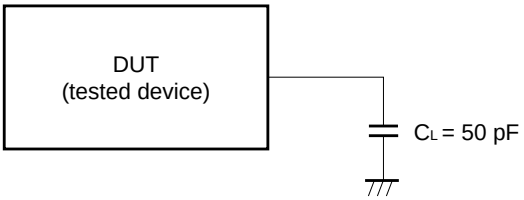
(c) Other than (a) and (b)



AC test output test point



Load condition



Caution If the loaded capacitance exceeds 50 pF due to the circuit configuration, decrease the load capacitance of this device to less than 50 pF by using a buffer.

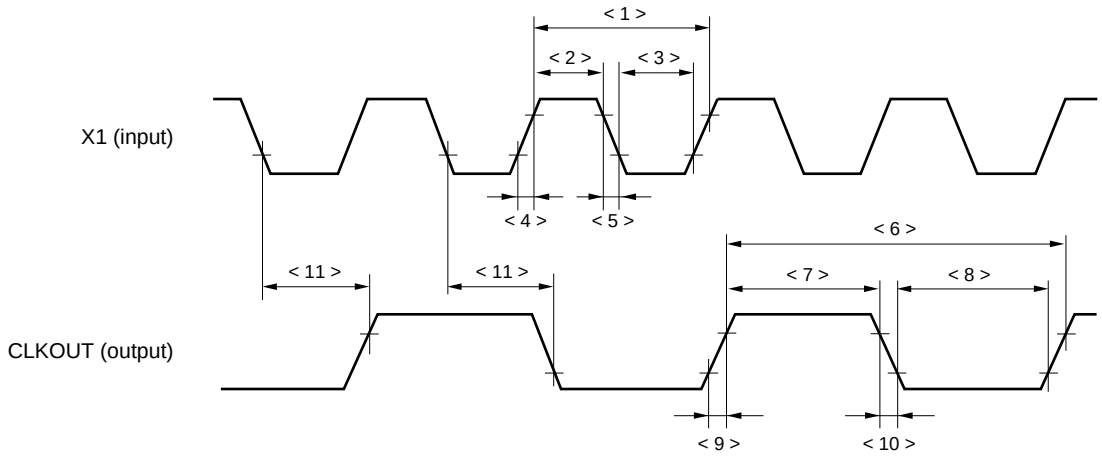
(1) Clock timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
X1 input cycle	<1>	t_{CYX}	Direct mode	15	DC	ns
			PLL mode ($f_{XX} = \phi/5$)	150	**Note**	ns
			PLL mode ($f_{XX} = \phi$)	30	**Note**	ns
X1 input high-level width	<2>	t_{WXH}	Direct mode	4		ns
			PLL mode ($f_{XX} = \phi/5$)	50		ns
			PLL mode ($f_{XX} = \phi$)	10		ns
X1 input low-level width	<3>	t_{WXL}	Direct mode	4		ns
			PLL mode ($f_{XX} = \phi/5$)	50		ns
			PLL mode ($f_{XX} = \phi$)	10		ns
X1 input rise time	<4>	t_{XR}	Direct mode		5	ns
			PLL mode ($f_{XX} = \phi/5$)		15	ns
			PLL mode ($f_{XX} = \phi$)		5	ns
X1 input fall time	<5>	t_{XF}	Direct mode		5	ns
			PLL mode ($f_{XX} = \phi/5$)		15	ns
			PLL mode ($f_{XX} = \phi$)		5	ns
CPU operating frequency	—	ϕ		0	33	MHz
CLKOUT output cycle	<6>	t_{CYK}		30	DC	ns
CLKOUT high-level width	<7>	t_{WKH}		0.5T – 5		ns
CLKOUT low-level width	<8>	t_{WKL}		0.5T – 5		ns
CLKOUT rise time	<9>	t_{KR}			5	ns
CLKOUT fall time	<10>	t_{KF}			5	ns
CLKOUT delay time from X1 ↓	<11>	t_{DXK}	Direct mode	3	17	ns

Note Under evaluation

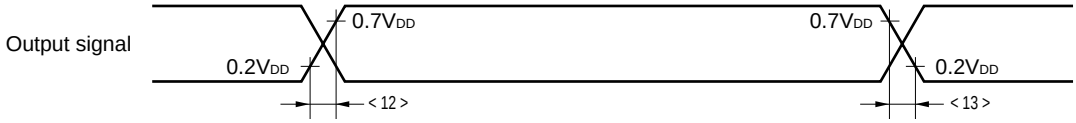
Remark T = t_{CYK}

Parameter	Symbol		Condition	TYP.	Unit
Free-running oscillation frequency	—	ϕ_P	PLL mode	Under evaluation	MHz



(2) Output wave (other than X1, CLKOUT)

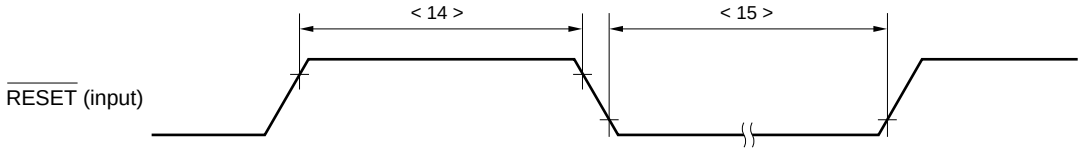
Parameter	Symbol		Condition	MIN.	MAX.	Unit
Output rise time	<12>	t_{OR}			10	ns
Output fall time	<13>	t_{OF}			10	ns



(3) Reset timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width	<14>	t_{WRSH}		500		ns
$\overline{\text{RESET}}$ low-level width	<15>	t_{WRSL}	On power application, or on releasing STOP mode	500 + T_{OS}		ns
			Except on power application or except on releasing STOP mode	500		ns

Remark T_{OS}: oscillation stabilization time



[MEMO]

(4) Read timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CLKOUT ↑→ address delay time	<16>	t_{DKA}		3	14	ns
CLKOUT ↑→ address float delay time	<17>	t_{FKA}		t_{DKA}	17	ns
CLKOUT ↓→ ASTB delay time	<18>	t_{DKST}		3	14	ns
CLKOUT ↓→ $\overline{\text{DSTB}}$ delay time	<19>	t_{DKD}		3	14	ns
Data input setup time (to CLKOUT ↑)	<20>	t_{SIDK}		5		ns
Data input hold time (from CLKOUT ↑)	<21>	t_{HKID}		5		ns
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<22>	t_{SWTK}		5		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<23>	t_{HKWT}		5		ns
Address setup time (to ASTB ↓)	<24>	t_{SAST}		0.5T – 10		ns
Address hold time (from ASTB ↓)	<25>	t_{HSTA}		0.5T – 10		ns
$\overline{\text{DSTB}}$ ↓→ address float delay time	<26>	t_{FDA}			0	ns
Data input setup time (to address)	<27>	t_{SAID}			(2 + n)T – 17	ns
Data input setup time (from $\overline{\text{DSTB}}$ ↓)	<28>	t_{SDID}			(1 + n)T – 17	ns
ASTB ↓→ $\overline{\text{DSTB}}$ ↓ delay time	<29>	t_{DSTD}		0.5T – 10		ns
Data input hold time (from $\overline{\text{DSTB}}$ ↑)	<30>	t_{HDID}		0		ns
$\overline{\text{DSTB}}$ ↑→ address output delay time	<31>	t_{DDA}		(1 + i)T		ns
$\overline{\text{DSTB}}$ ↑→ ASTB ↑ delay time	<32>	t_{DDST1}		0.5T – 10		ns
$\overline{\text{DSTB}}$ ↑→ ASTB ↓ delay time	<33>	t_{DDST2}		(1.5 + i)T – 10		ns
$\overline{\text{DSTB}}$ low-level width	<34>	t_{WDL}		(1 + n)T – 10		ns
ASTB high-level width	<35>	t_{WSTH}		T – 10		ns
$\overline{\text{WAIT}}$ setup time (to address)	<36>	t_{SAWT1}	n ≥ 1		1.5T – 15	ns
	<37>	t_{SAWT2}			(1.5 + n)T – 15	ns
$\overline{\text{WAIT}}$ hold time (from address)	<38>	t_{HAWT1}	n ≥ 1	(0.5 + n)T		ns
	<39>	t_{HAWT2}		(1.5 + n)T		ns
$\overline{\text{WAIT}}$ setup time (to ASTB ↓)	<40>	t_{SSTWT1}	n ≥ 1		T – 15	ns
	<41>	t_{SSTWT2}			(1 + n)T – 15	ns
$\overline{\text{WAIT}}$ hold time (from ASTB ↓)	<42>	t_{HSTWT1}	n ≥ 1	nT		ns
	<43>	t_{HSTWT2}		(1 + n)T		ns

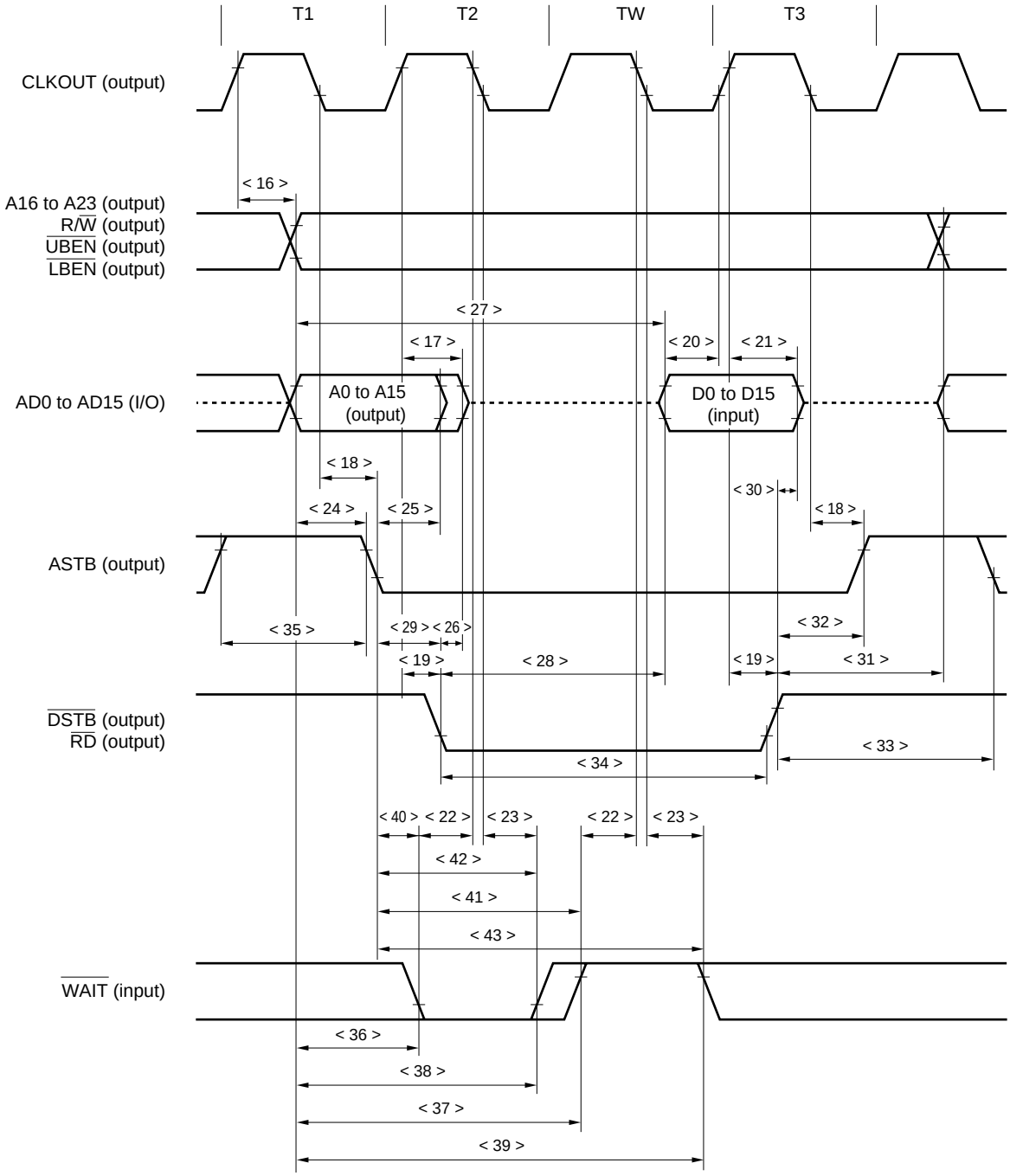
Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

3. i indicates the number of idle states (0 or 1) to be inserted in the read cycle.

4. Be sure to observe at least one of data input hold times t_{HKID} (<21>) and t_{HDID} (<30>).

(4) Read Timing (2/2): 1 wait



Remarks 1. $\overline{WRL}$, $\overline{WRH}$: High-level output
2. The broken line indicates the high-impedance state.

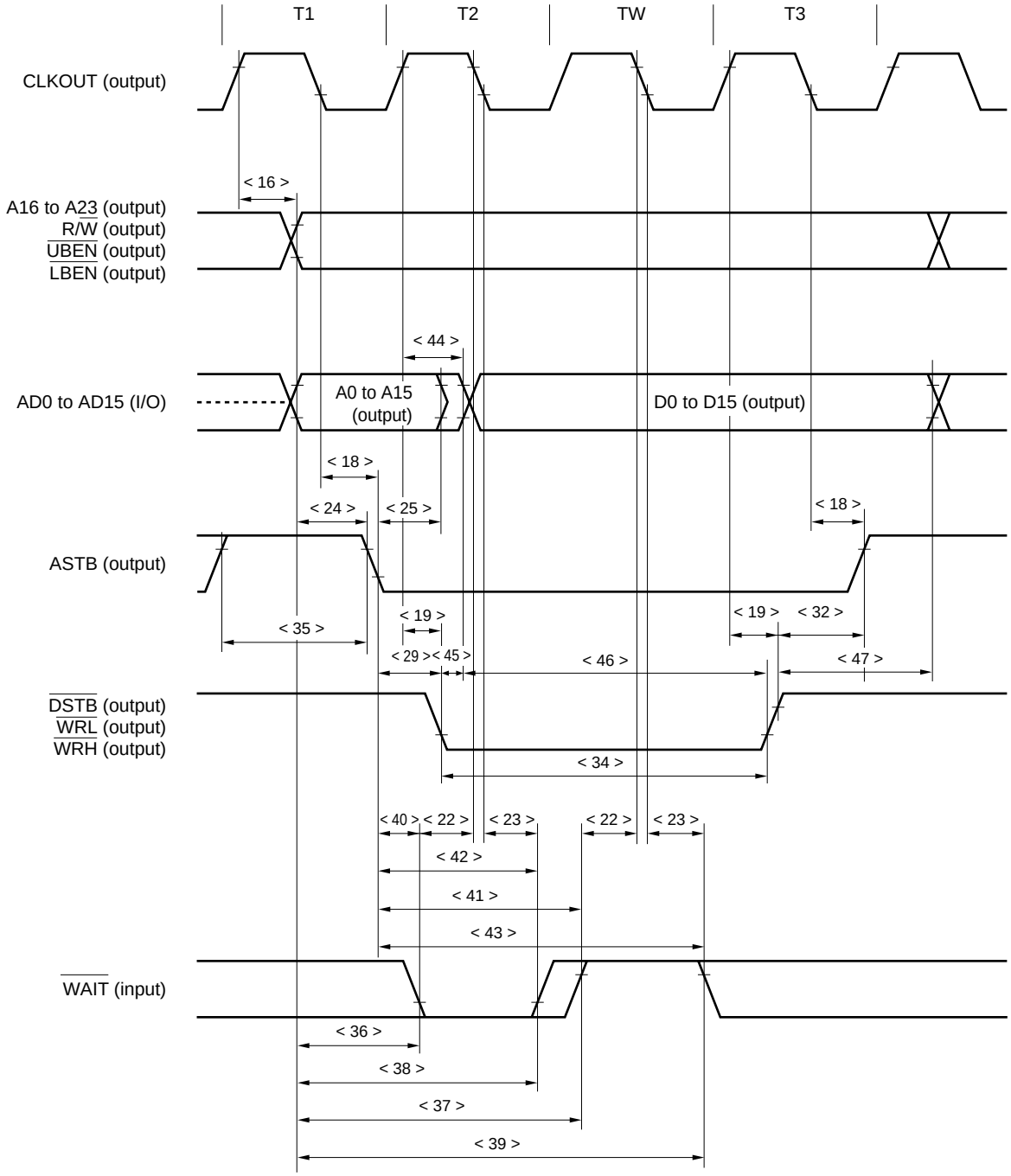
(5) Write timing (1/2)

Parameter	Symbol		Condition	MIN.	MAX.	Unit
CLKOUT ↑→ address delay time	<16>	t_{DKA}		3	14	ns
CLKOUT ↓→ ASTB delay time	<18>	t_{DKST}		3	14	ns
CLKOUT ↑→ $\overline{\text{DSTB}}$ delay time	<19>	t_{DKD}		3	14	ns
$\overline{\text{WAIT}}$ setup time (to CLKOUT ↓)	<22>	t_{SWTK}		5		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT ↓)	<23>	t_{HKWT}		5		ns
Address setup time (to ASTB ↓)	<24>	t_{SAST}		0.5T – 10		ns
Address hold time (from ASTB ↓)	<25>	t_{HSTA}		0.5T – 10		ns
ASTB ↓→ $\overline{\text{DSTB}}$ ↓ delay time	<29>	t_{DSTD}		0.5T – 10		ns
$\overline{\text{DSTB}}$ ↑→ ASTB ↑ delay time	<32>	t_{DDST1}		0.5T – 10		ns
$\overline{\text{DSTB}}$ low-level width	<34>	t_{WDL}		(1 + n)T – 10		ns
ASTB high-level width	<35>	t_{WSTH}		T – 10		ns
$\overline{\text{WAIT}}$ setup time (to address)	<36>	t_{SAWT1}			1.5T – 15	ns
	<37>	t_{SAWT2}	n ≥ 1		(1.5 + n)T – 15	ns
$\overline{\text{WAIT}}$ hold time (from address)	<38>	t_{HAWT1}		(0.5 + n)T		ns
	<39>	t_{HAWT2}	n ≥ 1	(1.5 + n)T		ns
$\overline{\text{WAIT}}$ setup time (to ASTB ↓)	<40>	t_{SSTWT1}			T – 15	ns
	<41>	t_{SSTWT2}	n ≥ 1		(1 + n)T – 15	ns
$\overline{\text{WAIT}}$ hold time (from ASTB ↓)	<42>	t_{HSTWT1}		nT		ns
	<43>	t_{HSTWT2}	n ≥ 1	(1 + n)T		ns
CLKOUT ↑ → data output delay time	<44>	t_{DKOD}			14	ns
$\overline{\text{DSTB}}$ ↓ → data output delay time	<45>	t_{DDOD}			5	ns
Data output setup time (to $\overline{\text{DSTB}}$ ↑)	<46>	t_{SODD}		(1 + n)T – 15		ns
Data output hold time (from $\overline{\text{DSTB}}$ ↑)	<47>	t_{HDOD}		T – 10		ns

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(5) Write timing (2/2): 1 wait



Remarks 1. RD: High-level output
2. The broken line indicates the high-impedance state.

(6) Bus hold timing (1/2)

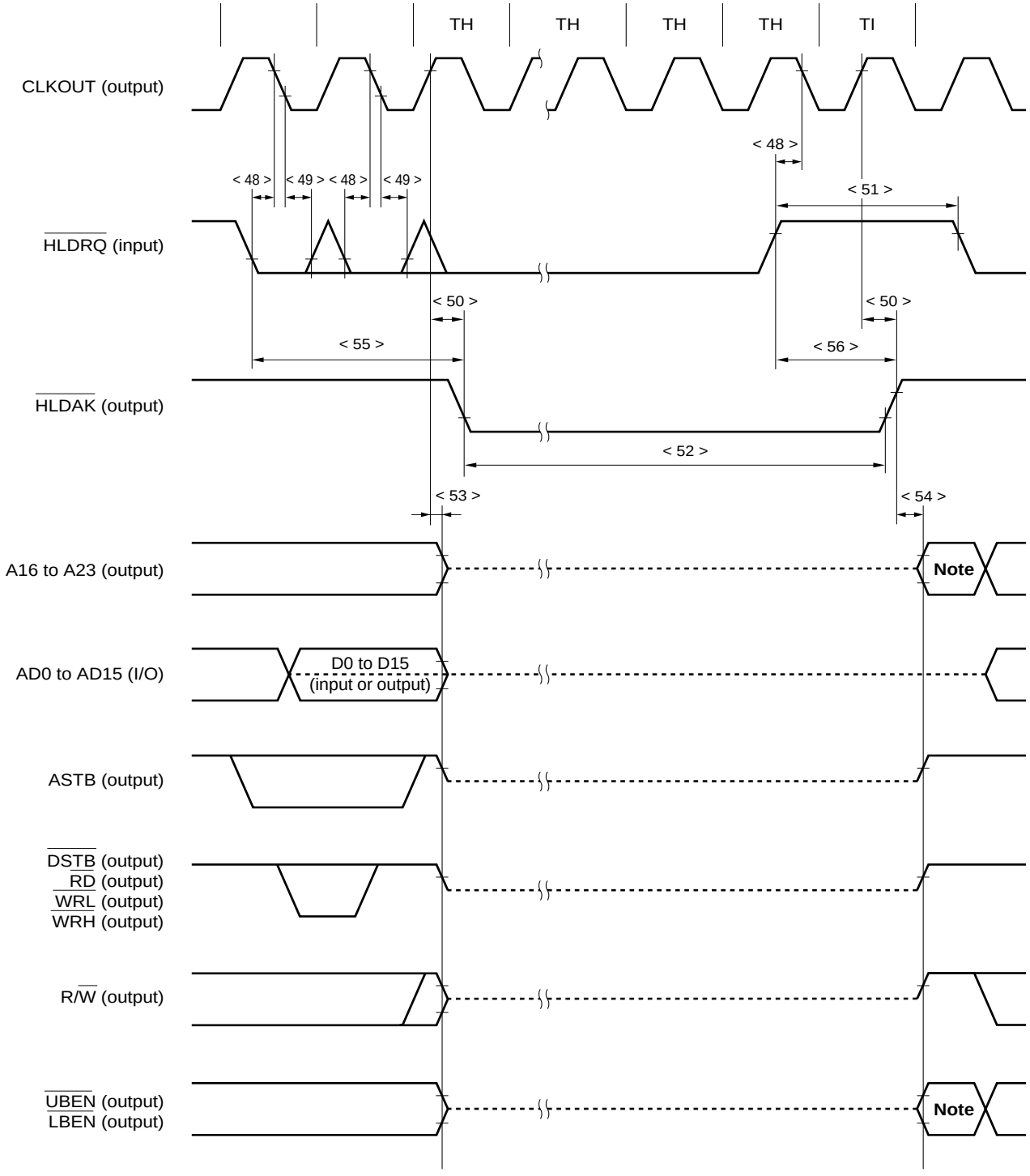
Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (to CLKOUT ↓)	<48>	t_{SHOK}		5		ns
$\overline{\text{HLDRQ}}$ hold time (from CLKOUT ↓)	<49>	t_{HKHQ}		5		ns
CLKOUT ↑→ $\overline{\text{HLDAK}}$ delay time	<50>	t_{DKHA}			14	ns
$\overline{\text{HLDRQ}}$ high-level width	<51>	t_{WHQH}		T + 10		ns
$\overline{\text{HLDAK}}$ low-level width	<52>	t_{WHAL}		T – 10		ns
CLKOUT↑ → bus float delay time	<53>	t_{DKF}			**Note**	ns
$\overline{\text{HLDAK}}$ ↑→ bus output delay time	<54>	t_{DHAC}		0		ns
$\overline{\text{HLDRQ}}$ ↓→ $\overline{\text{HLDAK}}$ ↓ delay time	<55>	t_{DHQHA1}		1.5T	(2 n + 7.5)T + 20	ns
$\overline{\text{HLDRQ}}$ ↑→ $\overline{\text{HLDAK}}$ ↑ delay time	<56>	t_{DHQHA2}		0.5T	1.5T + 20	ns

Note Under evaluation

Remarks 1. T = t_{CYK}

2. n indicates the number of wait clocks inserted in the bus cycle. The sampling timing differs when the programmable wait state is inserted.

(6) Bus hold timing (2/2)



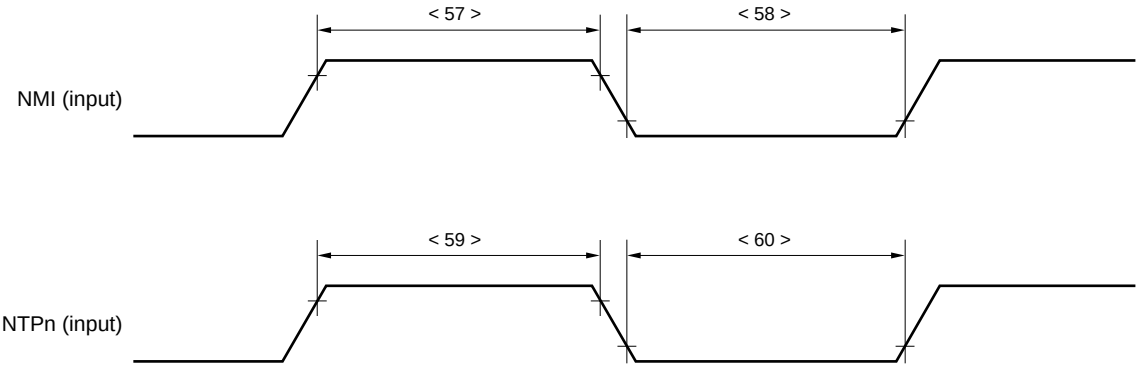
Note Under evaluation.

Remark The broken line indicates the high-impedance state.

(7) Interrupt timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
NMI high-level width	<57>	t_{WNIH}		500		ns
NMI low-level width	<58>	t_{WNIL}		500		ns
INTPn high-level width	<59>	t_{WITH}	n = 00 to 05, 10 to 14, 20 to 24, 30, 50 to 53	3T + 10		ns
INTPn low-level width	<60>	t_{WITL}	n = 00 to 05, 10 to 14, 20 to 24, 30, 50 to 53	3T + 10		ns

Remark T = t_{CYK}

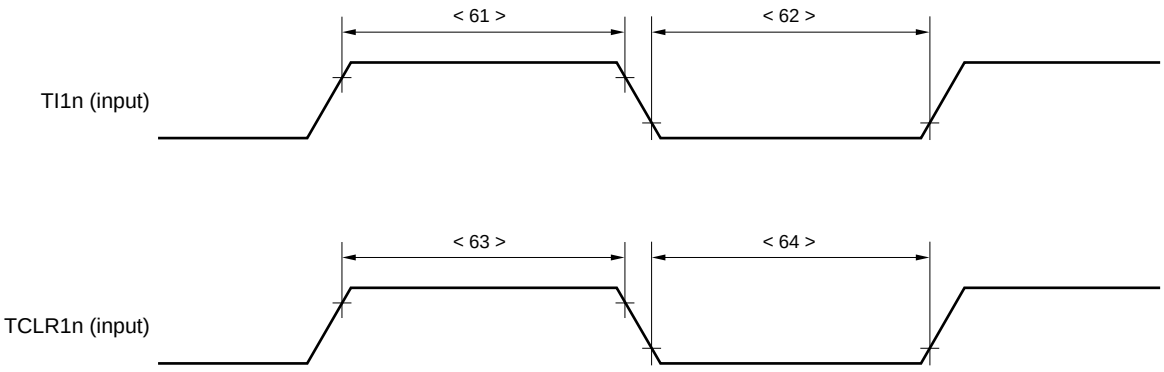


Remark n = 00 to 05, 10 to 14, 20 to 24, 30, 50 to 53

(8) RPU timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
TIn high-level width	<61>	t_{WTIH}	n = 0, 1, 20 to 24	3T + 10		ns
TIn low-level width	<62>	t_{WTIL}	n = 0, 1, 20 to 24	3T + 10		ns
TCLR0 high-level width	<63>	t_{WTCH}		3T + 10		ns
TCLR0 low-level width	<34>	t_{WTCL}		3T + 10		ns

Remark T = t_{CYK}



Remark n = 0, 1, 20 to 24

(9) CSI timing (1/2)

(a) Master mode

(i) CSI0, CSI2, CSI3 timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<65>	t_{CYSK}	Output	160		ns
$\overline{SCKn}$ high-level width	<66>	t_{WSKH}	Output	$0.5t_{CYSK}$ – 20		ns
$\overline{SCKn}$ low-level width	<67>	t_{WSKL}	Output	$0.5t_{CYSK}$ – 20		ns
SIn setup time (to $\overline{SCKn}$ ↑)	<68>	t_{SSISK}		30		ns
SIn hold time (from $\overline{SCKn}$ ↑)	<69>	t_{HSKSI}		0		ns
SOn output delay time (from $\overline{SCKn}$ ↓)	<70>	t_{DSKSO}			18	ns
SOn output hold time (from $\overline{SCKn}$ ↑)	<71>	t_{HSKSO}		$0.5t_{CYSK}$ – 5		ns

Remark n = 0, 2, 3

(ii) CSI1 timing

Parameter	Symbol		Condition		MIN.	MAX.	Unit
$\overline{SCK1}$ cycle	<65>	t_{CYSK}	Output	R_L = 1 kΩ	500		ns
$\overline{SCK1}$ high-level width	<66>	t_{WSKH}	Output	C_L = 50 pF	$0.5t_{CYSK}$ – 70		ns
$\overline{SCK1}$ low-level width	<67>	t_{WSKL}	Output		$0.5t_{CYSK}$ – 70		ns
SI1 setup time (to $\overline{SCK1}$ ↑)	<68>	t_{SSISK}			100		ns
SI1 hold time (from $\overline{SCK1}$ ↑)	<69>	t_{HSKSI}			50		ns
SO1 output delay time (from $\overline{SCK1}$ ↓)	<70>	t_{DSKSO}	R_L = 1 KΩ, C_L = 50 pF			150	ns
SO1 output hold time (from $\overline{SCK1}$ ↑)	<71>	t_{HSKSO}			$0.5t_{CYSK}$ – 5		ns

Remark R_L and C_L are the load resistance and load capacitance respectively of the $\overline{SCK1}$ and SO1 output lines.

(b) Slave mode

(i) CSI0, CSI2, CSI3 timing

Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<65>	t_{CYSK}	Input	160		ns
$\overline{SCKn}$ high-level width	<66>	t_{WSKH}	Input	50		ns
$\overline{SCKn}$ low-level width	<67>	t_{WSKL}	Input	50		ns
SIn setup time (to $\overline{SCKn}$ ↑)	<68>	t_{SSISK}		10		ns
SIn hold time (from $\overline{SCKn}$ ↑)	<69>	t_{HSKSI}		10		ns
SOn output delay time (from $\overline{SCKn}$ ↓)	<70>	t_{DSKSO}			30	ns
SOn output hold time (from $\overline{SCKn}$ ↑)	<71>	t_{HSKSO}		t_{WSKH}		ns

Remark n = 0, 2, 3

(9) CSI timing (2/2)

(ii) CSI1 timing

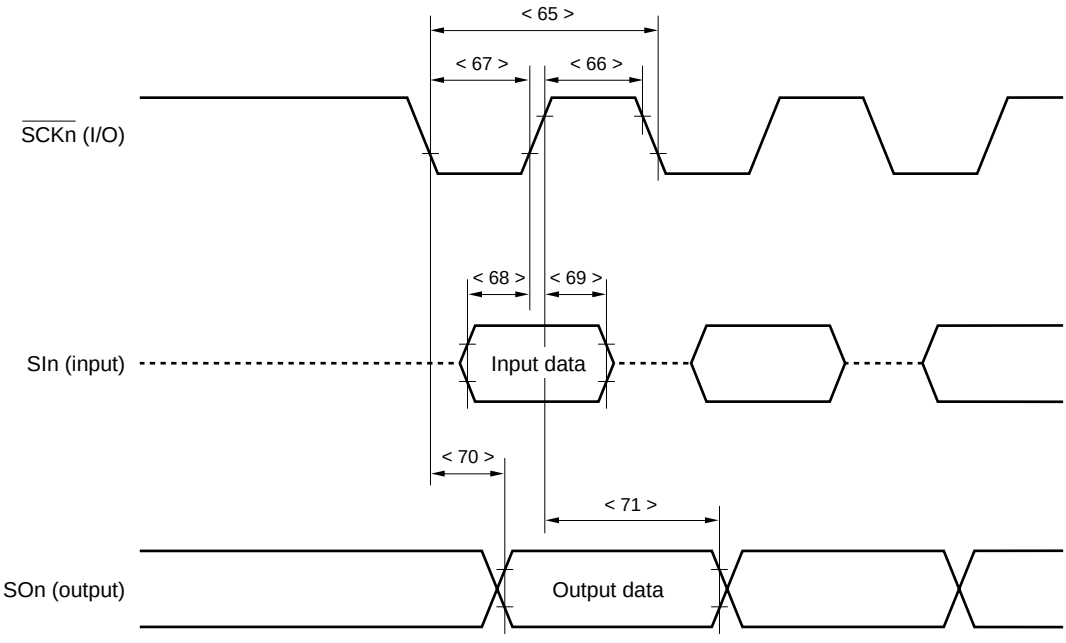
Parameter	Symbol		Condition	MIN.	MAX.	Unit
$\overline{SCK1}$ cycle	<65>	t_{CYSK}	Input	500		ns
$\overline{SCK1}$ high-level width	<66>	t_{WSKH}	Input	180		ns
$\overline{SCK1}$ low-level width	<67>	t_{WSKL}	Input	180		ns
SI1 setup time (to $\overline{SCK1}$ ↑)	<68>	t_{SSISK}		100		ns
SI1 hold time (from $\overline{SCK1}$ ↑)	<69>	t_{HSKSI}		50		ns
SO1 output delay time (from $\overline{SCK1}$ ↓)	<70>	t_{DSKSO}	R_L = 1 kΩ, C_L = 50 pF		150	ns
SO1 output hold time (from $\overline{SCK1}$ ↑)	<71>	t_{HSKSO}		t_{WSKH}		ns

Remark R_L and C_L are the load resistance and load capacitance respectively of the $\overline{SCK1}$ and SO1 output lines.

(c) SCKn cycle when V854 Series products are connected to each other

Parameter	Symbol		Condition (operating mode of master V854)	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<65>	t_{CYSK}	Transmission	160		ns
			Reception	160		ns
			Transmission/reception	160		ns

Remark n = 0 to 3



Remarks 1. The broken line indicates the high-impedance state.
2. n = 0 to 3

A/D Converter Characteristics

(T_A = –40 to +85°C, V_{DD} = AV_{DD} = BV_{DD} = CV_{DD} = 2.7 to 3.6V, V_{SS} = AV_{SS} = BV_{SS} = CV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX	Unit
Resolution	—		8			bit
Total error	—				**Note**	%
Quantization error	—				**Note**	LSB
Conversion time	t_{CONV}		2		**Note**	μs
Sampling time	t_{SAMP}		**Note**		**Note**	μs
Zero-scale error	—				±2	LSB
Full-scale error	—				±2	LSB
Linearity error	—				±2	LSB
Analog input voltage	V_{IAN}		–0.3		AV_{REF} + 0.3	V
Analog input resistance	R_{AN}			**Note**		MΩ
				Note		MΩ
AV_{REF} input voltage	AV_{REF}		**Note**		V_{DD}	V
AV_{REF} input current	AI_{REF}				**Note**	mA
					Note	μA
AV_{DD} current	AI_{DD}				**Note**	μA
ADTRG high-level width	T_{WADH}		3T + 10			ns
ADTRG low-level width	T_{WADL}		3T + 10			ns

Note Under evaluation

4.2 Flash Memory Programming Mode

Basic Characteristics (under evaluation)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Operating frequency	f_X				33	MHz
Supply voltage	V_{DD}		2.7		3.6	V
	V_{PPL}	V_{PP} low level detection	–0.3		$0.2V_{DD}$	V
	V_{PPM}	V_{DD} level of V_{PP} detection	$0.8V_{DD}$		$1.2V_{DD}$	V
	V_{PPH}	V_{PP} high voltage detection	7.2		7.8	V
V_{DD} supply current	I_{DO}				**Note**	mA
V_{PP} supply current	I_{PP}	V_{PP} = 7.5 V			**Note**	mA
Number of rewrite	C_{WRT}				100	times
Number of write	t_{WRT}			50		μs
Erasure time	t_{ERASE}				**Note**	s

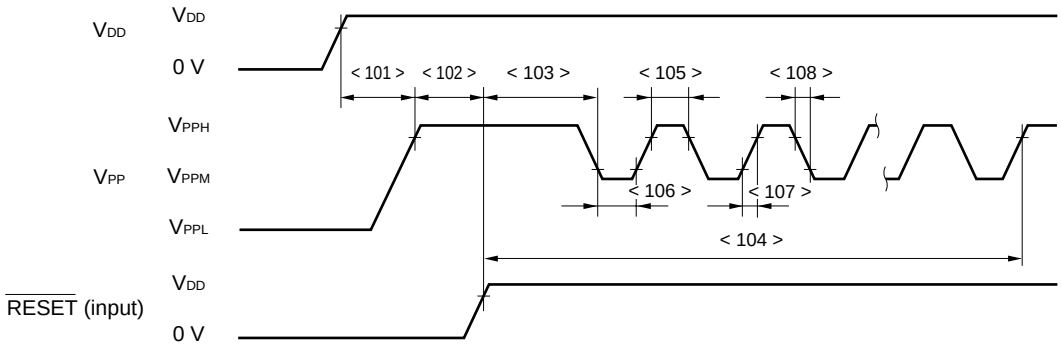
Note Under evaluation

Serial Write Operation Characteristics

Parameter	Symbol		Conditions	MIN.	TYP.	MAX.	Unit
V_{DD} ↑→ $\overline{RESET}$ ↑ setup time	<101>	t_{DRPSR}		**Note**			μs
V_{PP} ↑→ $\overline{RESET}$ ↑ setup time	<102>	t_{PSRRF}		**Note**			μs
$\overline{RESET}$ ↑→ V_{PP} count start time	<103>	t_{RFCF}		**Note**			μs
Count execution time	<104>	t_{COUNT}		**Note**		**Note**	ms
V_{PP} counter high-level width	<105>	t_{CH}		**Note**			μs
V_{PP} counter low-level width	<106>	t_{CL}		**Note**			μs
V_{PP} counter rise time	<107>	t_R				**Note**	μs
V_{PP} counter fall time	<108>	t_F				**Note**	μs

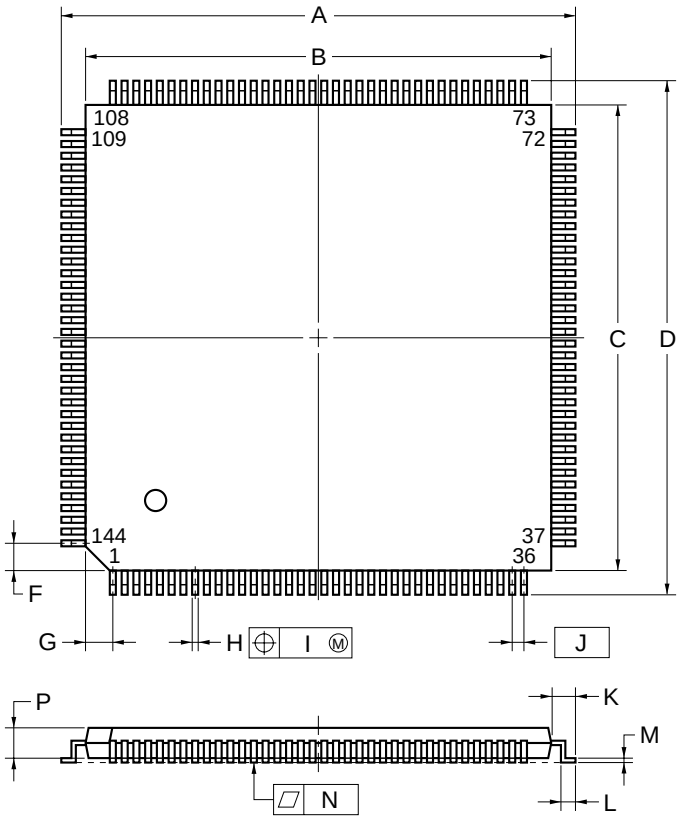
Note Under evaluation

Remark T = t_{CYK}

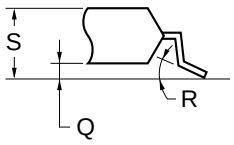


5. PACKAGE DRAWING

144 PIN PLASTIC LQFP (FINE PITCH) (20×20)



detail of lead end



NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	22.0±0.2	0.866±0.008
B	20.0±0.2	$0.787^{+0.009}_{-0.008}$
C	20.0±0.2	$0.787^{+0.009}_{-0.008}$
D	22.0±0.2	0.866±0.008
F	1.25	0.049
G	1.25	0.049
H	$0.22^{+0.05}_{-0.04}$	0.009±0.002
I	0.10	0.004
J	0.5 (T.P.)	0.020 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
L	0.5±0.2	$0.020^{+0.008}_{-0.009}$
M	$0.145^{+0.055}_{-0.045}$	0.006±0.002
N	0.10	0.004
P	1.4±0.1	0.055±0.004
Q	0.125±0.075	0.005±0.003
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.7 MAX.	0.067 MAX.

S144GJ-50-8EU-2

6. RECOMMENDED SOLDERING CONDITIONS

Undefined

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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Related document : μPD70F3008Y Data Sheet (U12755E)
V850 Family Instruction Application Table (U10229J) (Japanese version)

Reference document: Electrical Characteristics for Microcomputer (IEI-601) (Japanese version)

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