IXYS

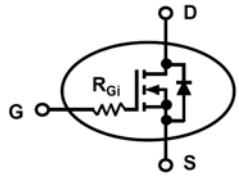
Preliminary Technical Information

High Voltage Power MOSFET

IXTL2N450

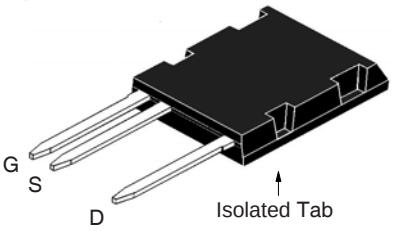
V_{DSS} = 4500V
I_{D25} = 2A
$R_{DS(on)}$ ≤ 23Ω

(Electrically Isolated Tab)



N-Channel Enhancement Mode

ISOPLUS i5-Pak™



G = Gate S = Source
D = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	4500	V
V_{DGR}	T_J = 25°C to 150°C, R_{GS} = 1MΩ	4500	V
V_{GSS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25°C	2	A
I_{DM}	T_C = 25°C, Pulse Width Limited by T_{JM}	8	A
P_D	T_C = 25°C	220	W
T_J		- 55 ... +150	°C
T_{JM}		150	°C
T_{stg}		- 55 ... +150	°C
T_L	Maximum Lead Temperature for Soldering	300	°C
T_{SOLD}	Plastic Body for 10s	260	°C
F_C	Mounting Force	20..120 / 4.5..27	N/lb.
V_{ISOL}	50/60Hz, 1 Minute	4000	V~
Weight		8	g

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250μA	3.5		5.5	V
I_{GSS}	V_{GS} = ±20V, V_{DS} = 0V			±200	nA
I_{DSS}	V_{DS} = 3.6kV, V_{GS} = 0V			25	μA
	V_{DS} = 4.5kV			50	μA
	V_{DS} = 3.6kV Note 2, T_J = 125°C		250		μA
$R_{DS(on)}$	V_{GS} = 10V, I_D = 0.5 • I_{D25}, Note 1			23	Ω

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ RMS Electrical Isolation
- Molding Epoxies meet UL 94 V-0 Flammability Classification

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- High Voltage Power Supplies
- Capacitor Discharge Applications
- Pulse Circuits
- Laser and X-Ray Generation Systems

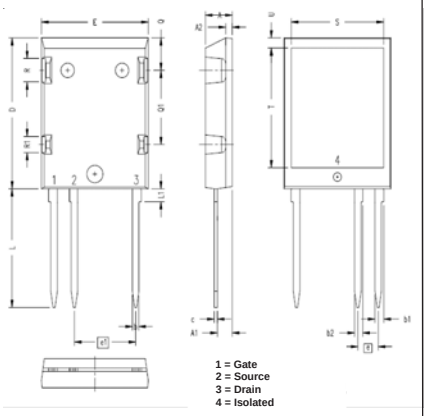
Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 60V, I_D = 0.5 • I_{D25}, Note 1	1.3	2.2		S
C_{iss}	V_{GS} = 0V, V_{DS} = 25V, f = 1MHz		6900		pF
C_{oss}			264		pF
C_{rss}			88		pF
R_{Gi}	Integrated Gate Input Resistance		3.0		Ω
$t_{d(on)}$	**Resistive Switching Times**		44		ns
t_r	V_{GS} = 10V, V_{DS} = 1kV, I_D = 1A		38		ns
$t_{d(off)}$	R_G = 0Ω (External)		100		ns
t_f			205		ns
$Q_{g(on)}$	V_{GS} = 10V, V_{DS} = 1kV, I_D = 0.5 • I_{D25}		156		nC
Q_{gs}			38		nC
Q_{gd}			67		nC
R_{thJC}				0.56	°C/W
R_{thCS}			0.15		°C/W

Source-Drain Diode

Symbol	Test Conditions (T_J = 25°C, Unless Otherwise Specified)	Characteristic Values Min.	Typ.	Max.	
I_S	V_{GS} = 0V			2	A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			8	A
V_{SD}	I_F = I_S, V_{GS} = 0V, Note 1			3	V
t_{rr}	I_F = 2A, -di/dt = 100A/μs, V_R = 100V		1.75		μs

Notes: 1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Part must be heatsunk for high-temp Idss measurement.

ISOPLUS i5-Pak™ (IXTL) Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETER MIN	MILLIMETER MAX
A	0.190	0.205	4.83	5.21
A1	0.102	0.118	2.59	3.00
A2	0.046	0.055	1.17	1.40
b	0.045	0.055	1.14	1.40
b1	0.063	0.072	1.60	1.83
b2	0.058	0.068	1.47	1.73
c	0.020	0.029	0.51	0.74
D	1.020	1.040	25.91	26.42
E	0.770	0.799	19.56	20.29
e	0.150 BSC		3.81 BSC	
e1	0.450 BSC		11.43 BSC	
L	0.780	0.820	19.81	20.83
L1	0.080	0.102	2.03	2.59
Q	0.210	0.235	5.33	5.97
Q1	0.490	0.513	12.45	13.03
R	0.150	0.180	3.81	4.57
R1	0.100	0.130	2.54	3.30
S	0.668	0.690	16.97	17.53
T	0.801	0.821	20.34	20.85
U	0.065	0.080	1.65	2.03

PRELIMANARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

Fig. 1. Output Characteristics @ T_J = 25ºC

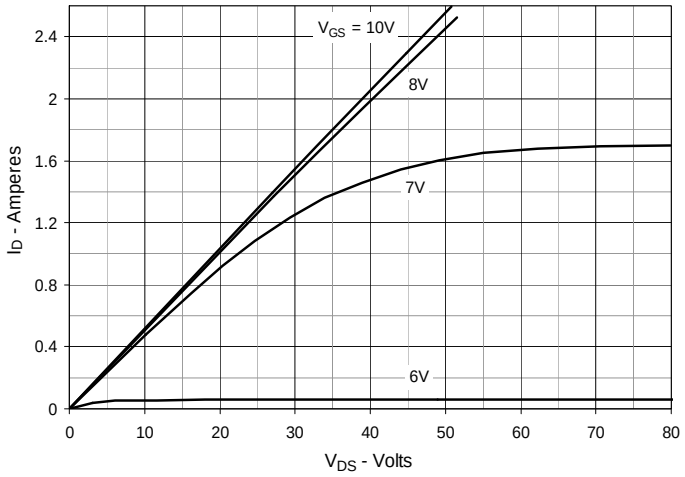


Fig. 3. Output Characteristics @ T_J = 125ºC

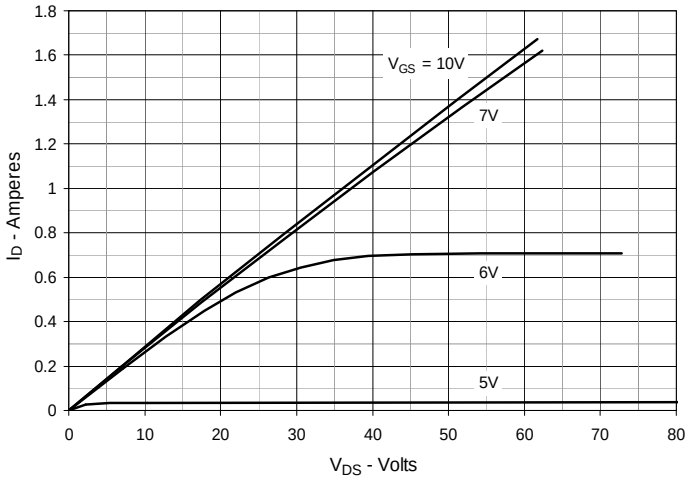


Fig. 3. $R_{DS(on)}$ Normalized to I_D = 1A Value vs. Junction Temperature

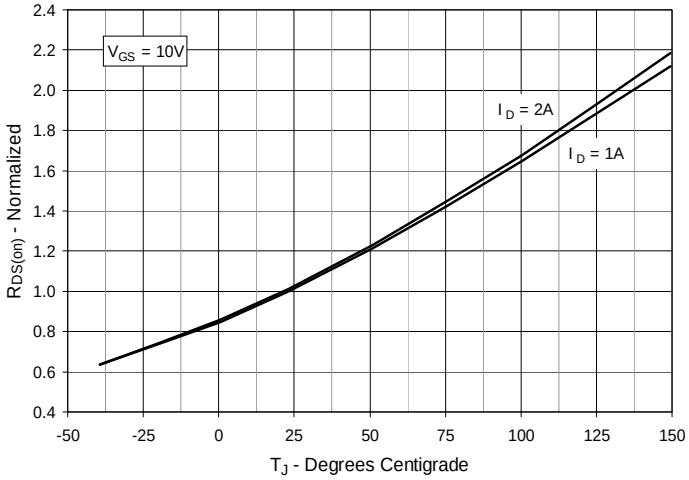


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 1A Value vs. Drain Current

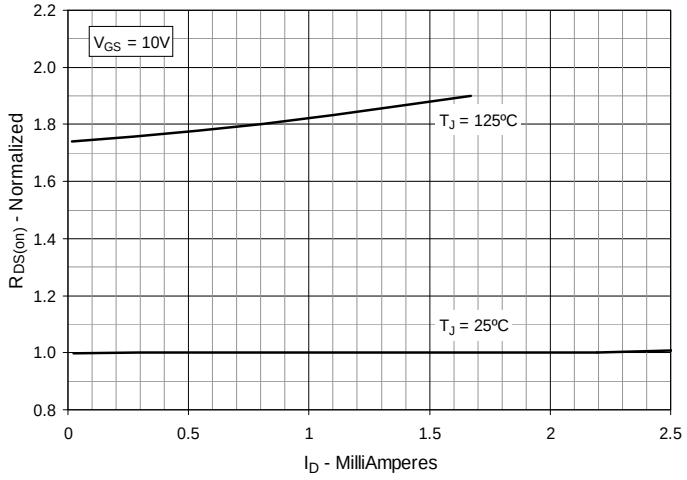


Fig. 5. Maximum Drain Current vs. Case Temperature

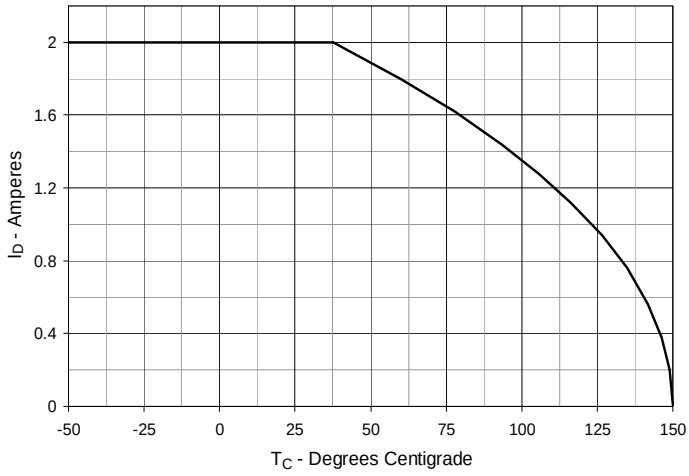


Fig. 6. Input Admittance

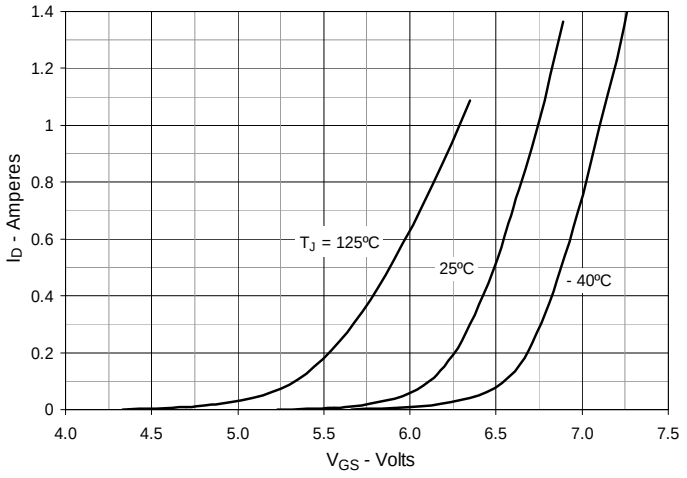


Fig. 7. Transconductance

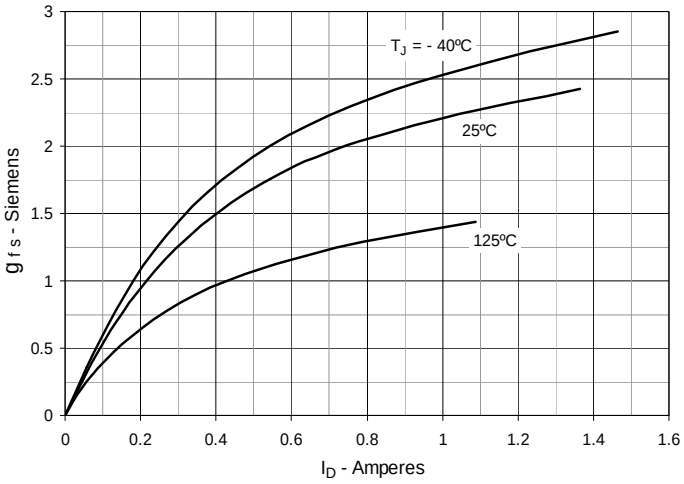


Fig. 8. Forward Voltage Drop of Intrintsic Diode

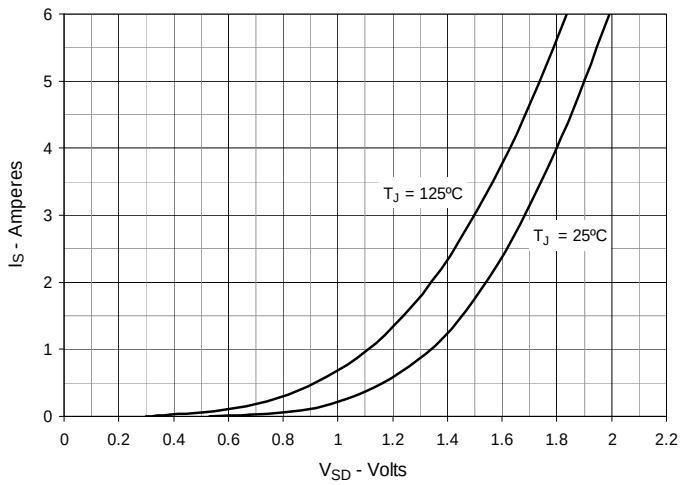


Fig. 9. Gate Charge

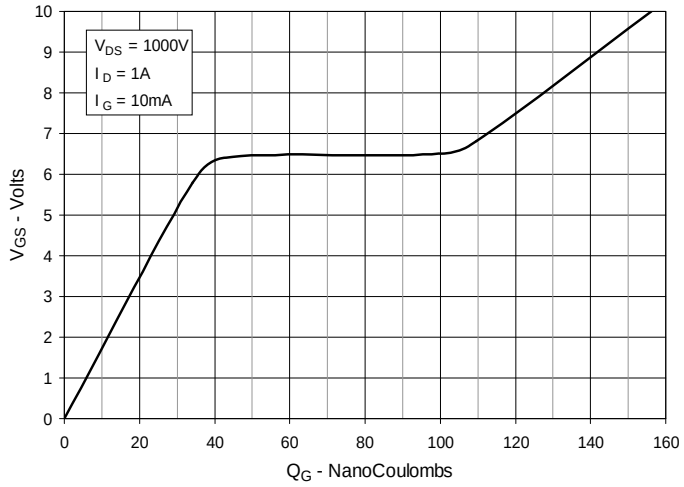


Fig. 10. Capacitance

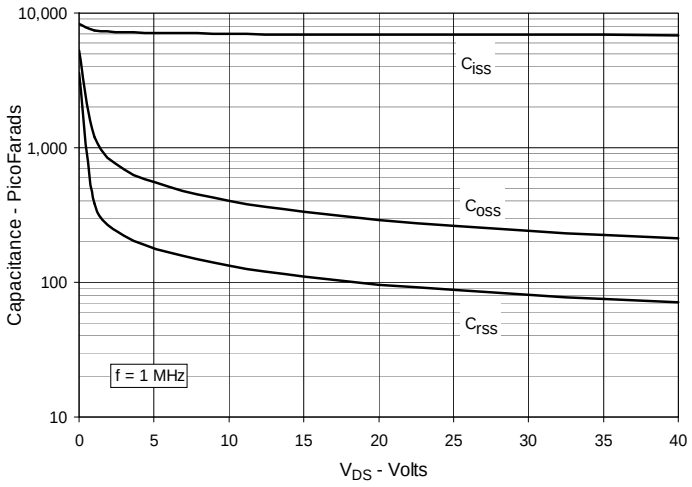


Fig. 11. Resistive Switching Times vs. External Gate Resistance

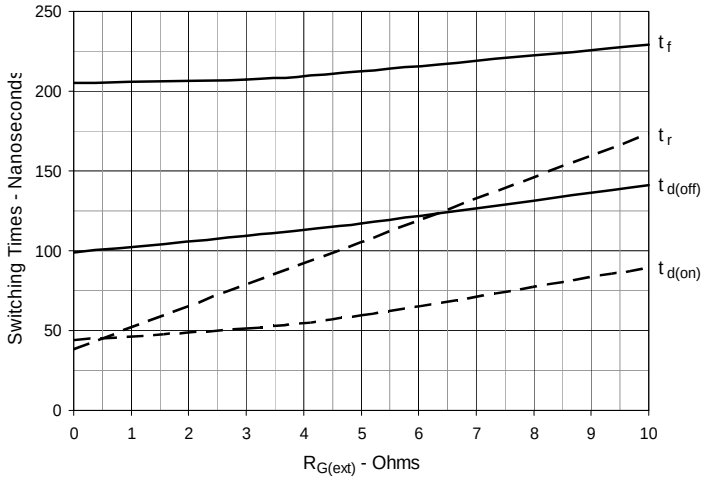


Fig. 12. Forward-Bias Safe Operating Area

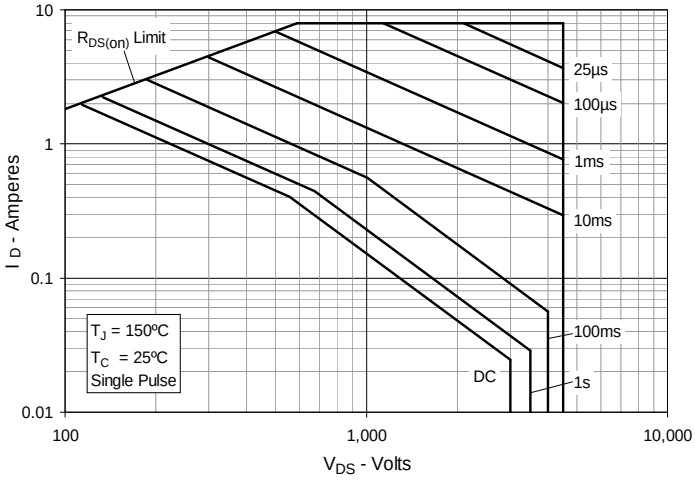


Fig. 13. Maximum Transient Thermal Impedance