H3208
1024 x 8
CMOS EEPROM

HUGHES AIRCRAFT COMPANY

MICROELECTRONICS CENTER

DESCRIPTION

Hughes H3208 is a CMOS Electrically Erasable and Programmable ROM (EEPROM) organized as 1024 x 8 bits. Read, write and erase operations are performed with a single 5V power supply using TTL level control signals.

All data modification is accomplished with $\overline{WE}$ at a logic low level. Erasing or writing is controlled by appropriate control signals on $\overline{CE}$ and $\overline{OE}$ and by information presented on the address lines.

Chip or row erase operations may be performed when both $\overline{OE}$ and $\overline{WE}$ are at logic low. With logic lows on A0-A2, a chip enable ($\overline{CE}$) low pulse will initiate a chip erase operation. With a valid address presented on pins A0-A9, a chip enable pulse will execute a row erase for the row that holds the particular address.

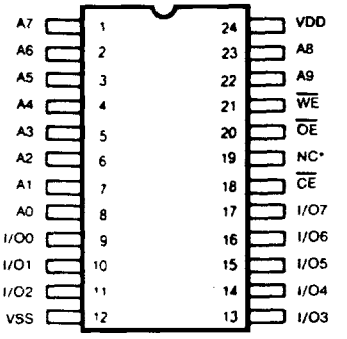
A byte write operation is accomplished with $\overline{OE}$ high and $\overline{WE}$ low. Data will be latched on the falling edge of the $\overline{CE}$ and written to the address presented on address lines A0-A9.

The 3208 is available in a variety of plastic and ceramic dual-in-line packages. Commercial (HC3208), Industrial (HI3208) and Military (HB3208) versions are available.

FEATURES

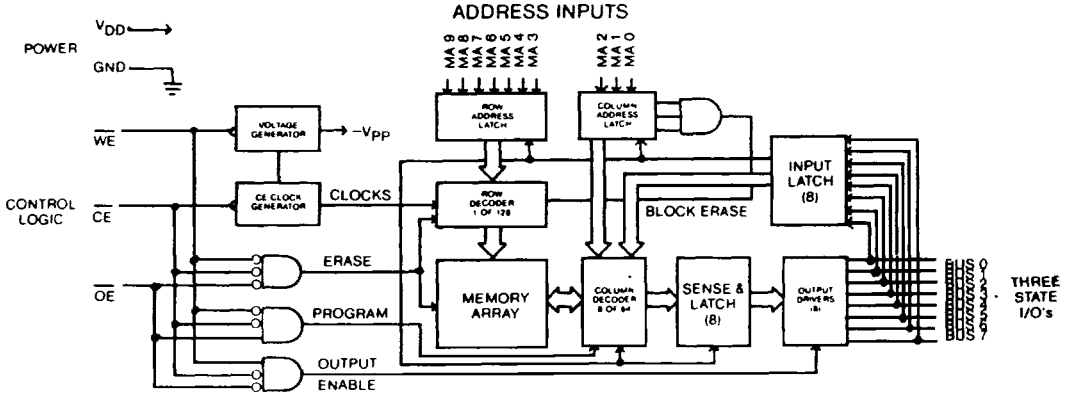
- Byte wide organization – 1024 x 8 bit
- Single 5V power supply– read, write and erase
- Very low power dissipation – CMOS
- Chip and row erasable
- On chip address and data latches
- Simple and efficient 3-line control (CE, OE, WE)
- 10-year data retention
- 10,000 byte erase/write cycles

PIN CONFIGURATION



*No connection to this pin allowed (Internal pull-up to V_{DD}).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

DC Supply Voltage Range ..... −0.3 to +7 Volts
(All voltages referenced to GND terminal)
Input Voltage Range ..... −0.3 to V_{DD} + 0.3V
Storage Temperature Range ... −65°C to +150°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Erase/Write functions above V_{DD} = 5.5V will adversely affect endurance[1].

RECOMMENDED OPERATING CONDITIONS

		All Modes
Supply Voltage		5v ± 5%
Temperature Range	Plastic Package	−40°C to +85°C
	Ceramic Package	−55°C to +125°C

DC OPERATING CHARACTERISTICS

V_{DD} = 5.5V Unless Otherwise Specified

Symbol	Parameter	+25°C			−40°C to +85°C		−55°C to +125°C		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
I_{DDS}	V_{DD} Standby Current	–	2	100	–	100	–	100	µA	CE = OE = WE= 5.5V
I_{DDA}	V_{DD} Active Current	–	750	1000	–	1000	–	1000	µA	CE =OE = 0 WE = 5.5V
I_{DPP}	V_{DD} Program Current	–	1	2	–	2	–	2	mA	WE = 0V
V_{OL}	Output Low Voltage	–	0.25	0.45	–	0.45	–	0.45	V	V_{DD} = 5V I_O = 2.1mA
V_{OH}	Output High Voltage	3.0	4.5	–	3.0	–	3.0	–	V	V_{DD} = 5V I_O = −400µA
V_{IL}	Input Low Voltage	–	–	0.8	–	0.8	–	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	3.0	–	–	3.0	–	3.0	–	V	V_{DD} = 5V
I_{LI}	Input Leakage Current	–	–	±10	–	±10	–	±10	µA	V_{IN} = 0 or V_{DD}
I_{LO}	Output Leakage Current	–	–	±10	–	±10	–	±10	µA	V_O = 0 or V_{DD}

Notes:
1. Endurance is the maximum number of erase/write cycles per byte.
2. Retention is the amount of time the data is retained in memory without power being supplied.

AC OPERATING CHARACTERISTICS

Read: V_{DD} = 5V ±5% Unless Otherwise Specified

Symbol	Parameter	+25°C			−40°C to +85°C		−55°C to +125°C		Units	Test Conditions
		Min.	Typ.1	Max.	Min.	Max.	Min.	Max.		
t_{AS}	Address Set-Up Time	400	–	–	475	–	350	–	ns	$\overline{WE} = V_L$
t_{AH}	Address Hold Time	100	50	–	125	–	150	–	ns	$\overline{WE} = V_L$
t_{ACE}	Access Time from $\overline{CE}$	–	500	700	–	825	–	925	ns	$\overline{WE} = V_L$, $\overline{OE} = V_L$
t_{OE}	Output Enable Time	–	250	400	–	450	–	500	ns	$\overline{WE} = V_L$, $\overline{OE} = V_L$
t_{DCE}	$\overline{CE}$ to High Impedance	0	–	–	0	–	0	–	ns	–
t_{DOE}	$\overline{OE}$ to High Impedance	0	–	–	0	–	0	–	ns	$\overline{CE} = V_L$, $\overline{WE} = V_L$
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$, or $\overline{WE}$ which ever occurs first	0	–	–	0	–	0	–	ns	–
t_{CEH}	$\overline{CE}$ High Time	1.1	0.5	–	1.4	–	1.4	–	µs	–
I_{DYN}	V_{DD} Dynamic Current	–	0.5	1.0	–	1.2	–	1.2	mA	f = 100 KHz

Read Test Conditions

Output Load: C_L = 50 pF

Input Levels: V_H = 3.2 Volts, V_L = 0.45 Volts

Timing Measurement Reference Levels: Input = Output = 50%

Erase and Write, V_{DD} = 5V Unless Otherwise Specified

Symbol	Parameter	+25°C			−40°C to +85°C		−55°C to +125°C		Units	Test Conditions
		Min.	Typ.	Max.	Min.	Max.	Min.	Max.		
t_{AS}	Row Erase Address Set-Up Time	400	–	–	475	–	550	–	µs	–
t_{AH}	Row Erase Address Hold Time	100	–	–	125	–	150	–	ms	$\overline{WE} = V_L$
t_{WRITE}	Byte Write Pulse Width	1	–	–	1	–	1	–	ms	$\overline{WE} = V_L$
t_{AS}	Byte Write Address Set-Up Time	400	–	–	475	–	550	–	ns	$\overline{WE} = V_L$
t_{AH}	Byte Write Address Hold Time	100	–	–	125	–	150	–	ns	$\overline{WE} = V_L$
t_{DS}	Byte Write Data Set-Up Time	100	–	–	125	–	150	–	ns	$\overline{WE} = V_L$
t_{DH}	Byte Write Data Hold Time	100	–	–	125	–	150	–	ns	$\overline{WE} = V_L$

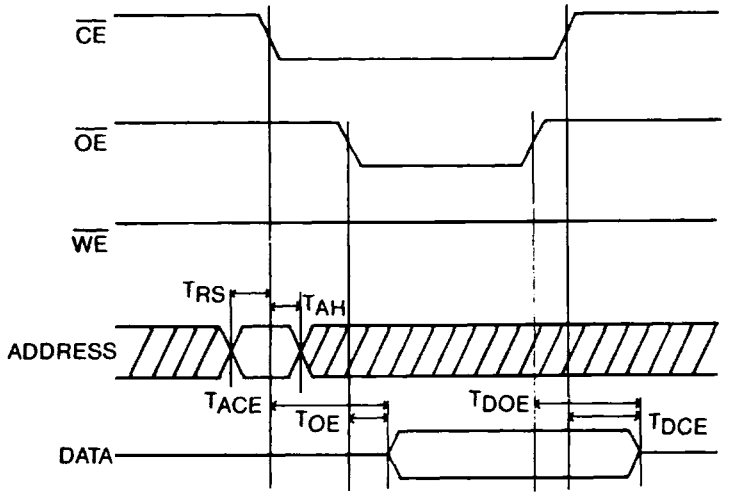
Programming Test Conditions

Input Levels: V_H = 3.2 Volts, V_L = 0.45 Volts

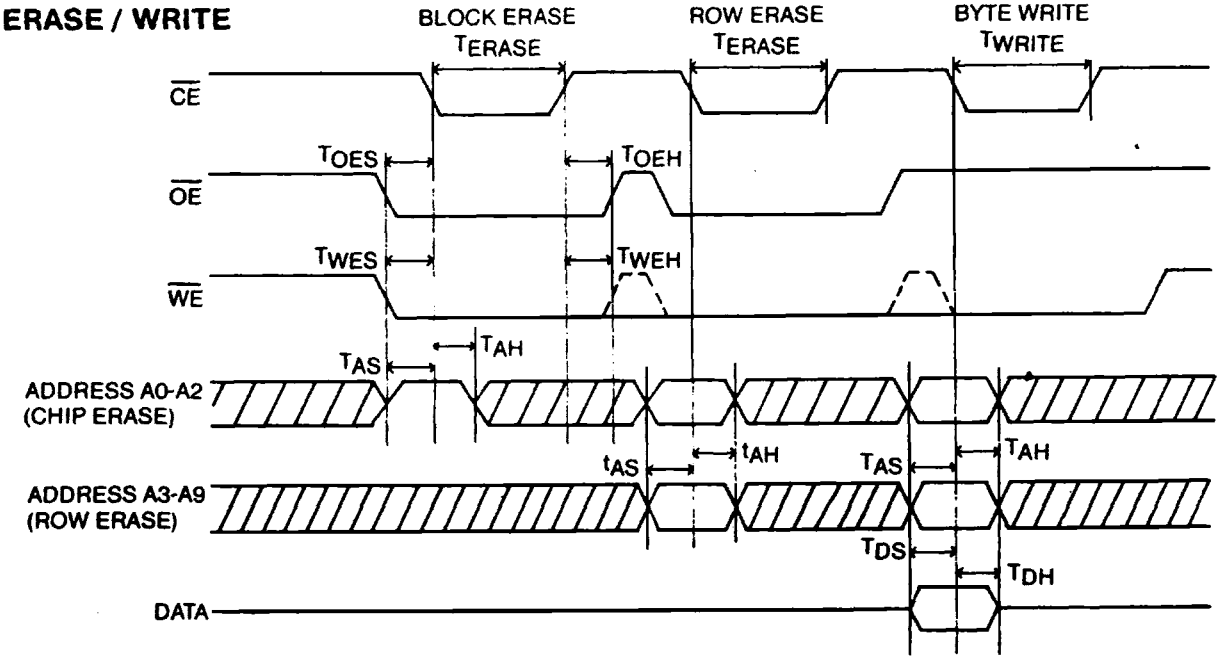
Timing Measurement Reference Levels: Input = Output = 50%

TIMING DIAGRAM

READ CYCLE



ERASE / WRITE



OPERATING MODES

The H3208 has four modes of operation: Read, Chip Erase, Row Erase, and Byte Write, all enabled when the chip is enabled ($\overline{CE}$ = low). In the Read Mode the H3208 functions as a normal CMOS ROM. When the Write Enable input ($\overline{WE}$) is lowered to V_{IL}, the Erase or Write Mode is enabled. In the Block Erase Mode, all bytes are reset to a logic low (GND), while in the Row Erase Mode, all bits in the Page are set to a logic low. In the Write Mode, bits of addressed byte may be programmed to a logic high. An Erase Operation is required before re-writing over previously Programmed data. Detailed procedures for each mode follow:

READ MODE: The circuit reads addresses on the falling edge of $\overline{CE}$ and latches the accessed data until $\overline{CE}$ goes high again. The latched data will appear at the outputs whenever $\overline{CE}$ is low, $\overline{WE}$ is high, and $\overline{OE}$ is low.

BLOCK ERASE MODE: A Block Erase (all 0's in memory) is accomplished by setting $\overline{WE}$ and $\overline{OE}$ low (with A 0 - A 2 High), and then pulsing $\overline{CE}$ low.

ROW ERASE MODE: A Row Erase is accomplished in the same manner as a Block Erase with any one of the three lowest address lines set to a logic low.

WRITE MODE: A Write consists of programming 1's into bits that contain a 0. A byte is written by setting $\overline{WE}$ and $\overline{OE}$ low, and pulsing $\overline{CE}$ low. The address and data lines must be valid when $\overline{CE}$ falls. Data and addresses are latched while $\overline{CE}$ is low.

SUMMARY OF OPERATING MODES

Logic 1 = High, Logic 0 = Low, X = Do not care

STATE	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O BUS	CONDITIONS
Standby (selected)	1	X	X	Floating	
Read	0	1	0	Data Output	
Erase (Block)	0	0	0	Floating	A 0 - A 2 = 1
Erase (Row)	0	0	0	Floating	A 3 - A 9 Valid
Write	0	0	1	Data Input	

PIN DESCRIPTIONS

A 0 - A 9: Address inputs which select one of 1024 bytes of memory for either Read, Row Erase, or Program. The addresses need to be valid during the falling edge of $\overline{CE}$.

I/O_0 - I/O_7: Bidirectional three-state data lines that are Data outputs during a Read operation and Data inputs during a Write operation.

GND: Negative supply terminal and V = 0 reference.

V_{DD}: Positive supply terminal.

$\overline{WE}$: Write Enable. A Logic Low enables all Data modifications. Erasing or Writing is controlled by appropriate control signals on $\overline{CE}$ and $\overline{OE}$.

$\overline{OE}$: Output Enable. A Logic High disables the Data Output Drivers in normal operation. During programming operations, a Logic Low selects the Erase Mode.

$\overline{CE}$: Chip Enable. A Logic Low at this input latches the input address during a Read operation and latches both addresses and data inputs during a Write operation. For the read operation, accessed data is latched and valid as long as $\overline{CE}$ is held at a Logic Low. A programming operation is initiated on the falling edge of $\overline{CE}$ and terminated on the rising edge of $\overline{CE}$.

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Printed in U.S.A.