

SRAM MODULE

16K x 32 SRAM

FEATURES

- High speed: 10*, 15, 20, 25 and 35ns
- High-performance, low-power, CMOS double-metal process
- Single +5V ±10% power supply
- Easy memory expansion with \overline{CE} and \overline{OE} functions
- Low profile
- All inputs and outputs are TTL-compatible
- Industry-standard pinout
- Upgradable with 64K x 32, 128K x 32 and 256K x 32 modules

OPTIONS

- Timing
 - 10ns access
 - 12ns access
 - 15ns access
 - 20ns access
 - 25ns access

MARKING

- 10*
- 12
- 15
- 20
- 25

Packages

- 64-pin SIMM
- 64-pin ZIP

M
Z

2V data retention

L

Part Number Example: MT8S1632M-10 L

*Consult factory

NOTE: Not all combinations of operating temperature, speed, data retention and low power are necessarily available. Please contact the factory for availability of specific part number combinations.

GENERAL DESCRIPTION

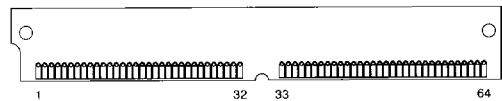
The MT8S1632 is a high-speed SRAM memory module containing 16,384 words organized in a x32-bit configuration. The module consists of eight 16K x 4 fast SRAMs mounted on a 64-pin, double-sided, FR4-printed circuit board.

Data is written into to the SRAM memory when write enable (\overline{WE}) and chip enable (\overline{CE}) inputs are both LOW. Reading is accomplished when \overline{WE} remains HIGH and \overline{CE} and output enable (\overline{OE}) are LOW. \overline{CE} can set the output in High-Z for additional flexibility in system design, and memory expansion is accomplished by use of the \overline{OE} and \overline{CE} functions.

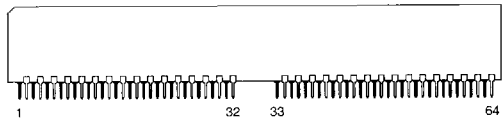
PD0 and PD1 identify the module's density, allowing interchangeable use of alternate density, industry-standard

PIN ASSIGNMENT (Top View)

64-Pin SIMM (SF-1)



64-Pin ZIP (SG-2)



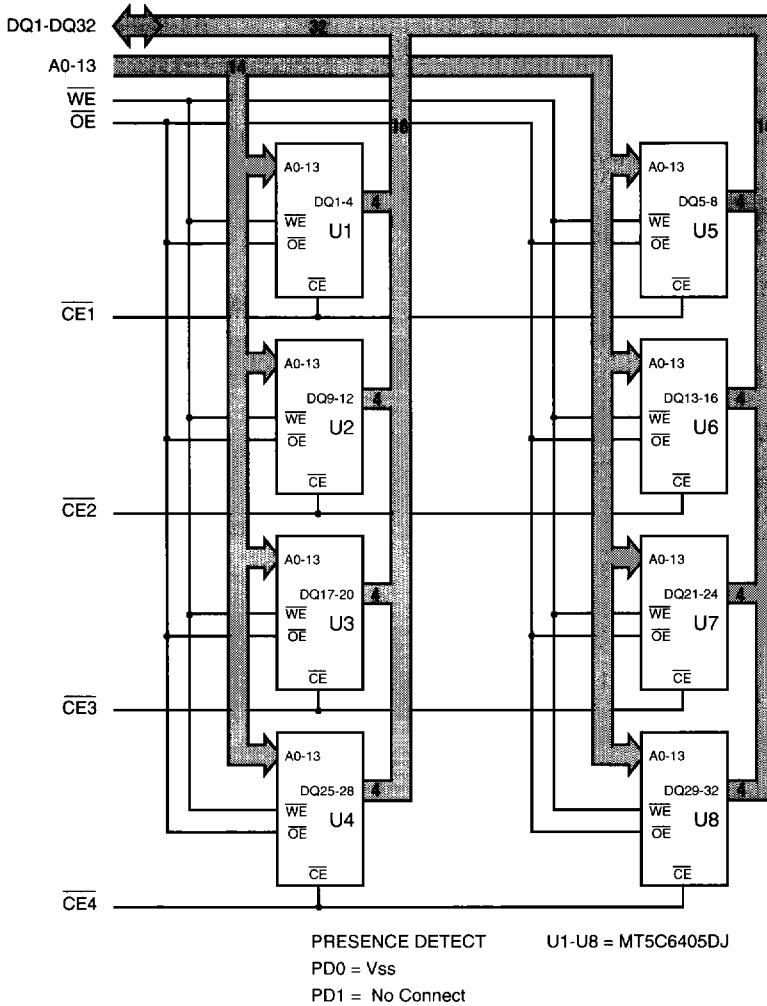
PIN #	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	Vss	17	A2	33	CE4	49	A4
2	PD0	18	A9	34	CE3	50	A11
3	PD1	19	DQ13	35	NC	51	A5
4	DQ1	20	DQ5	36	NC	52	A12
5	DQ9	21	DQ14	37	OE	53	Vcc
6	DQ2	22	DQ6	38	Vss	54	A13
7	DQ10	23	DQ15	39	DQ25	55	A6
8	DQ3	24	DQ7	40	DQ17	56	DQ21
9	DQ11	25	DQ16	41	DQ26	57	DQ29
10	DQ4	26	DQ8	42	DQ18	58	DQ22
11	DQ12	27	Vss	43	DQ27	59	DQ30
12	Vcc	28	WE	44	DQ19	60	DQ23
13	A0	29	NC	45	DQ28	61	DQ31
14	A7	30	NC	46	DQ20	62	DQ24
15	A1	31	CE2	47	A3	63	DQ32
16	A8	32	CE1	48	A10	64	Vss

modules. Four chip enable inputs, ($\overline{CE1}$, $\overline{CE2}$, $\overline{CE3}$ and $\overline{CE4}$), are used to enable the module's 4 bytes independently.

The Micron SRAM family uses a high-speed, low-power CMOS design in a four-transistor memory cell featuring double-layer metal, double-layer polysilicon technology. All module components may be powered from a single +5V supply and all inputs and outputs are fully TTL-compatible. The "L" option offers reduced-voltage operation for systems with low standby power requirements.

SRAM MODULE

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

MODE	\overline{OE}	\overline{CE}	WE	DQ	POWER
STANDBY	X	H	X	HIGH-Z	STANDBY
READ	L	L	H	Q	ACTIVE
NOT SELECTED	H	L	H	HIGH-Z	ACTIVE
WRITE	X	L	L	D	ACTIVE

SRAM MODULE

ABSOLUTE MAXIMUM RATINGS*

Voltage on Vcc Supply Relative to Vss	-1V to +7V
Storage Temperature	-55°C to +125°C
Power Dissipation	8W
Short Circuit Output Current	50mA
Voltage on Any Pin Relative to Vss	-1V to Vcc +1V

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{cc} = 5V ±10%)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V _{IH}	2.2	V _{cc} +1	V	1
Input Low (Logic 0) Voltage		V _{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V _{IN} ≤ V _{cc}	I _{LI}	-40	40	μA	
Output Leakage Current	Output(s) disabled 0V ≤ V _{OUT} ≤ V _{cc}	I _{LO}	-5	5	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.4	V	1
Supply Voltage		V _{cc}	4.5	5.5	V	1

SRAM MODULE

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX					UNITS	NOTES
				-10*	-12	-15	-20	-25		
Operating Current: TTL Input Levels	$\overline{CE} \leq V_{IL}; V_{cc} = \text{MAX}$ f = MAX = 1/4RC outputs open	I _{cc}	520	1,520	1,480	1,460	1,320	1,120	mA	3, 13
Standby Current: TTL Input Levels	$\overline{CE} \geq V_{IH}; V_{cc} = \text{MAX}$ f = MAX = 1/4RC outputs open	I _{sb1}	160	480	400	360	320	280	mA	13
Power Supply Current: Standby	$\overline{CE} \geq V_{cc} - 0.2V; V_{cc} = \text{MAX}$ V _{IN} ≤ V _{SS} +0.2V or V _{IN} ≥ V _{cc} -0.2V; f = 0	I _{sb2}	3.2	24	24	24	24	24	mA	13

*Consult factory

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: A0-A13, \overline{WE} , \overline{OE}	T _A = 25°C; f = 1 MHz V _{cc} = 5V	C _i	60	pF	4
Input Capacitance: $\overline{CE}1$ - $\overline{CE}4$		C ₁₂	15	pF	4
Input/Output Capacitance: DQ1-DQ32		C _{i/o}	10	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 (Note 5) ($0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$; $V_{CC} = 5V \pm 10\%$)

DESCRIPTION	SYM	-10*		-12		-15		-20		-25		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ Cycle													
READ cycle time	^t RC	10		12		15		20		25		ns	
Address access time	^t AA		10		12		15		20		25	ns	
Chip Enable access time	^t ACE		9		10		12		15		20	ns	
Output hold from address change	^t OH	3		3		3		3		3		ns	
Chip Enable to output in Low-Z	^t LZCE†	2		2		2		2		2		ns	7, 14
Chip Enable to output in High-Z	^t HZCE		5		6		7		8		8	ns	6, 7
Chip disable to power-up time	^t PU	0		0		0		0		0		ns	
Chip Enable to power-down time	^t PD		10		12		15		20		25	ns	
Output Enable access time	^t AOE		5		6		7		8		8	ns	
Output disable to output in Low-Z	^t LZOE	0		0		0		0		0		ns	
Output Enable to output in High-Z	^t HZOE		5		6		6		7		8	ns	6
WRITE Cycle													
WRITE cycle time	^t WC	10		12		15		20		25		ns	
Chip Enable to end of write	^t CW	8		10		12		15		20		ns	
Address valid to end of write	^t AW	8		10		12		15		20		ns	
Address setup time	^t AS	0		0		0		0		0		ns	
Address hold from end of write	^t AH	0		0		0		0		0		ns	
WRITE pulse width	^t WP1	7		8		10		12		15		ns	
WRITE pulse width	^t WP2	9		10		14		18		20		ns	
Data setup time	^t DS	6		7		8		9		10		ns	
Data hold time	^t DH	1		1		1		1		1		ns	
Write disable to output in Low-Z	^t LZWE	2		2		2		2		2		ns	7
Write Enable to output in High-Z	^t HZWE		5		5		6		8		8	ns	6, 7

*Consult factory

SRAM MODULE

AC TEST CONDITIONS

Input pulse levels	V _{ss} to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

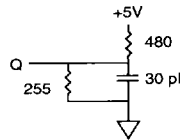


Fig. 1 OUTPUT LOAD EQUIVALENT

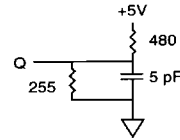


Fig. 2 OUTPUT LOAD EQUIVALENT

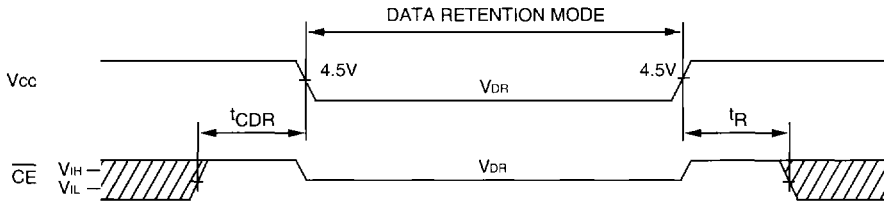
NOTES

- All voltages referenced to V_{ss} (GND).
- 3V for pulse width < t_{RC}/2.
- I_{cc} is dependent on output loading and cycle rates.
- This parameter is sampled.
- Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
- t_{HZCE}, t_{HZOE} and t_{HZWE} are specified with C_L = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, and t_{HZWE} is less than t_{LZWE}.
- \overline{WE} is HIGH for READ cycle.
- Device is continuously selected. All chip enables are held in their active state.
- Address valid prior to, or coincident with, latest occurring chip enable.
- t_{RC}=Read Cycle Time
- Chip enable and write enable can initiate and terminate a WRITE cycle.
- Typical values are measured at 5V, 25°C and 20ns cycle time.
- Typical currents are measured at 25°C.
- Output enable (\overline{OE}) is inactive (HIGH).
- Output enable (\overline{OE}) is active (LOW).

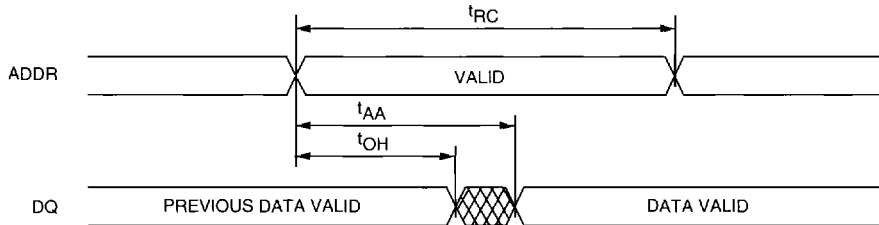
DATA RETENTION ELECTRICAL CHARACTERISTICS (L version only)

DESCRIPTION	CONDITIONS		SYMBOL	MIN	TYP	MAX	UNITS	NOTES
V _{cc} for Retention Data			V _{DR}	2			V	
Data Retention Current	$\overline{CE} \geq (V_{cc} - 0.2V)$ $V_{IN} \geq (V_{cc} - 0.2V)$ or $\leq 0.2V$	V _{cc} = 2V	I _{ccDR}		760	2,400	μA	14
		V _{cc} = 3V				1,000	4,400	μA
Chip Deselect to Data Retention Time			t _{CDR}	0			ns	4
Operation Recovery Time			t _R	t _{RC}			ns	4,11

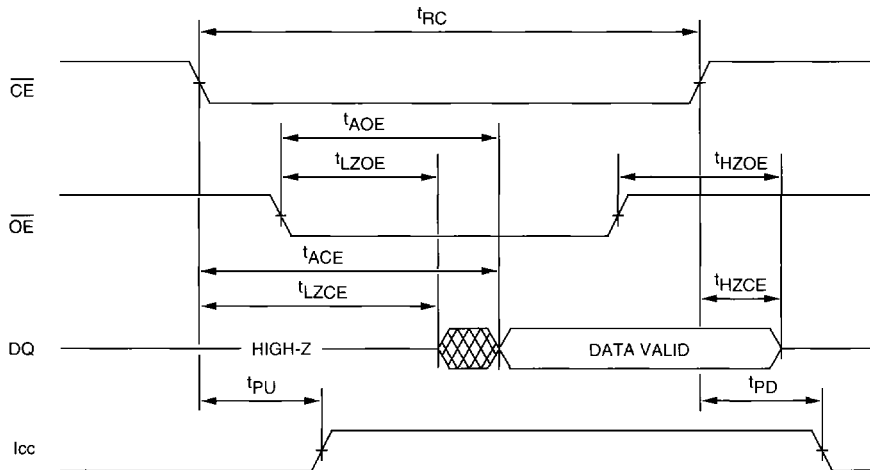
LOW V_{CC} DATA-RETENTION WAVEFORM





READ CYCLE NO. 1 8, 9



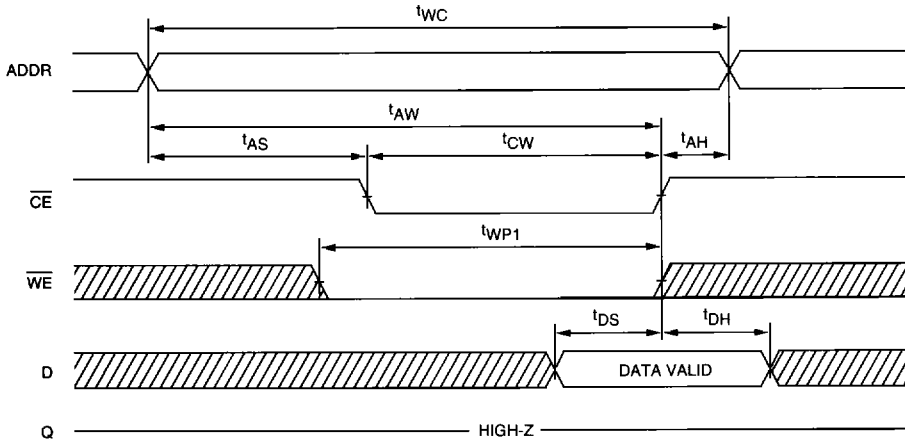
READ CYCLE NO. 2 7, 8, 10



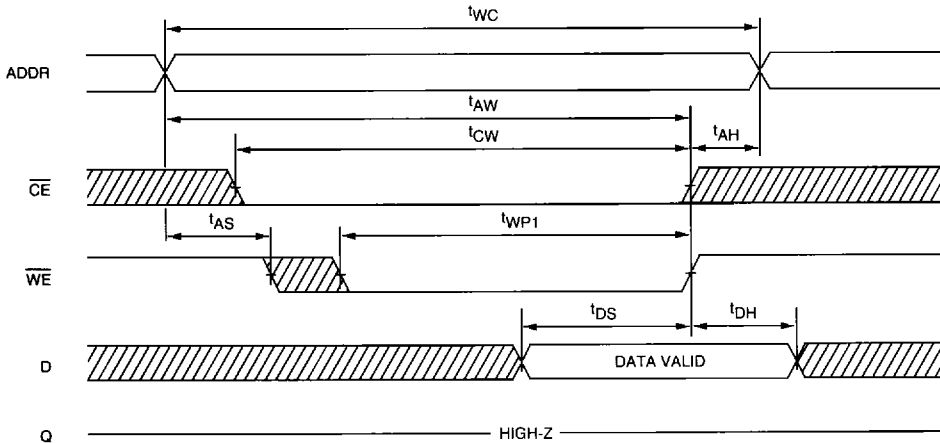
 DON'T CARE
 UNDEFINED



SRAM MODULE

WRITE CYCLE NO. 1¹²
(Chip Enable Controlled)

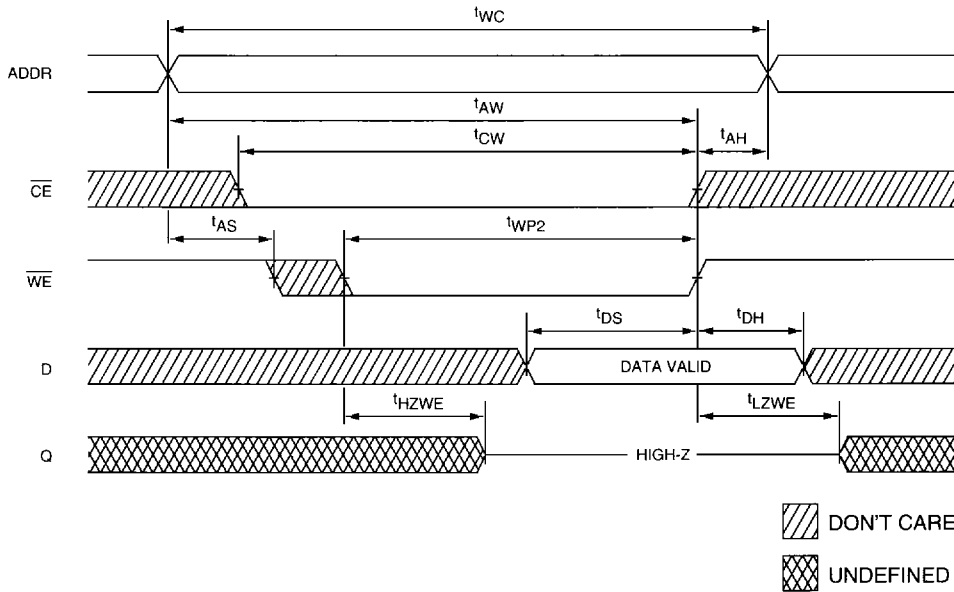


WRITE CYCLE NO. 2^{7, 12, 15}
(Write Enable Controlled)



 DON'T CARE
 UNDEFINED

WRITE CYCLE NO. 3 7, 12, 16
 (Write Enable Controlled)



SRAM MODULE