To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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M51995AP/AFP

Switching Regulator Control

REJ03D0835-0300
Rev.3.00
Jun 06, 2008

Description

M51995A is the primary switching regulator controller which is especially designed to get the regulated DC voltage from AC power supply.

This IC can directly drive the MOS-FET with fast rise and fast fall output pulse.

Type M51995A has the functions of not only high frequency OSC and fast output drive but also current limit with fast response and high sensibility so the true “fast switching regulator” can be realized.

It has another big feature of current protection to short and over current, owing to the integrated timer-type protection circuit, if few parts are added to the primary side.

The M51995A is equivalent to the M51977 with externally re-settable OVP (over voltage protection) circuit.

Features

- 500 kHz operation to MOS FET
  - Output current : ±2 A
  - Output rise time 60 ns, fall time 40 ns
  - Modified totempole output method with small through current
- Compact and light-weight power supply
  - Small start-up current : 90 μA typ.
  - Big difference between “start-up voltage” and “stop voltage” makes the smoothing capacitor of the power input section small.
    Start-up threshold 16 V, stop voltage 10 V
  - Packages with high power dissipation are used to with-stand the heat generated by the gate-drive current of MOS FET.
    16-pin DIP, 20-pin SOP 1.5 W (at 25°C)
- Simplified peripheral circuit with protection circuit and built-in large-capacity totempole output
  - High-speed current limiting circuit using pulse-by-pulse method (Two system of CLM+pin, CLM–pin)
  - Protection by intermittent operation of output over current : Timer protection circuit
  - Over-voltage protection circuit with an externally re-settable latch (OVP)
  - Protection circuit for output miss action at low supply voltage (UVLO)
- High-performance and highly functional power supply
  - Triangular wave oscillator for easy dead time setting

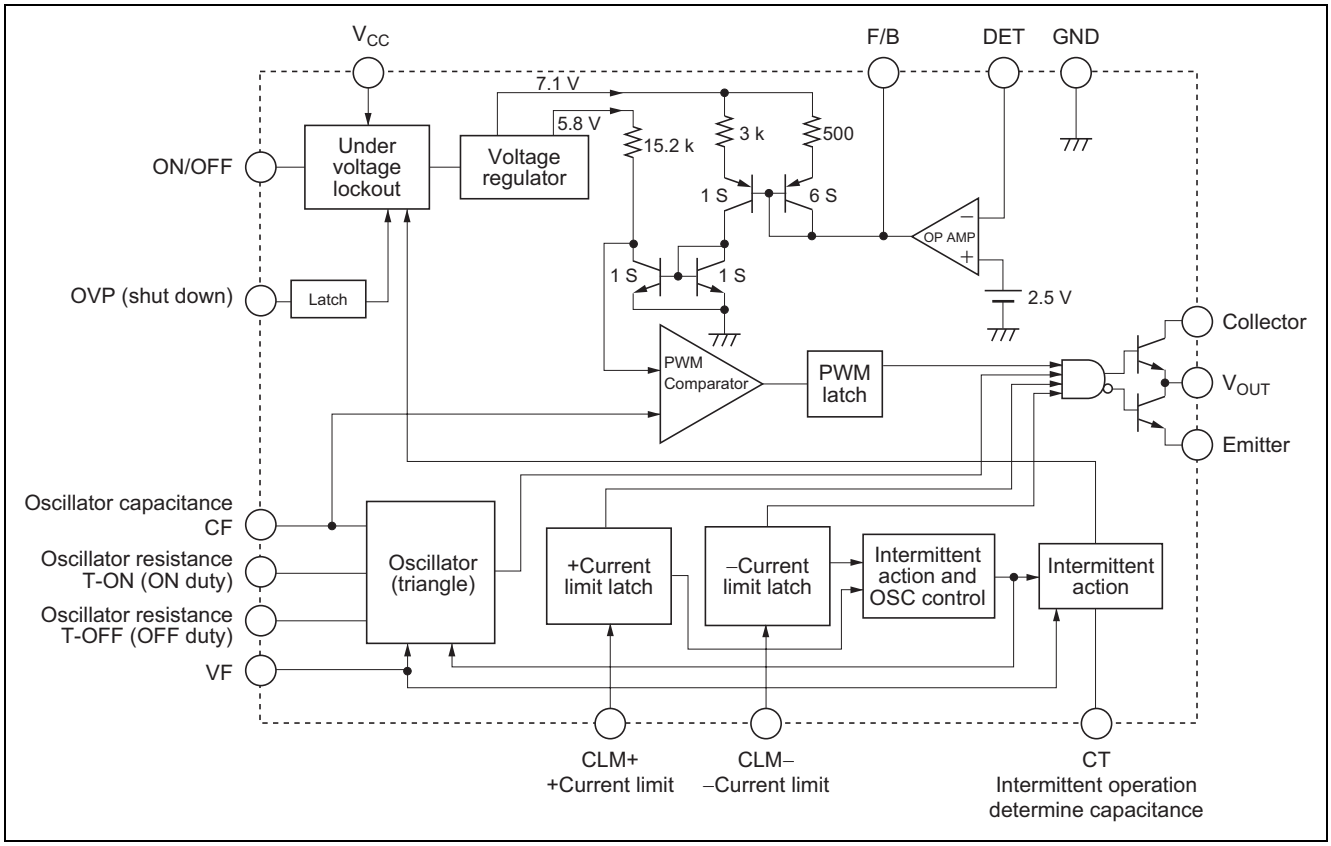
Application

Feed forward regulator, fly-back regulator

Recommended Operating Conditions

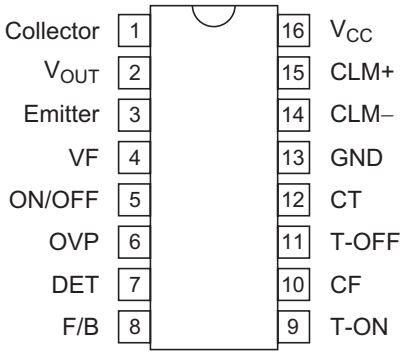
- Supply voltage range: 12 to 36 V
- Operating frequency: less than 500 kHz
- Oscillator frequency setting resistance
  - T-ON pin resistance R_{ON}: 10 k to 75 kΩ
  - T-OFF pin resistance R_{OFF}: 2 k to 30 kΩ

Block Diagram



Pin Arrangement

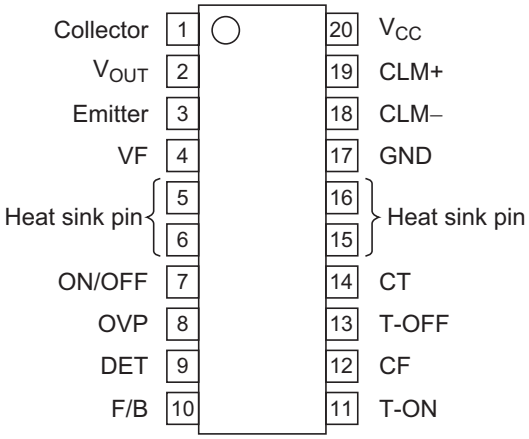
M51995AP



(Top view)

Outline: PRDP0016AA-A (16P4)

M51995AFP



(Top view)

Outline: PRSP0020DA-A (20P2N-A)

Note: Connect the heat sink pin to GND.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	36	V	
Collector voltage	V_C	36	V	
Output current	I_O	±2	A	Peak
		±0.15		Continuous
V_F terminal voltage	V_{VF}	V_{CC}	V	
ON/OFF terminal voltage	$V_{ON/OFF}$	V_{CC}	V	
CLM−terminal voltage	V_{CLM-}	−4.0 to +4.0	V	
CLM+terminal voltage	V_{CLM+}	−0.3 to +4.0	V	
OVP terminal current	I_{OVP}	8	mA	
DET terminal voltage	V_{DET}	6	V	
DET terminal input current	I_{DET}	5	mA	
F/B terminal voltage	V_{FB}	0 to 10	V	
T-ON terminal input current	I_{TON}	−1	mA	
T-OFF terminal input current	I_{TOFF}	−2	mA	
Power dissipation	Pd	1.5	W	Ta = 25°C
Thermal derating factor	Kθ	12	mW/°C	Ta > 25°C
Operating temperature	Topr	−30 to +85	°C	
Storage temperature	Tstg	−40 to +125	°C	
Junction temperature	Tj	150	°C	

Notes: 1. "+" sign shows the direction of current flow into the IC and "−" sign shows the current flow from the IC.
2. This terminal has the constant voltage characteristic of 6 to 8 V, when current is supplied from outside. The maximum allowable voltage is 6 V when the constant voltage is applied to this terminal. And maximum allowable current into this terminal is 5 mA.
3. The low impedance voltage supply should not be applied to the OVP terminal.

Electrical Characteristics

(V_{CC} = 18 V, Ta = 25°C, unless otherwise noted)

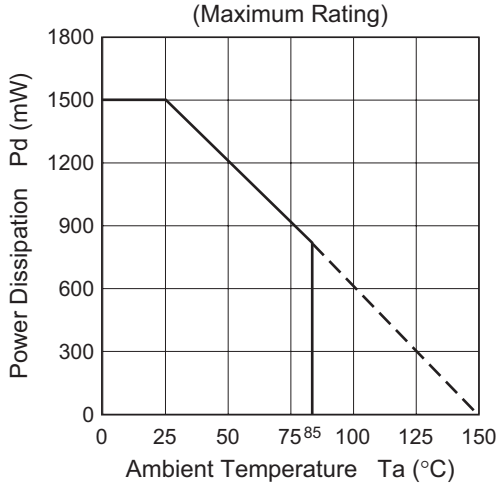
Block	Item	Symbol	Limits			Unit	Test Conditions
			Min.	Typ.	Max.		
Supply voltage circuit current	Operating supply voltage range	V_{CC}	$V_{CC(STOP)}$	—	35	V	
	Operation start-up voltage	$V_{CC(START)}$	15.2	16.2	17.2	V	
	Operation stop voltage	$V_{CC(STOP)}$	9.0	9.9	10.9	V	
	Difference voltage between operation start and stop	ΔV_{CC}	5.0	6.3	7.6	V	$\Delta V_{CC} = V_{CC(START)} - V_{CC(STOP)}$
	Stand-by current	I_{CCL}	50	90	140	μA	V_{CC} = 14.5V, Ta = 25°C
			40	90	190	μA	V_{CC} = 14.5V, −30 ≤ Ta ≤ 85°C
	Operating circuit current	I_{CCO}	10	15	21	mA	V_{CC} = 30V
	Circuit current in OFF state	$I_{CC\ OFF}$	0.95	1.31	5.0	mA	V_{CC} = 25V
			50	90	140	μA	V_{CC} = 14V
	Circuit current in timer OFF state	$I_{CC\ CT}$	0.95	1.35	2.0	mA	V_{CC} = 25V
			—	160	240	μA	V_{CC} = 14V
	Circuit current in OVP state	$I_{CC\ OVP}$	1.3	2.0	3.0	mA	V_{CC} = 25V
			125	200	310	μA	V_{CC} = 9.5V
ON/OFF	ON/OFF terminal high threshold voltage	$V_{THH\ ON/OFF}$	2.1	2.6	3.1	V	
	ON/OFF terminal low threshold voltage	$V_{THL\ ON/OFF}$	1.9	2.4	2.9	V	
	ON/OFF terminal hysteresis voltage	$\Delta V_{THON/OFF}$	0.1	0.2	3.0	V	
F/B	Current at 0% duty	I_{FBMIND}	−2.1	−1.54	−1.0	mA	F/B terminal input current
	Current at maximum duty	I_{FBMAXD}	−0.90	−0.55	−0.40	mA	F/B terminal input current
	Current difference between max and 0% duty	ΔI_{FB}	−1.35	−0.99	−0.70	mA	$\Delta I_{FB} = I_{FBMIND} - I_{FBMAXD}$
	Terminal voltage	V_{FB}	4.9	5.9	7.1	V	F/B terminal input current = 0.95mA
	Terminal resistance	R_{FB}	420	600	780	Ω	
Detection	Detection voltage	V_{DET}	2.4	2.5	2.6	V	
	Input current of detection amp	I_{INDET}	—	1.0	3.0	μA	V_{DET} = 2.5V
	Voltage gain of detection amp	G_{AVDET}	30	40	—	dB	
OVP	OVP terminal H threshold voltage	V_{THOVPH}	540	750	960	mV	
	OVP terminal hysteresis voltage	ΔV_{THOVP}	—	30	—	mV	$\Delta V_{THOVP} = V_{THOVPH} - V_{THOVPL}$
	OVP terminal threshold current	I_{THOVP}	80	150	250	μA	
	OVP terminal input current	I_{INOVP}	80	150	250	μA	V_{OVP} = 400mV
	OVP reset supply voltage	V_{CCOVPC}	7.5	9.0	10.0	V	OVP terminal is open. (high impedance)
	Difference supply voltage between operation stop and OVP reset	$V_{CC(STOP)} - V_{CCOVPC}$	0.55	1.20	—	V	
	Current from OVP terminal for OVP reset	I_{THOVPC}	−480	−320	−213	μA	V_{CC} = 30V
			−210	−140	−93		V_{CC} = 18V

(V_{CC} = 18 V, Ta = 25°C, unless otherwise noted)

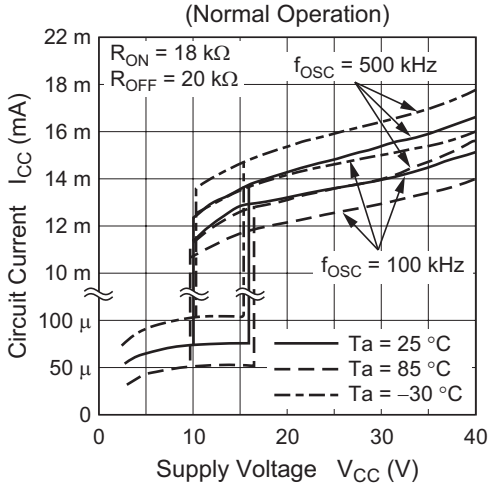
Block	Item	Symbol	Limits			Unit	Test Conditions
			Min.	Typ.	Max.		
Timer	Timer frequency	f_{TIMER}	0.27	0.40	0.60	Hz	C_T = 4.7µF
	Timer charge current	I_{TIMECH}	–193	–138	–102	µA	V_{CT} = 3.3V, Ta = –5°C
			–178	–127	–94		Ta = 25°C
			–147	–105	–78		Ta = 85°C
	OFF time/ON time ratio	$TIME_{OFF/ON}$	7.0	8.7	11.0	—	
CLM–	CLM–terminal threshold voltage	V_{THCLM-}	–220	–200	–180	mV	–5 ≤ Ta ≤ 85°C
	CLM–terminal current	I_{INCLM-}	–170	–125	–90	µA	V_{CLM-} = –0.1V
	Delay time from CLM– to V_{OUT}	T_{PDCLM-}	—	120	—	ns	
CLM+	CLM+ terminal threshold voltage	V_{THCLM+}	180	200	220	mV	–5 ≤ Ta ≤ 85°C
	CLM+ terminal current	I_{INCLM+}	–270	–205	–140	µA	V_{CLM+} = 0V
	Delay time from CLM+ to V_{OUT}	T_{PDCLM+}	—	90	—	ns	
Oscillator	Oscillating frequency	fosc	170	188	207	kHz	R_{ON} = 20kΩ, R_{OFF} = 17kΩ C_F = 220pF, –5 ≤ Ta ≤ 85°C
	Maximum ON duty	T_{DUTY}	47.0	50.0	53.0	%	
	Upper limit voltage of oscillation waveform	V_{OSCH}	3.97	4.37	4.77	V	f_{OSC} = 188kHz
	Lower limit voltage of oscillation waveform	V_{OSCL}	1.76	1.96	2.16	V	f_{OSC} = 188kHz
	Voltage difference between upper limit and lower limit of OSC waveform	ΔV_{OSC}	2.11	2.41	2.71	V	f_{OSC} = 188kHz
V_F	OSC frequency in CLM operating state (V_F = 5V)	f_{OSCVF}	170	188	207	kHz	R_{ON} = 20kΩ, R_{OFF} = 17kΩ C_F = 220pF
	OSC frequency in CLM operating state (V_F = 2V)		108	124	143		
	Duty in CLM operating state (V_F = 0.2V)	T_{VFDUTY}	11.0	13.7	22.0	—	Min off duty/Max on duty
	V_F voltage at timer operating start	V_{THTIME}	2.7	3.0	3.3	V	
	V_F terminal input current	I_{VF}	—	2	6	µA	Source current
Output	Output low voltage	$V_{OL}1$	—	0.05	0.4	V	V_{CC} = 18V, I_O = 10mA
		$V_{OL}2$	—	0.7	1.4	V	V_{CC} = 18V, I_O = 100mA
		$V_{OL}3$	—	0.69	1.0	V	V_{CC} = 5V, I_O = 1mA
		$V_{OL}4$	—	1.3	2.0	V	V_{CC} = 5V, I_O = 100mA
	Output high voltage	$V_{OH}1$	16.0	16.5	—	V	V_{CC} = 18V, I_O = –10mA
		$V_{OH}2$	15.5	16.0	—	V	V_{CC} = 18V, I_O = –100mA
	Output voltage rise time	T_{RISE}	—	50	—	ns	No load
	Output voltage fall time	T_{FALL}	—	35	—	ns	No load

Main Characteristics

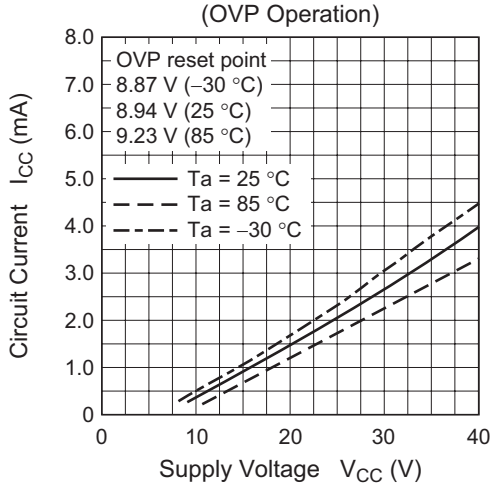
Thermal Derating
(Maximum Rating)



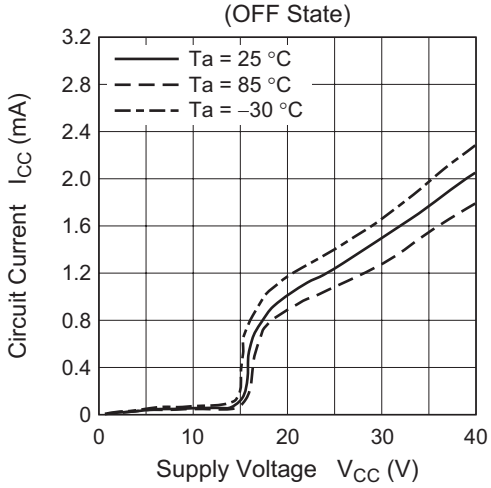
Circuit Current vs. Supply Voltage
(Normal Operation)



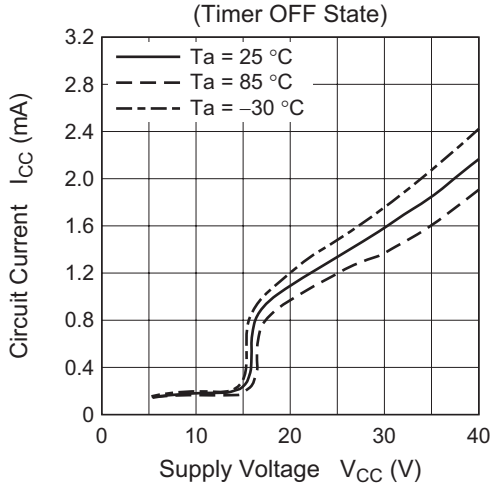
Circuit Current vs. Supply Voltage
(OVP Operation)



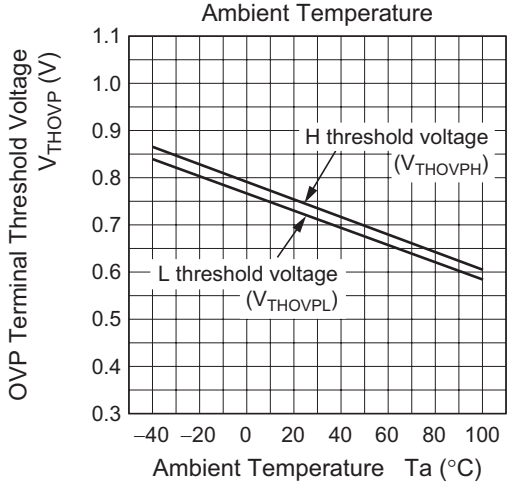
Circuit Current vs. Supply Voltage
(OFF State)



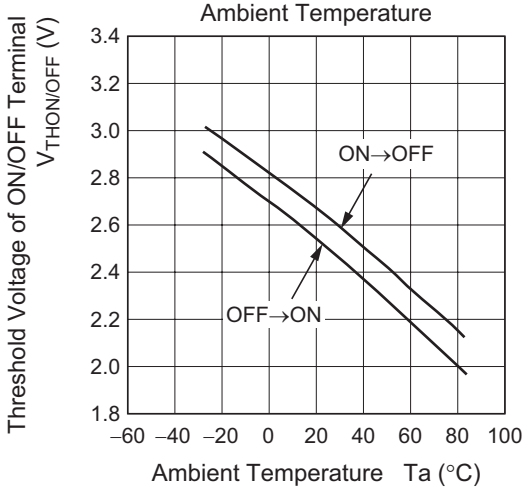
Circuit Current vs. Supply Voltage
(Timer OFF State)



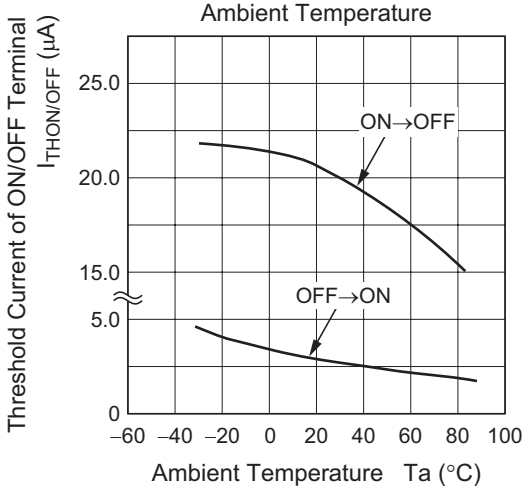
OVP Terminal Threshold Voltage vs.
Ambient Temperature



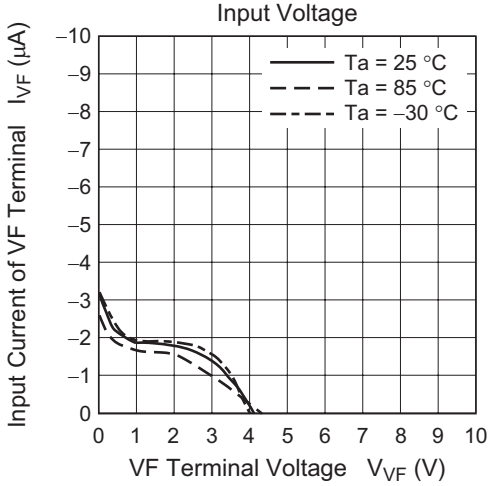
Threshold Voltage of ON/OFF Terminal vs. Ambient Temperature



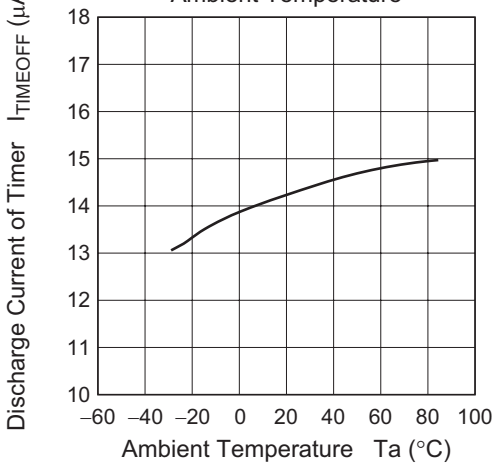
Threshold Current of ON/OFF Terminal vs. Ambient Temperature



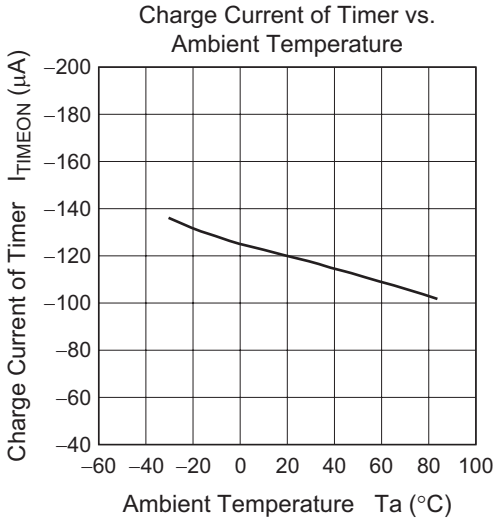
Input Current of VF Terminal vs. Input Voltage



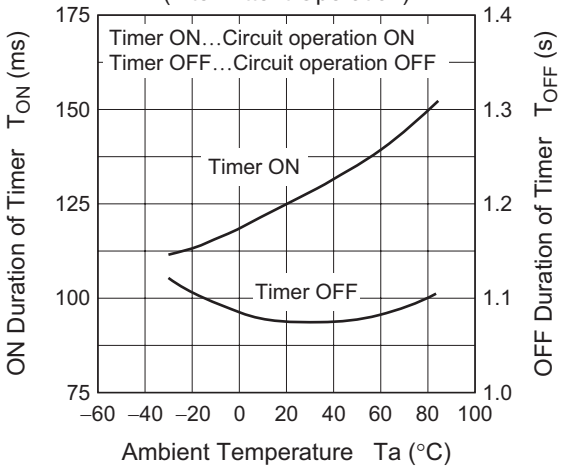
Discharge Current of Timer vs. Ambient Temperature



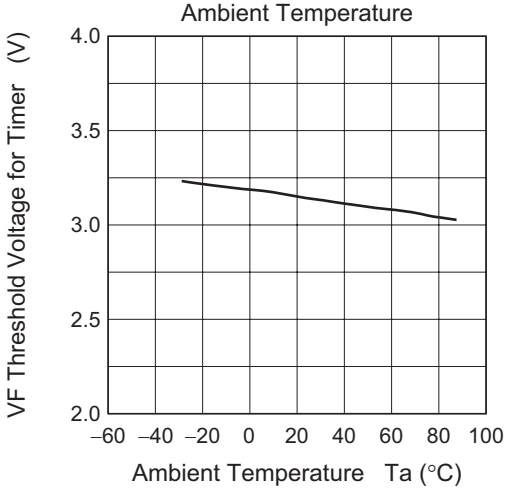
Charge Current of Timer vs. Ambient Temperature



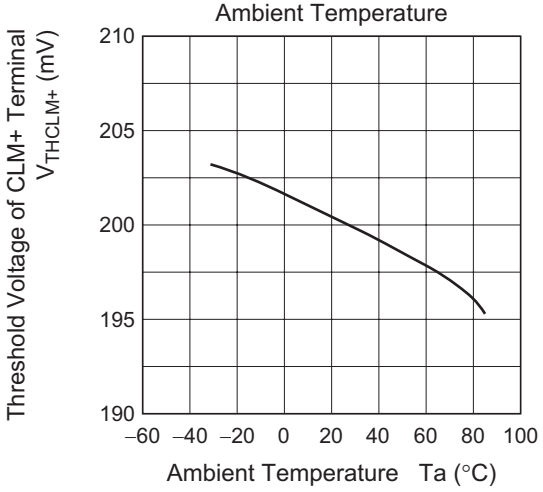
ON and OFF Duration of Timer vs. Ambient Temperature (Intermittent Operation)



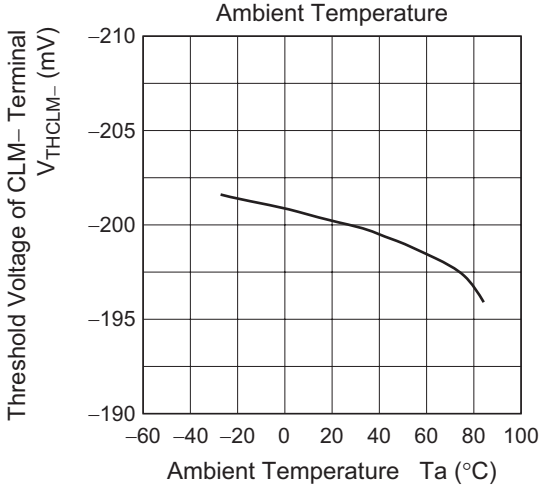
VF Threshold Voltage for Timer vs. Ambient Temperature



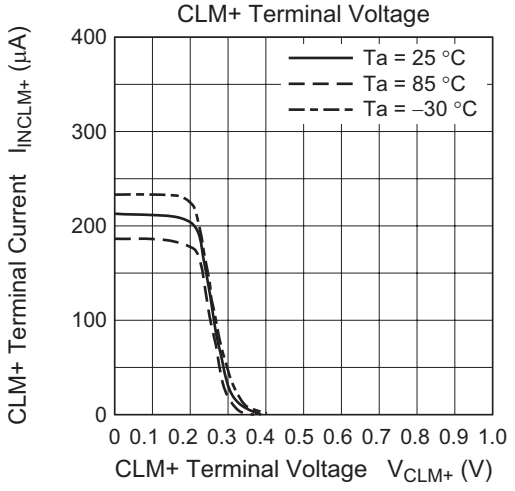
Threshold Voltage of CLM+ Terminal vs. Ambient Temperature



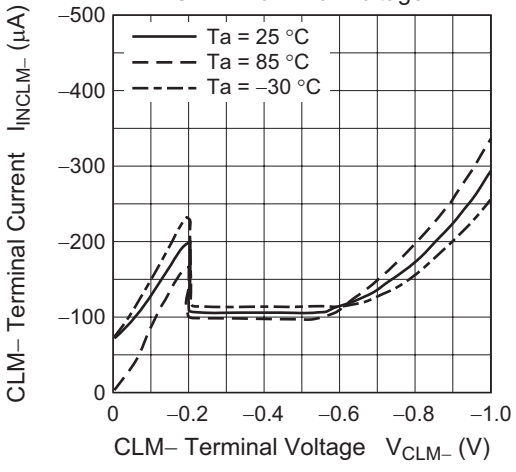
Threshold Voltage of CLM– Terminal vs. Ambient Temperature



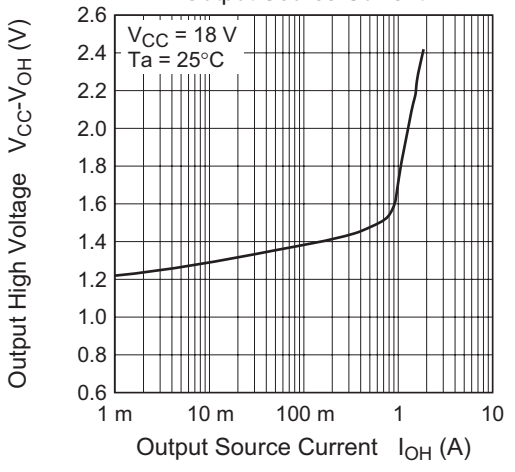
CLM+ Terminal Current vs. CLM+ Terminal Voltage



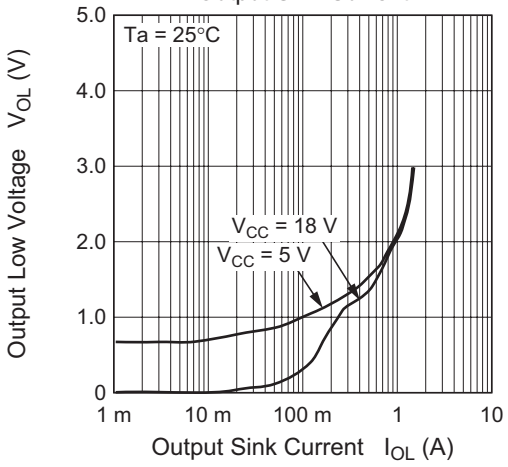
CLM– Terminal Current vs. CLM– Terminal Voltage



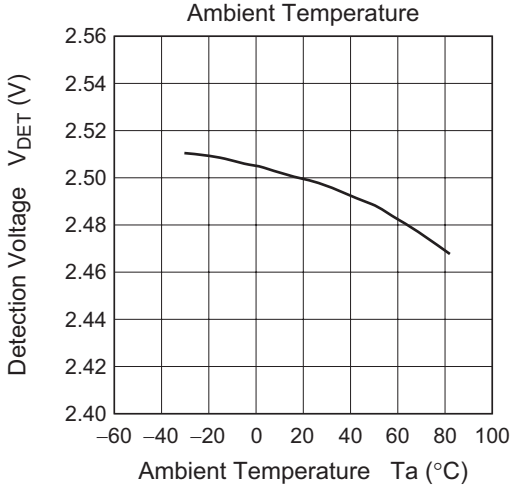
Output High Voltage vs. Output Source Current



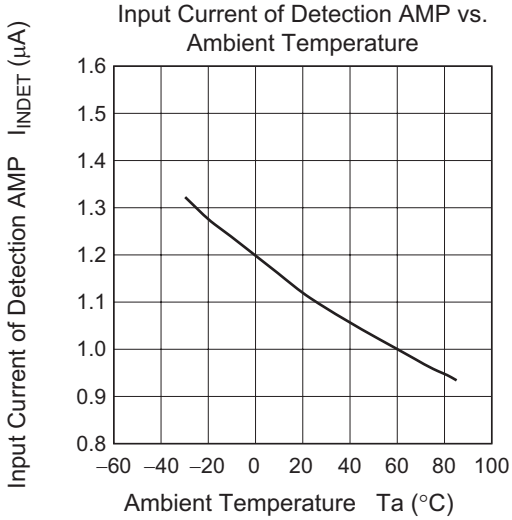
Output Low Voltage vs.
Output Sink Current



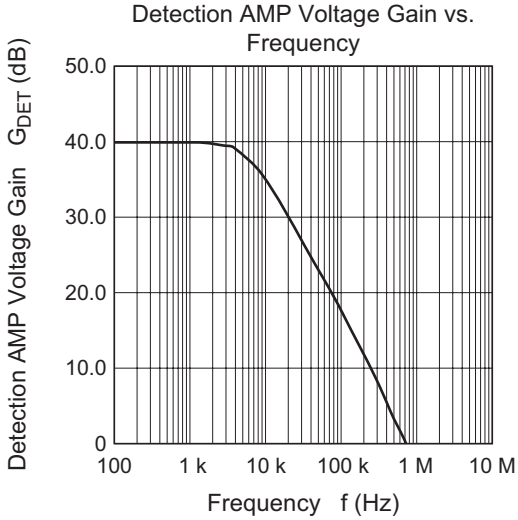
Detection Voltage vs.
Ambient Temperature



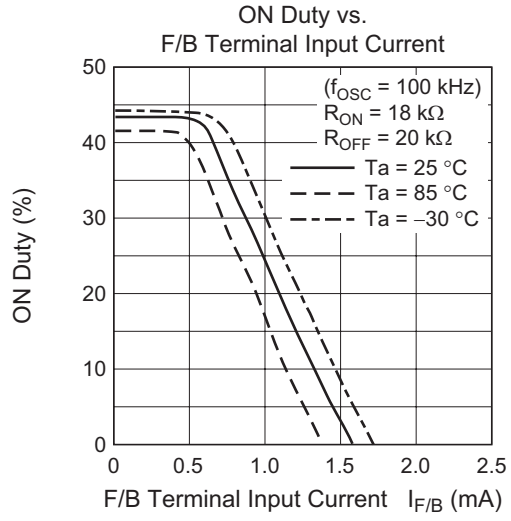
Input Current of Detection AMP vs.
Ambient Temperature



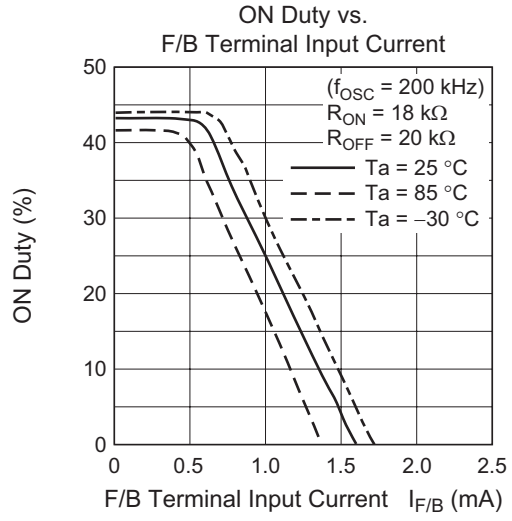
Detection AMP Voltage Gain vs.
Frequency



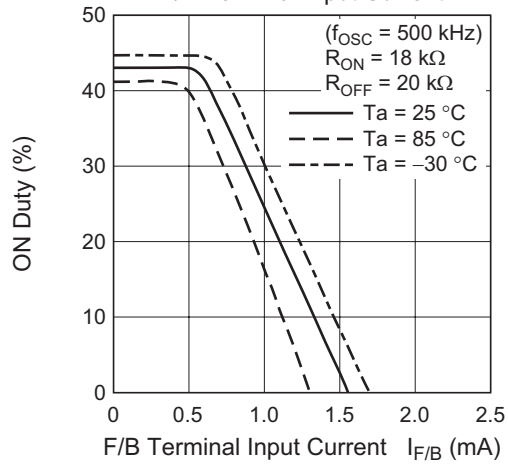
ON Duty vs.
F/B Terminal Input Current



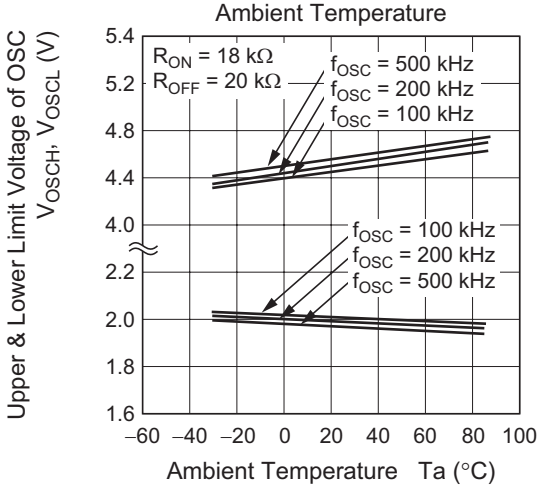
ON Duty vs.
F/B Terminal Input Current



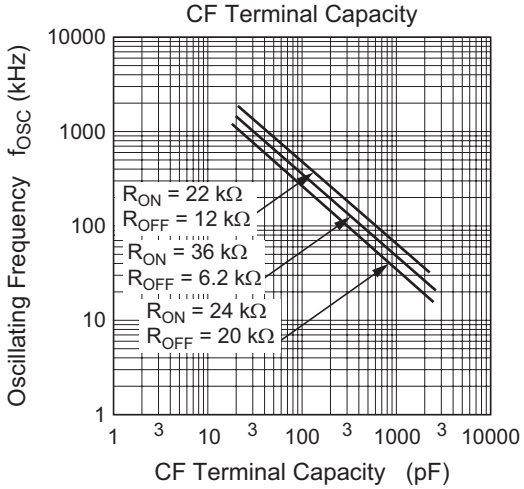
ON Duty vs.
F/B Terminal Input Current



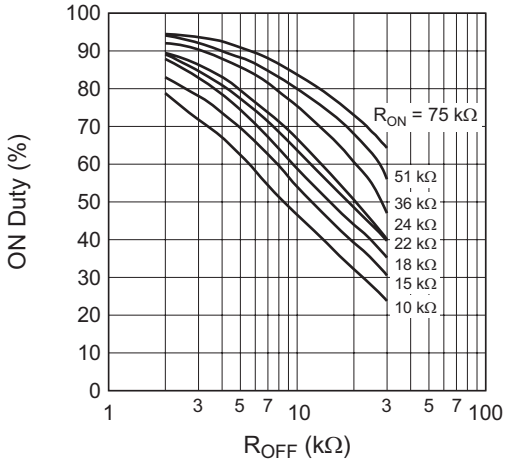
Upper & Lower Limit Voltage of OSC vs.
Ambient Temperature



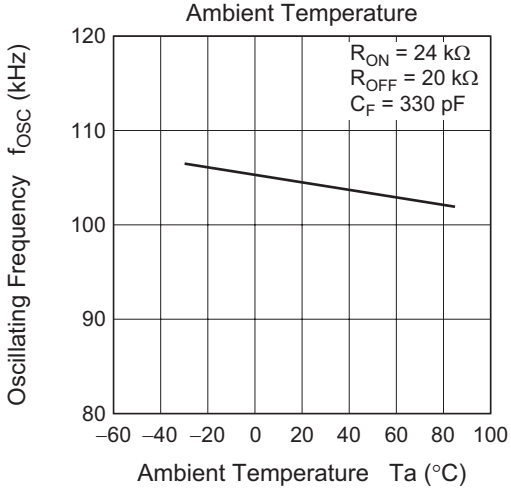
Oscillating Frequency vs.
CF Terminal Capacity



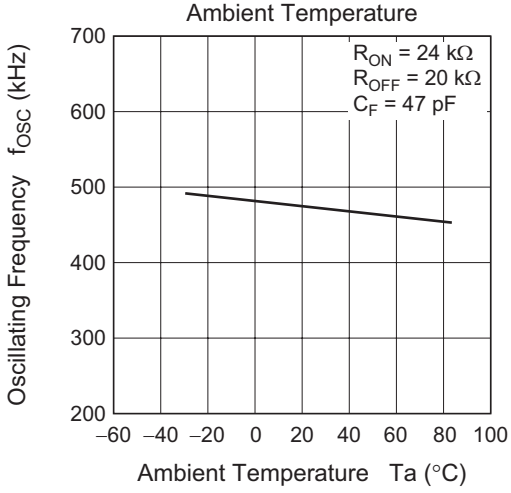
ON Duty vs. R_{OFF}



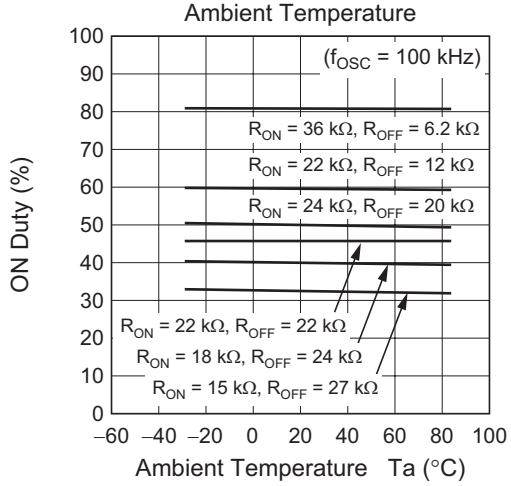
Oscillating Frequency vs.
Ambient Temperature



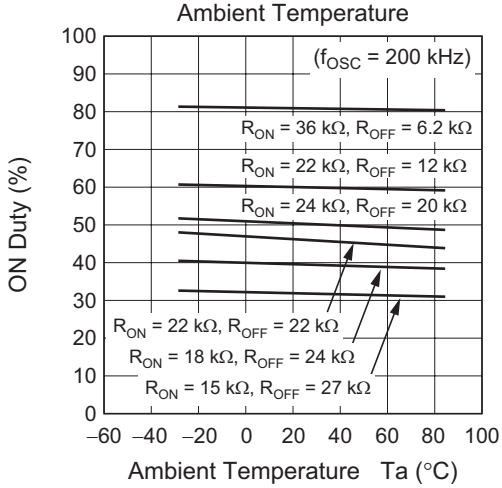
Oscillating Frequency vs.
Ambient Temperature



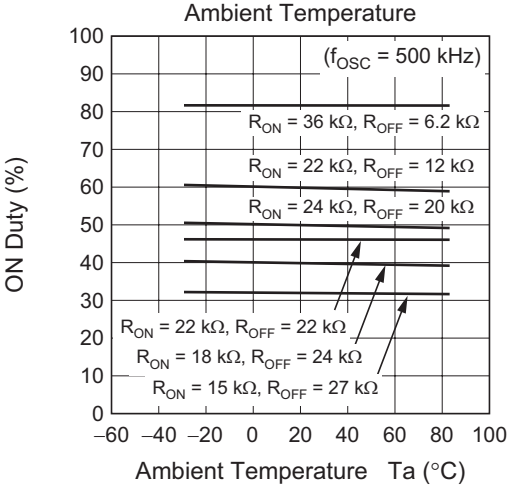
ON Duty vs.
Ambient Temperature



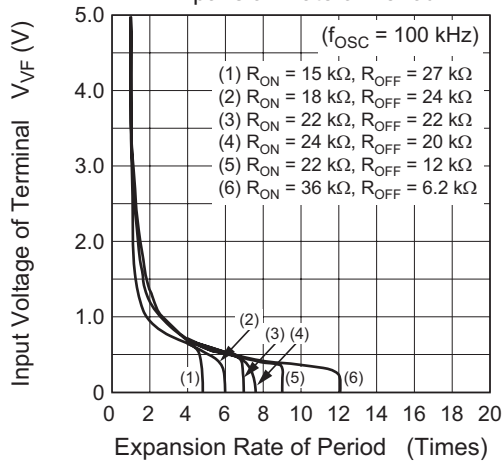
ON Duty vs.
Ambient Temperature



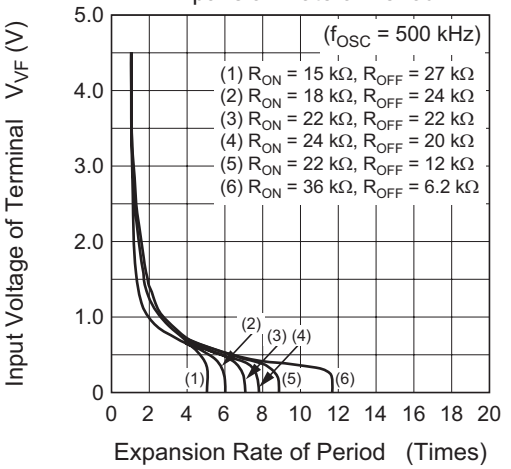
ON Duty vs.
Ambient Temperature



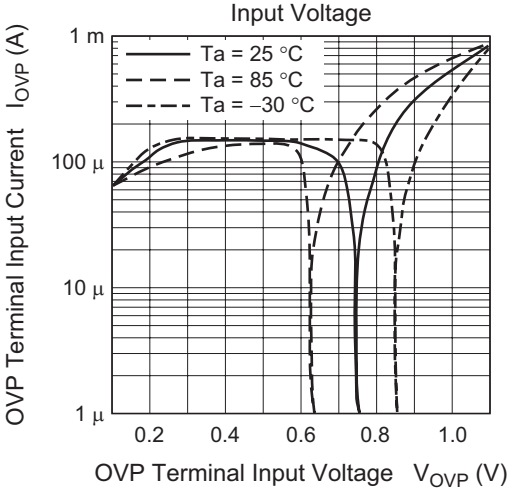
Input Voltage of Terminal vs.
Expansion Rate of Period



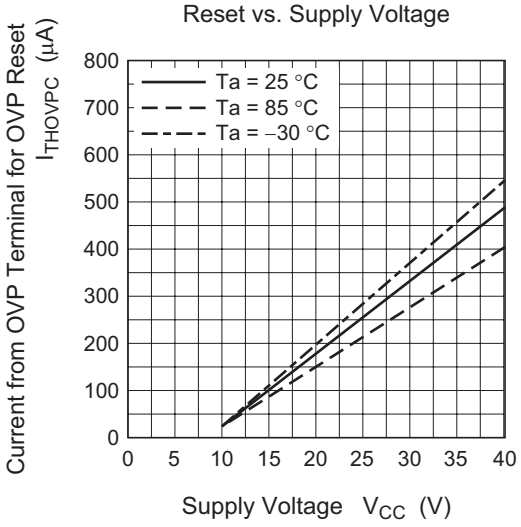
Input Voltage of Terminal vs.
Expansion Rate of Period



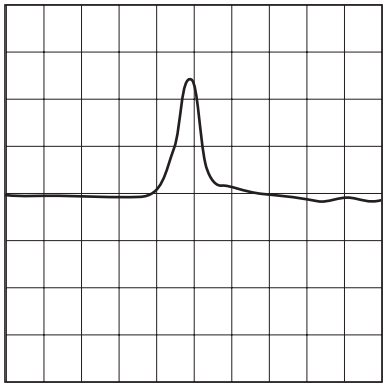
OVP Terminal Input Current vs.
Input Voltage



Current from OVP Terminal for OVP Reset vs. Supply Voltage

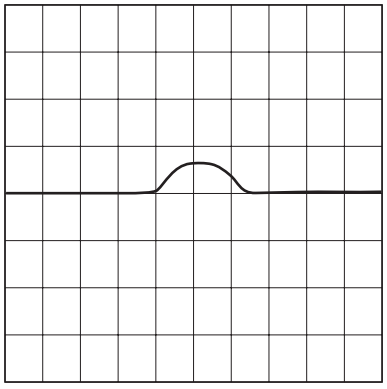


Output Through Current Waveform at Rising Edge of Output Pulse



Horizontal-axis: 20 ns/div
Vertical-axis: 50 mA/div

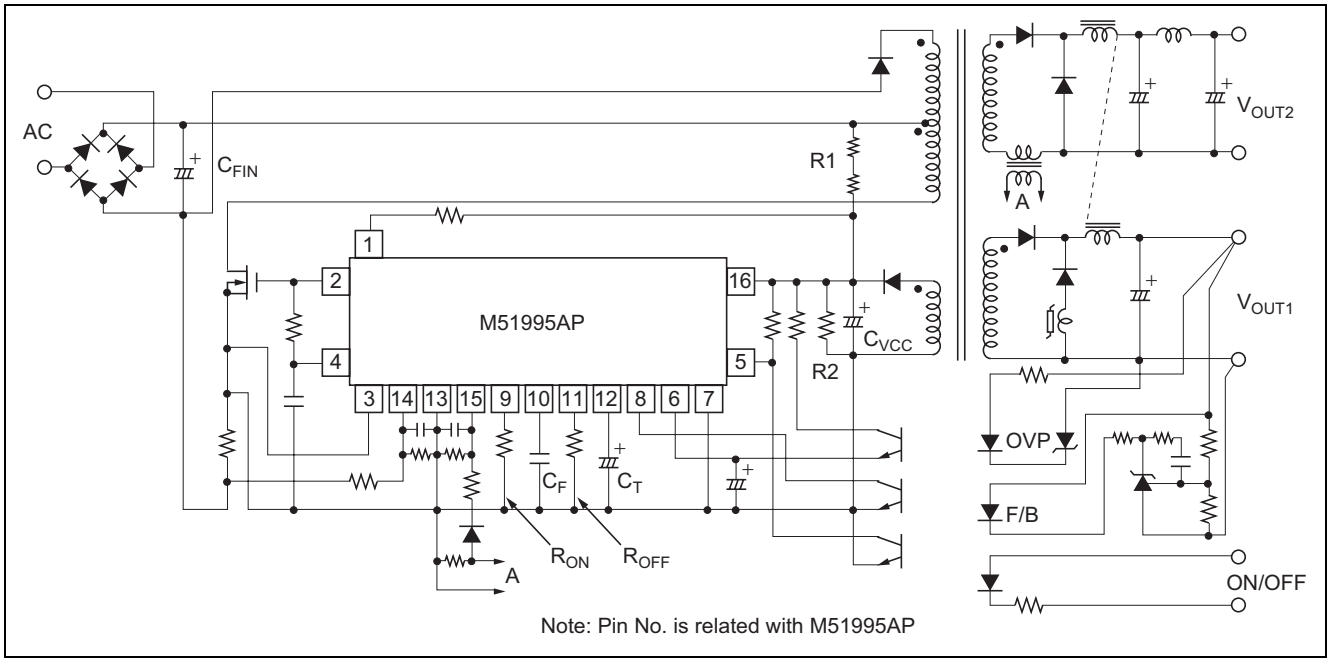
Output Through Current Waveform at Falling Edge of Output Pulse



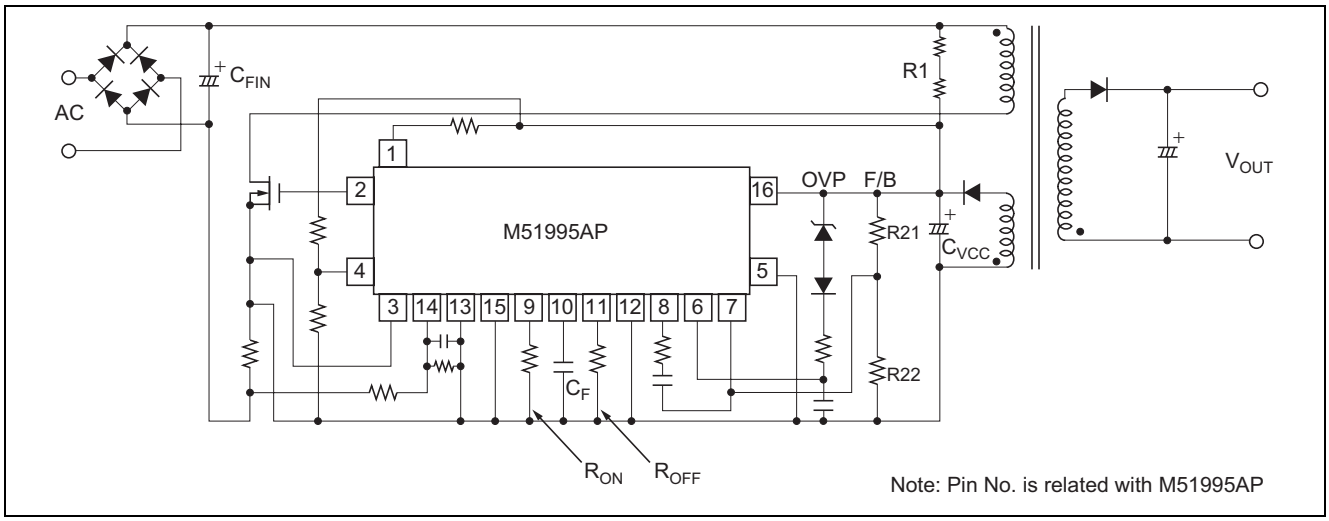
Horizontal-axis: 20 ns/div
Vertical-axis: 10 mA/div

Application Example

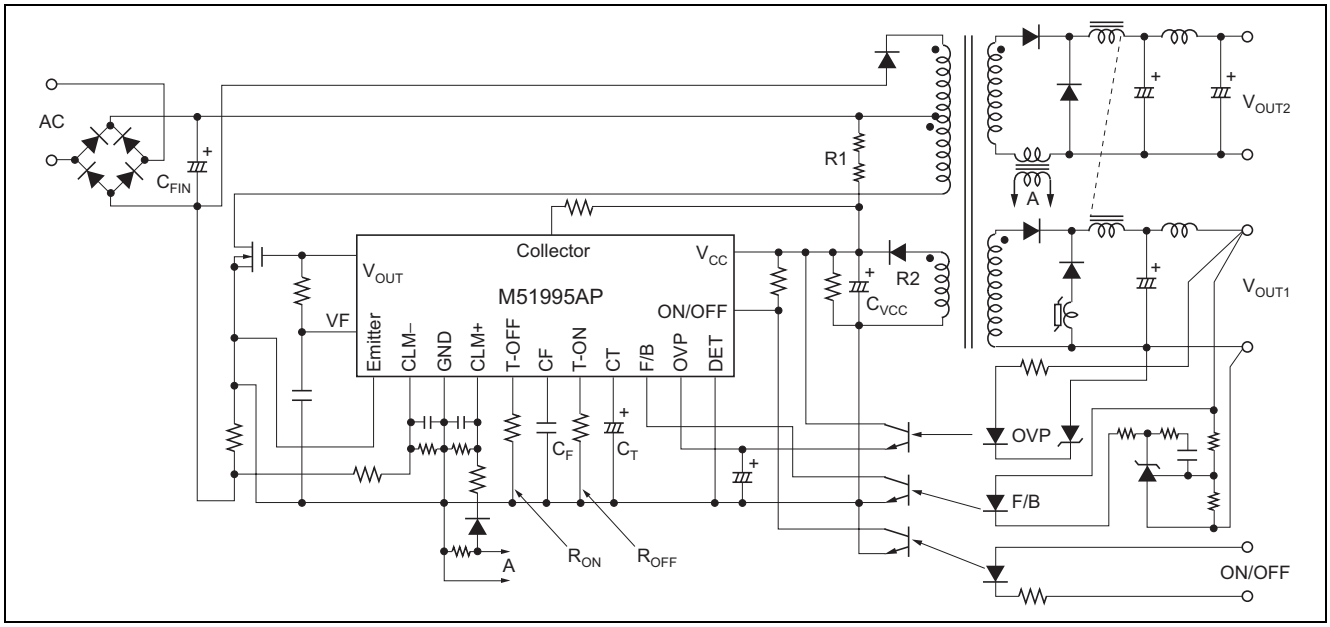
(1) Example application circuit diagram of feed forward regulator



(2) Example application circuit diagram of fly-back regulator



(3) Feed forward types SMPS with multi-output



Function Description

Type M51995AP and M51995AFP are especially designed for off-line primary PWM control IC of switching mode power supply (SMPS) to get DC voltage from AC power supply.

Using this IC, smart SMPS can be realized with reasonable cost and compact size as the number of external electric parts can be reduced and also parts can be replaced by reasonable one.

In the following circuit diagram, MOS FET is used for output transistor, however bipolar transistor can be used with no problem.

Start-up Circuit Section

The start-up current is such low current level as typical 90 μA, as shown in figure 1, when the V_{CC} voltage is increased from low level to start-up voltage $V_{CC(START)}$.

In this voltage range, only a few parts in this IC, which has the function to make the output voltage low level, is alive and I_{CC} current is used to keep output low level. The large voltage difference between $V_{CC(START)}$ and $V_{CC(STOP)}$ makes start-up easy, because it takes rather long duration from $V_{CC(START)}$ to $V_{CC(STOP)}$.

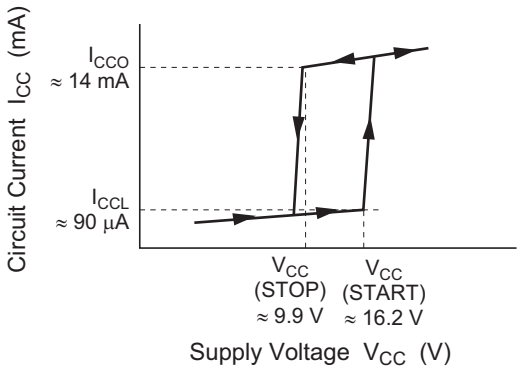


Figure 1 Circuit Current vs. Supply Voltage

Oscillator Section

The oscillation waveform is the triangle one. The ON-duration of output pulse depends on the rising duration of the triangle waveform and dead-time is decided by the falling duration.

The rising duration is determined by the product of external resistor R_{ON} and capacitor C_F and the falling duration is mainly determined by the product of resistor R_{OFF} and capacitor C_F.

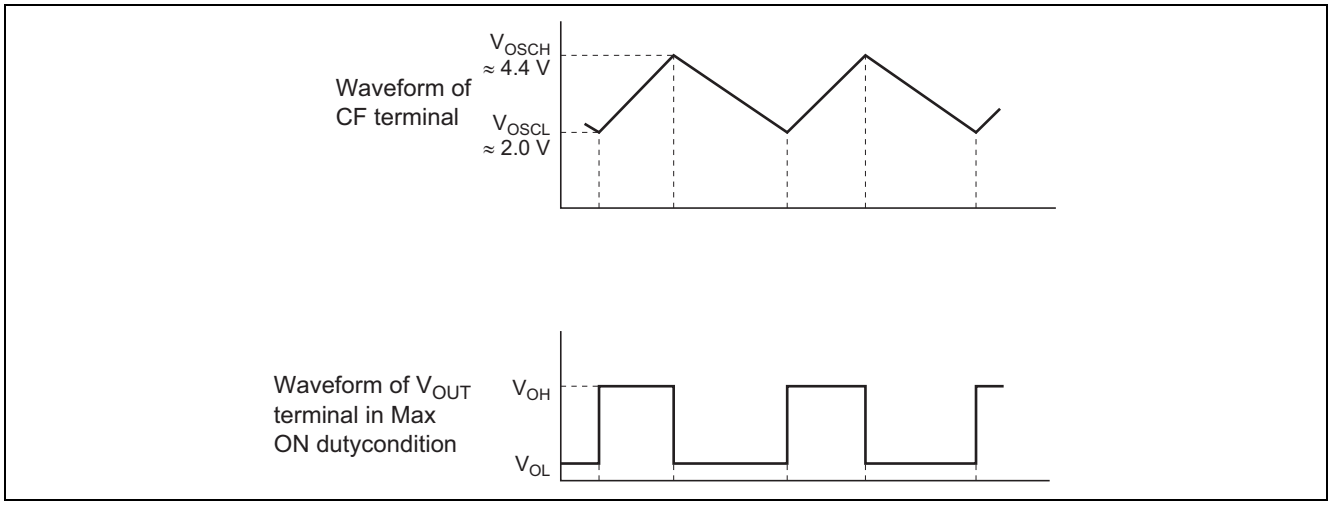


Figure 2 OSC Waveform at Normal Condition (no-operation of intermittent action and OSC control circuit)

1. Oscillator operation when intermittent action and OSC control circuit does not operate

   Figure 3 shows the equivalent charging and discharging circuit diagram of oscillator when the current limiting circuit does not operate. It means that intermittent action and OSC control circuit does not operate.

   The current flows through R_{ON} from the constant voltage source of 5.8 V. C_F is charged up by the same amplitude as R_{ON} current, when internal switch SW1 is switched to "charging side". The rise rate of C_F terminal is given as

$$\approx \frac{V_{T\text{-}ON}}{R_{ON} \times C_F} \text{ (V/s)} \quad \cdots\cdots (1)$$

   where $V_{T\text{-}ON} \approx 4.5$ V

   The maximum on duration is approximately given as

$$\approx \frac{(V_{OSCH} - V_{OSCL}) \times R_{ON} \times C_F}{V_{T\text{-}ON}} \text{ (s)} \quad \cdots\cdots (2)$$

   where $V_{OSCH} \approx 4.4$ V

   $V_{OSCL} \approx 2.0$ V

   C_F is discharged by the summed-up of R_{OFF} current and one sixteenth (1/16) of R_{ON} current by the function of Q2, Q3 and Q4 when SW1, SW2 are switched to "discharge side".

   So fall rate of CF terminal is given as

$$\approx \frac{V_{T\text{-}OFF}}{R_{OFF} \times C_F} + \frac{V_{T\text{-}ON}}{16 \times R_{ON} \times C_F} \text{ (V/s)} \quad \cdots\cdots (3)$$

   The minimum off duration approximately is given as

$$\approx \frac{(V_{OSCH} - V_{OSCL}) \times C_F}{\frac{V_{T\text{-}OFF}}{R_{OFF}} + \frac{V_{T\text{-}ON}}{16 \times R_{ON}}} \text{ (s)} \quad \cdots\cdots (4)$$

   where $V_{T-OFF} \approx 3.5$ V

   The cycle time of oscillation is given by the summation of equations 2 and 4.

   The frequency including the dead-time is not influenced by the temperature because of the built-in temperature compensating circuit.

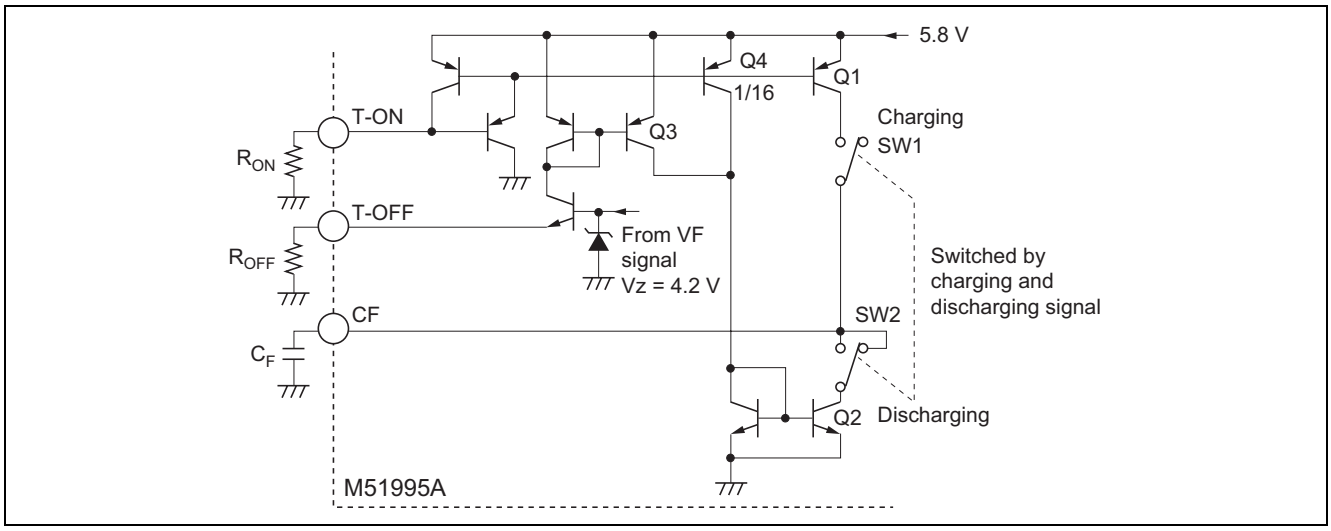


Figure 3 Schematic Diagram of Charging and Discharging Control Circuit for OSC Capacitor C_F

2. Oscillator operation when intermittent action and OSC control circuit operates.
When over current signal is applied to CLM+ or CLM– terminal, and the current limiting circuit, intermittent action and OSC control circuit starts to operate. In this case T-OFF terminal voltage depends on VF terminal voltage, so the oscillation frequency decreases and dead-time spreads.
The rise rate of oscillation waveform is given as

$$\approx \frac{V_{T\text{-}ON}}{R_{ON} \times C_F} \text{ (V/s)} \quad \cdots\cdots (5)$$

The fall rate of oscillation waveform is given as

$$\approx \frac{V_{VF} - V_{VFO}}{R_{OFF} \times C_F} + \frac{V_{T\text{-}ON}}{16 \times R_{ON} \times C_F} \text{ (V/s)} \quad \cdots\cdots (6)$$

where $V_{T\text{-}ON} \approx 4.5$ V

V_{VF} ; V_F terminal voltage

$V_{VFO} \approx 0.4$ V

$V_{VF} - V_{FO} = 0$ if $V_{VF} - V_{VFO} < 0$

$V_{VF} - V_{VFO} = V_{T\text{-}OFF}$ if $V_{VF} - V_{VFO} > V_{T-OFF} \approx 3.5$ V

So when $V_{VF} > 3.5$ V, the operation is just same as that in the no current limiting operation state.
The maximum on-duration is just same as that in the no-operation state of intermittent and oscillation control circuit and is given as follows;

$$\approx \frac{(V_{OSCH} - V_{OSCL}) \times R_{OFF} \times C_F}{V_{T\text{-}ON}} \text{ (s)} \quad \cdots\cdots (7)$$

The minimum off-duration is approximately given as;

$$\approx \frac{(V_{OSCH} - V_{OSCL}) \times C_F}{\frac{V_{VF} - V_{VFO}}{R_{OFF} \times C_F} + \frac{V_{T\text{-}ON}}{16 \times R_{ON} \times C_F}} \text{ (s)} \quad \cdots\cdots (8)$$

The oscillation period is given by the summation of equation (7) and (8).

As shown in figure 5, the internal circuit kills the first output pulse in the output waveform. The output waveform will appear from the second pulse cycle because the duration of first cycle takes C_F charging time longer comparing with that at the stable operating state.

Usually the applied voltage to VF terminal must be proportional the output voltage of the regulator.

So when the over current occurs and the output voltage of the regulator becomes low, the off-duration becomes wide.

There are two methods to get the control voltage, which depends on the output voltage, on primary side. For the fly back type regulator application, the induced voltage on the third or bias winding is dependent on output voltage. On the other hand, for the feed forward type regulator application, it can be used that the output voltage depends on the product of induced voltage and "on-duty", as the current of choke coil will continue at over load condition, it means the "continuous current" condition.

Figure 6 shows one of the examples for VF terminal application for the feed forward type regulator.

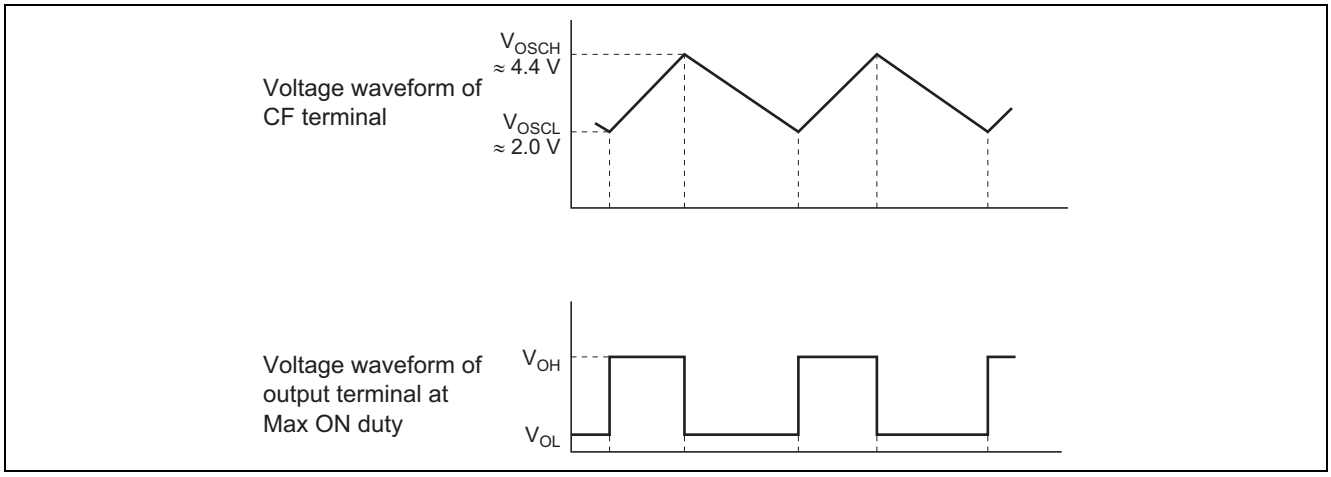


Figure 4 OSC Waveform with Operation of Intermittent and OSC Control Circuit Operation

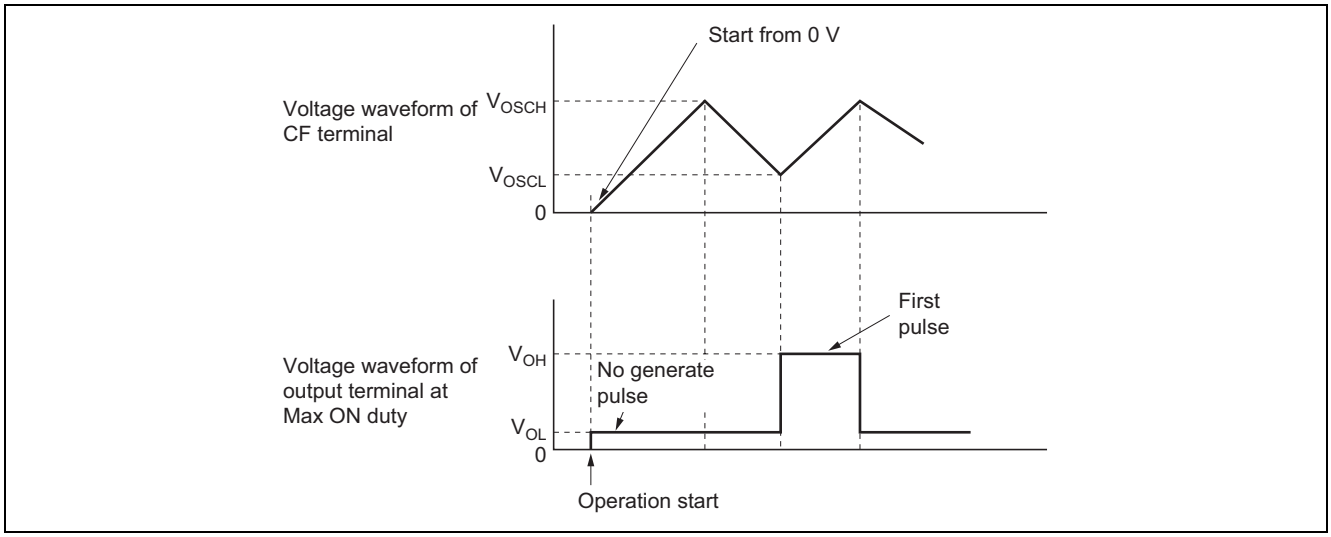


Figure 5 Relation between OSC and Output Waveform Circuit Operation at Start-up

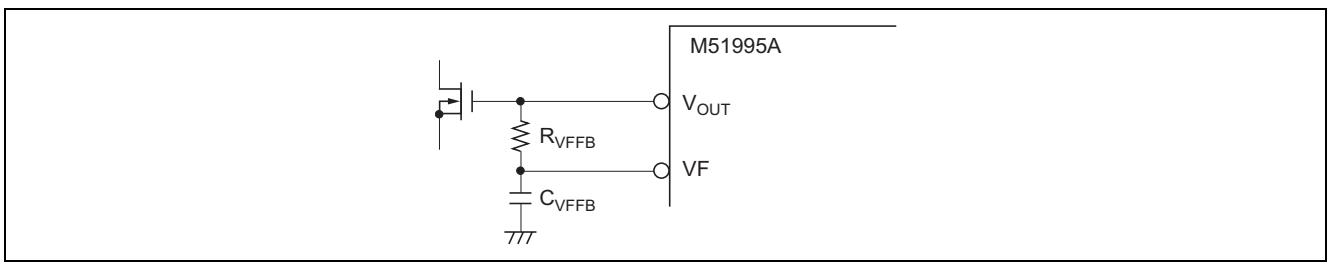


Figure 6 Feedback Loop with Low Pass Filter from Output to VF Terminal

PWM Comparator and PWM Latch Section

Figure 7 shows the PWM comparator and latch section. The on-duration of output waveform coincides with the rising duration of CF terminal waveform, when the infinitive resistor is connected between F/B terminal and GND.

When the F/B terminal has finite impedance and current flows out from F/B terminal, “A” point potential shown in figure 7 depends on this current. So the “A” point potential is close to GND level when the flow-out current becomes large.

“A” point potential is compared with the CF terminal oscillator waveform and PWM comparator, and the latch circuit is set when the potential of oscillator waveform is higher than “A” point potential.

On the other hand, this latch circuit is reset by high level signal during the dead-time of oscillation (falling duration of oscillation waveform). So the “B” point potential or output waveform of latch circuit is the one shown in figure 8.

The final output waveform or “C” point potential is got by combining the “B” point signal and dead-time signal logically. (please refer to figure 8)

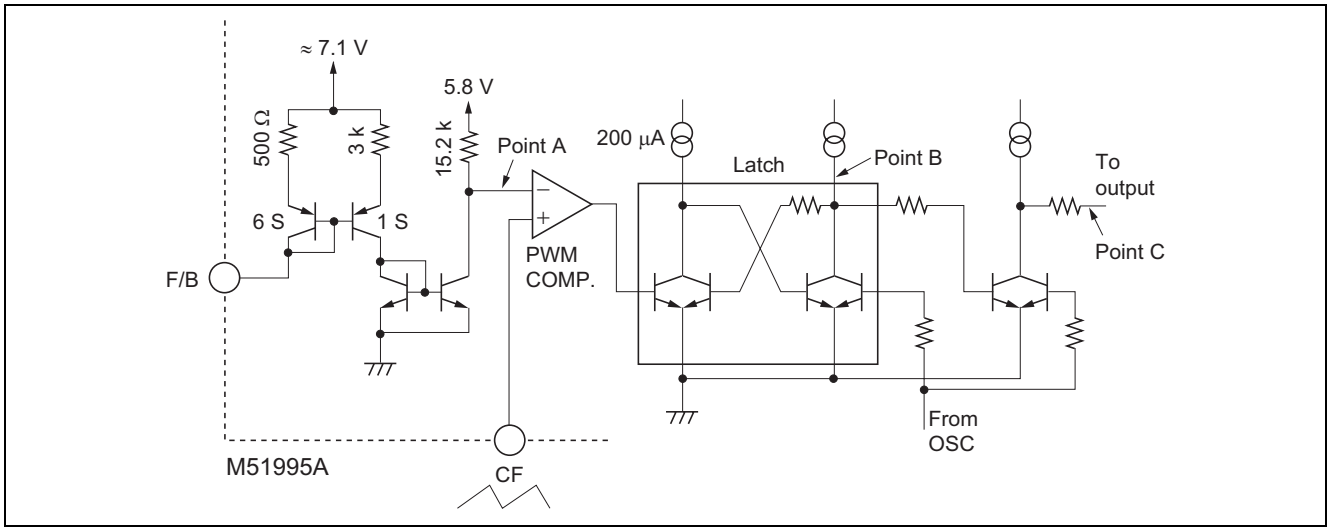


Figure 7 PWM Comparator and Latch Circuit

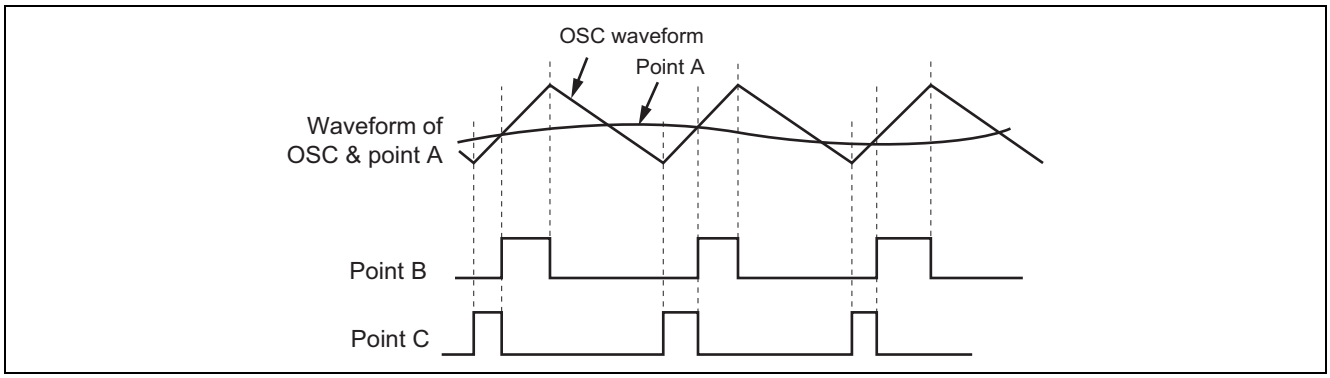


Figure 8 Waveforms of PWM Comparator Input point A, Latch Circuit Points B and C

Current Limiting Section

When the current-limit signal is applied before the crossing instant of “A” pint potential and CF terminal voltage shown in figure 7, this signal makes the output “off” and the off state will continue until next cycle. Figure 9 shows the timing relation among them.

The current limiting circuit has two input terminals, one has the detector-sensitivity of +200 mV to the GND terminal and the other has −200 mV. The circuit will be latched if the input signal is over the limit of either terminal.

If the current limiting circuit is set, no waveform is generated at output terminal however this state is reset during the succeeding dead-time.

So this current limiting circuit is able to have the function in every cycle, and is named “pulse-by-pulse current limit”.

It is rather recommended to use not "CLM+" but "CLM−" terminal, as the influence from the gate drive current of MOS FET can be eliminated and wide voltage rating of +4 V to −4 V is guaranteed for absolute maximum rating.

There happen some noise voltage on R_{CLM} during the switching of power transistor due to the snubber circuit and stray capacitor of the transformer windings.

To eliminate the abnormal operation by the noise voltage, the low pass filter, which consists of R_{NF} and C_{NF} is used as shown in figure 10.

It is recommended to use 10 to 100 Ω for R_{NF} because such range of R_{NF} is not influenced by the flow-out current of some 200 μA from C_{LM} terminal and C_{NF} is designed to have the enough value to absorb the noise voltage.

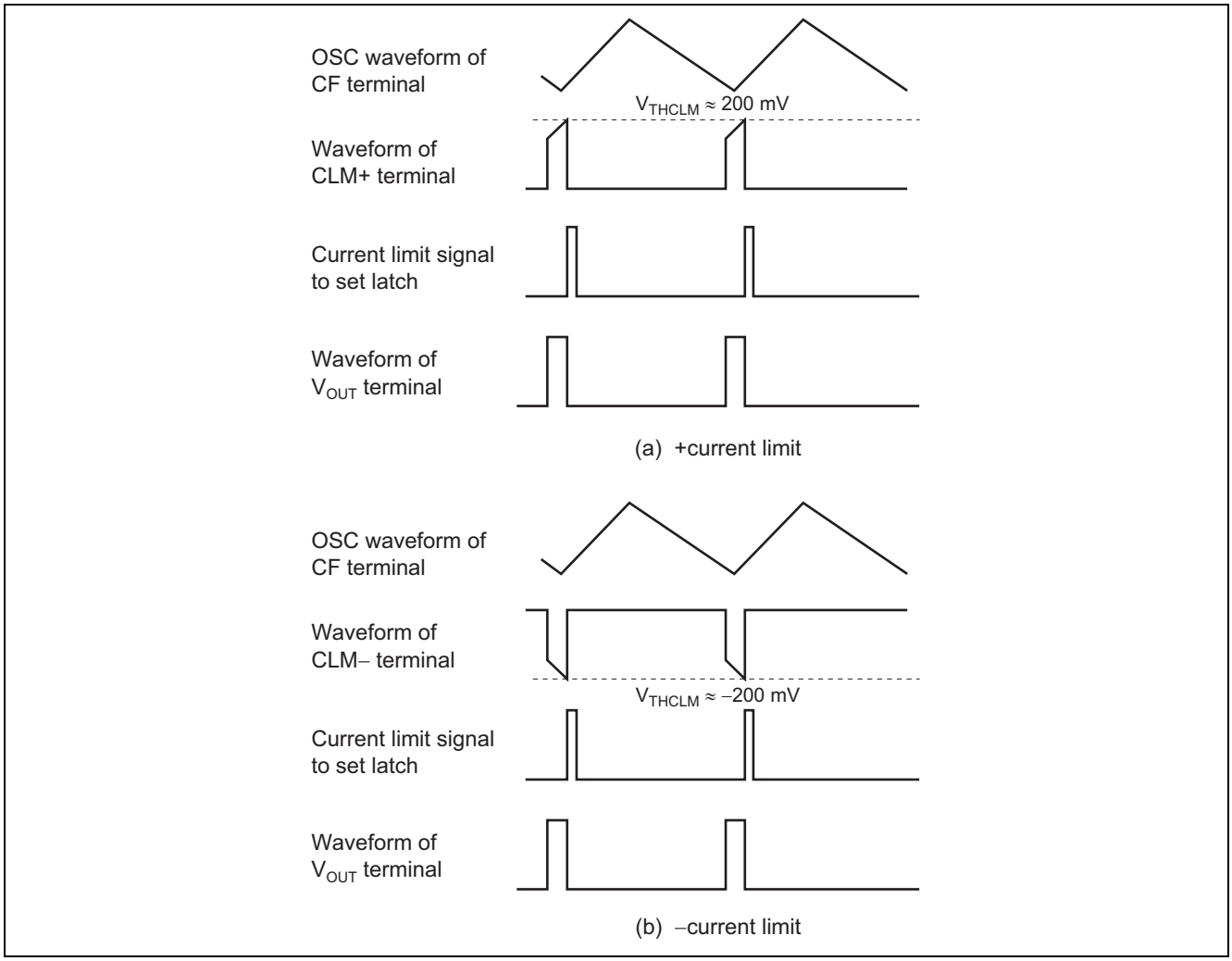


Figure 9 Operating Waveforms of Current Limiting Circuit

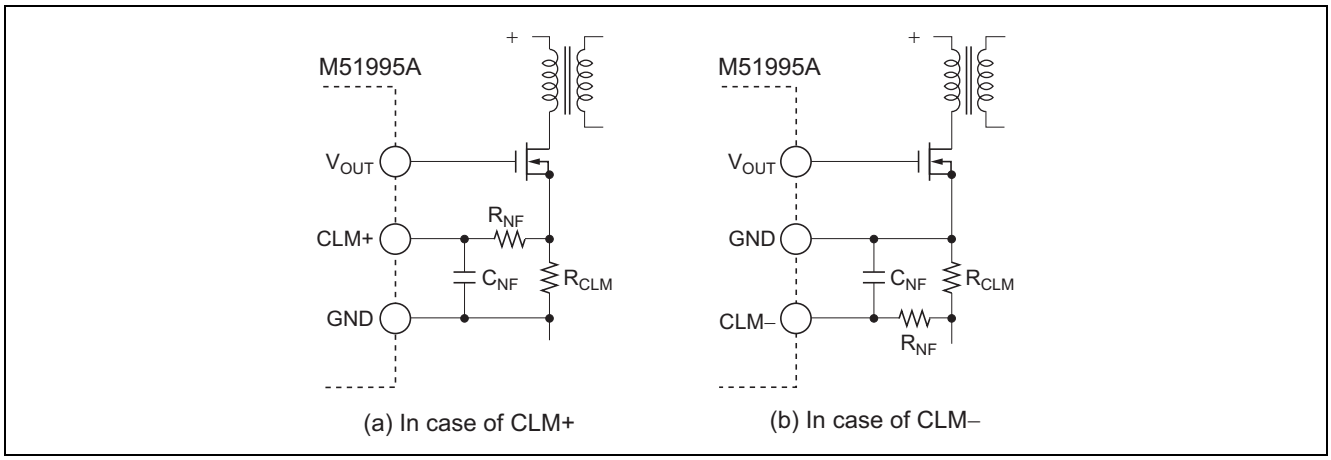


Figure 10 How to Connect Current Limit Circuit

Intermittent Action and Oscillation Control Section

When the internal current limiting circuit states to operate and also the VF level decreases to lower than the certain level of some 3 V, the dead-time spreads and intermittent action and OSC control circuit (which is one of the timer-type-protection circuit) starts to operate.

The intermittent action and OSC control circuit is the one to generate the control signal for oscillator and intermittent action circuit.

Figure 11 shows the timing-chart of this circuit. When the output of intermittent action and oscillation control is at "high" level, the waveform of oscillator depends on the VF terminal voltage and the intermittent action circuit begins to operate.

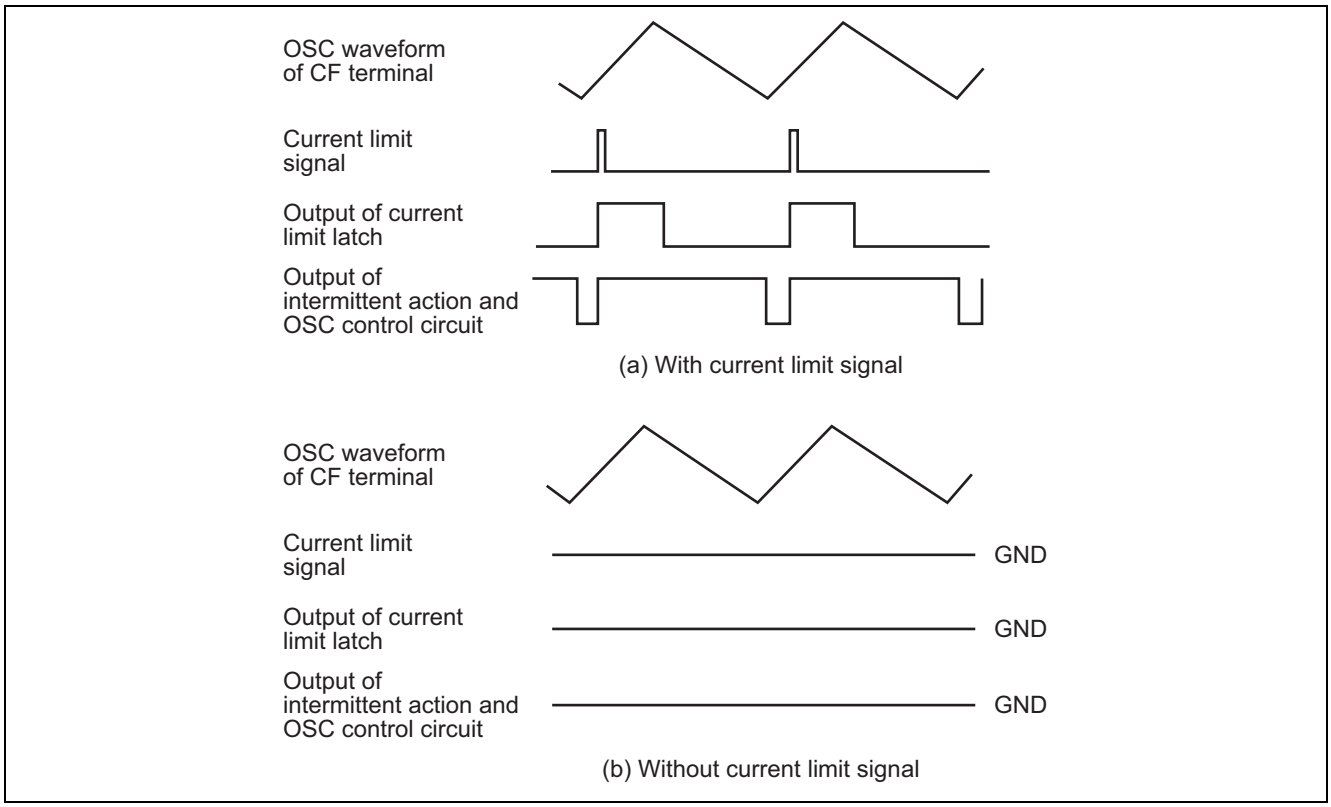


Figure 11 Timing Chart of Intermittent and OSC Control Circuit

Intermittent Action Circuit Section

Intermittent action circuit will start to operate when the output signal from the intermittent action and oscillation control circuit are “high” and also VF terminal voltage is lower than V_{THTIME} of about 3 V.

Figure 12 shows the block diagram of intermittent action circuit. Transistor Q is on state when VF terminal voltage is higher than V_{THTIME} of about 3 V, so the CT terminal voltage is near to GND potential.

When VF terminal voltage is lower than V_{THTIME}, Q becomes “off” and the CT has the possibility to be charged up.

Under this condition, if the intermittent action and oscillation control signal become “high” the switch SWA will close only in this “high” duration and C_T is charged up by the current of 120 μA through SW_A (SW_B is open) and CT terminal potential will rise. The output pulse can be generated only this duration. When the CT terminal voltage reaches to 8 V, the control logic circuit makes the SW_A “off” and SW_B “on”, in order to flow in the $I_{TIMEOFF}$ of 15 μA to CT terminal.

The IC operation will be ceased in the falling duration.

On the other hand, when CT terminal voltage decreases to lower than 2 V, the IC operation will be reset to original state, as the control logic circuit makes the SW_A “on” and SW_B “off”.

Therefore the parts in power circuit including secondary rectifier diodes are protected from the overheat by the over current.

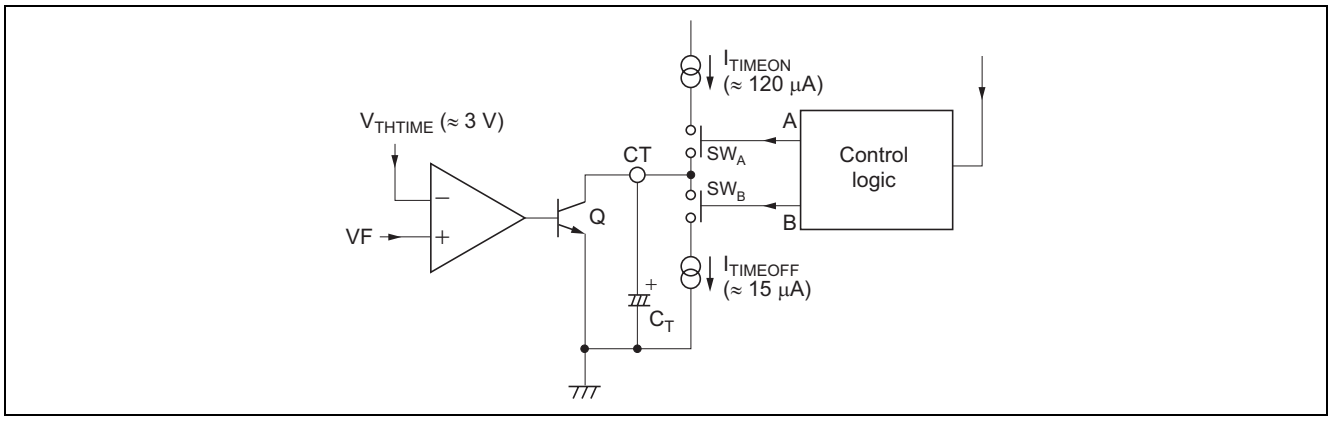


Figure 12 Block Diagram of Intermittent Action Circuit

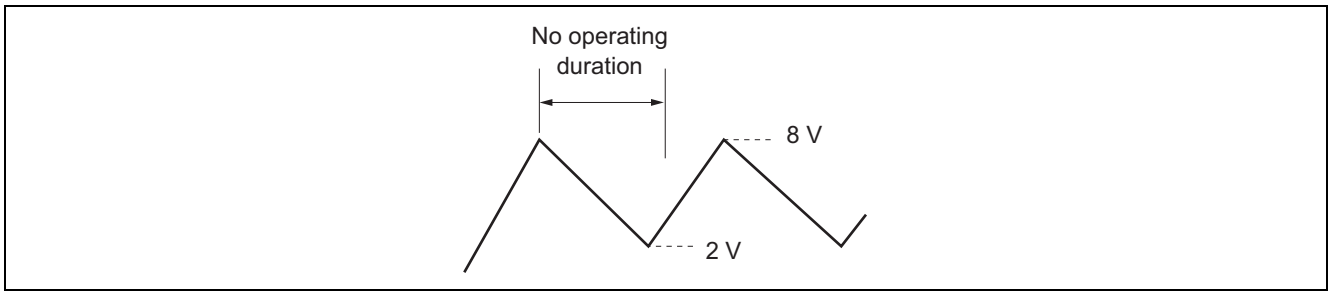


Figure 13 Waveform of CT Terminal

Figure 14 shows the I_{CC} versus V_{CC} in this timer-off duration.

In this duration the power is not supplied to IC from the third winding of transformer but through from the resistor R1 connected to V_{CC} line.

If the R1 shown in Application Example is selected adequate value, V_{CC} terminal voltage will be kept at not so high or low but adequate value, as the I_{CC} versus V_{CC} characteristics has such the one shown in figure 14.

To ground the CT terminal is recommended, when the intermittent mode is not used.

In this case the oscillated frequency will become low but the IC will neither stop the oscillation nor change to the intermittent action mode, when the current limit function becomes to operate and the VF terminal voltage becomes low.

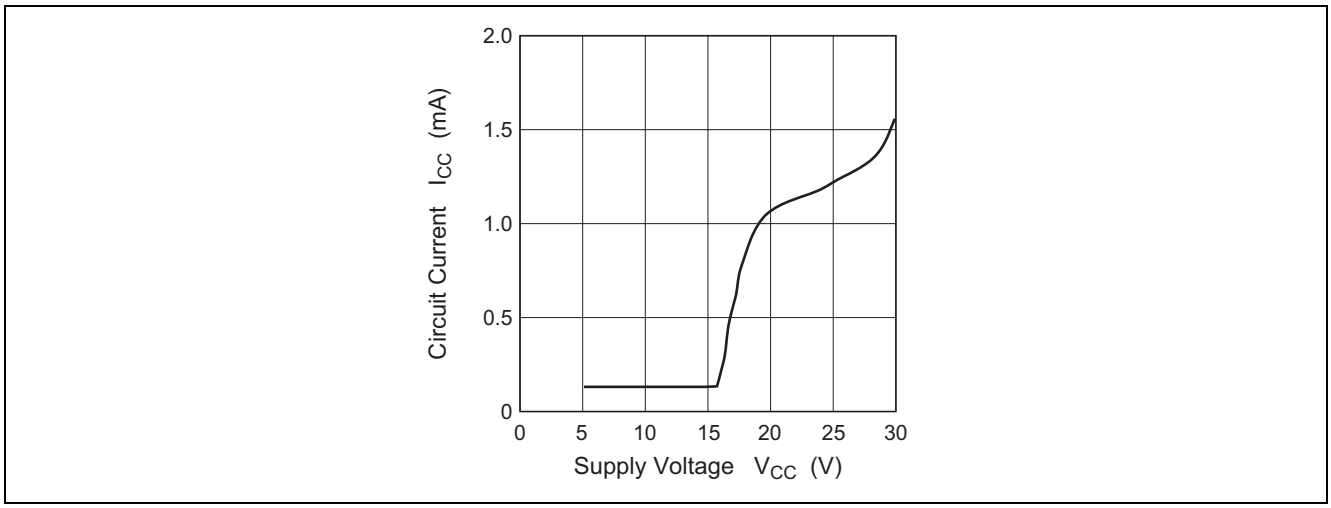


Figure 14 I_{CC} vs. V_{CC} in Timer-off Duration of Intermittent Action Circuit

Voltage Detector Circuit (DET) Section

The DET terminal can be used to control the output voltage which is determined by the winding ratio of fly back transformer in fly-back system or in case of common ground circuit of primary and secondary in feed forward system.

The circuit diagram is quite similar to that of shunt regulator type 431 as shown in figure 15. As well known from figure 15 and figure 16, the output of OP AMP has the current-sink ability, when the DET terminal voltage is higher than 2.5 V but it becomes high impedance state when lower than 2.5 V DET terminal and F/B terminal have inverting phase characteristics each other, so it is recommended to connect the resistor and capacitor in series between them for phase compensation. It is very important, one can not connect by resistor directly as there is the voltage difference between them and the capacitor has the DC stopper function.

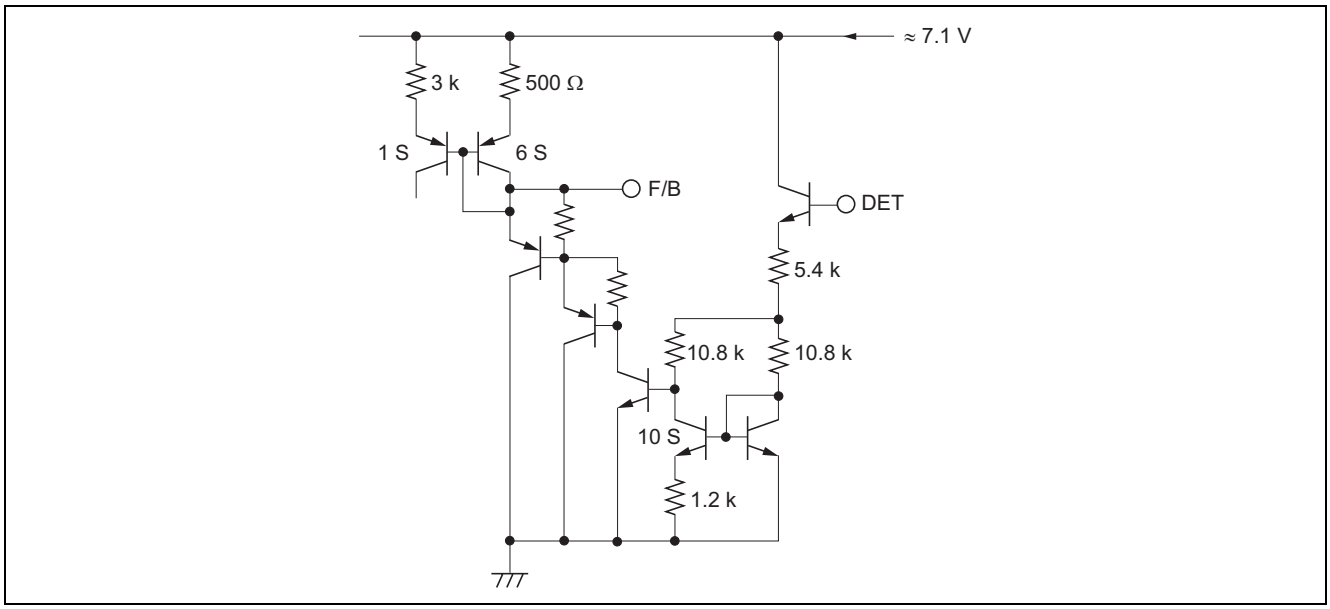


Figure 15 Equivalent Circuit Diagram of Voltage Detector

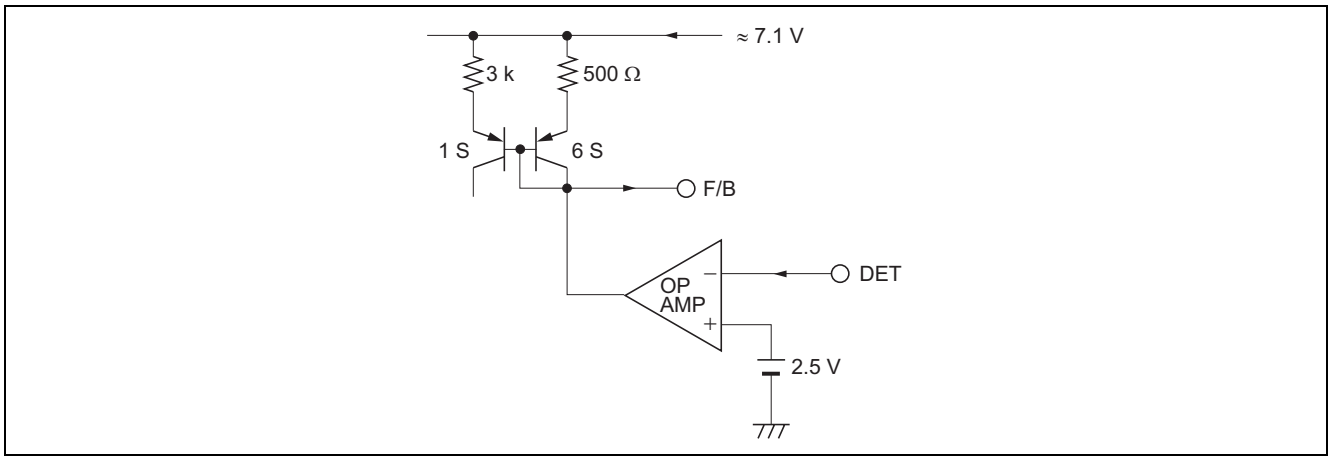


Figure 16 Equivalent Circuit Diagram of Voltage Detector

ON-OFF Circuit Section

Figure 17 shows the circuit diagram of ON-OFF circuit. The current flown into the ON-OFF terminal makes the Q4 "on" and the switching operation stop. On the other hand, the switching operation will recover as no current flown into ON/OFF terminal makes Q4 "off". As the constant current source connected to Q4 base terminal has such the hysteresis characteristics of 20 μA at operation and 3 μA at stopping. So the unstable operation is not appeared even if the ON/OFF terminal voltage signal varies slowly.

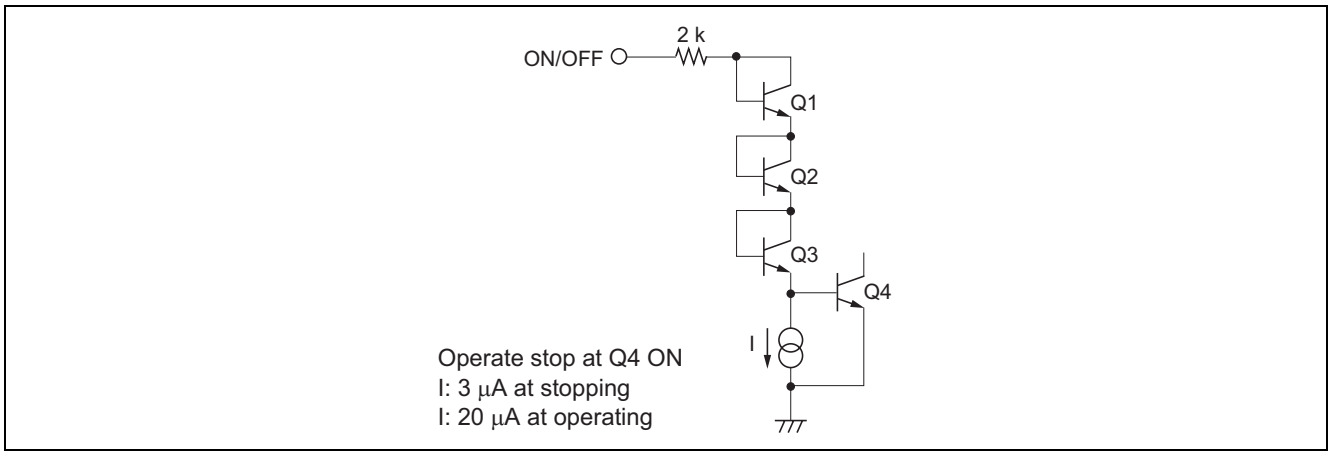


Figure 17 ON/OFF Circuit

Figure 18 shows how to connect the ON/OFF terminal. The switching operation will stop by switch-off and operate by switch-on.

Transistor or photo transistor can be replaced by this switch, of course. No resistor of 30 to 100 kΩ is connected and ON/OFF terminal is directly connected to GND, when it is not necessary to use the ON/OFF operation.

Figure 19 shows the I_{CC} versus V_{CC} characteristics in OFF state and V_{CC} will be kept at not so high or low but at the adequate voltage, when R1 shown in Application Example is selected properly.

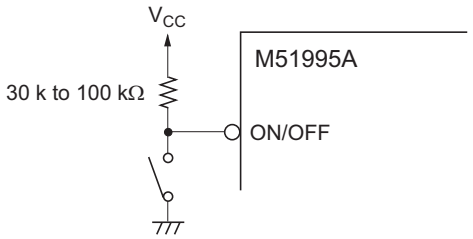


Figure 18 Connecting of ON/OFF Terminal

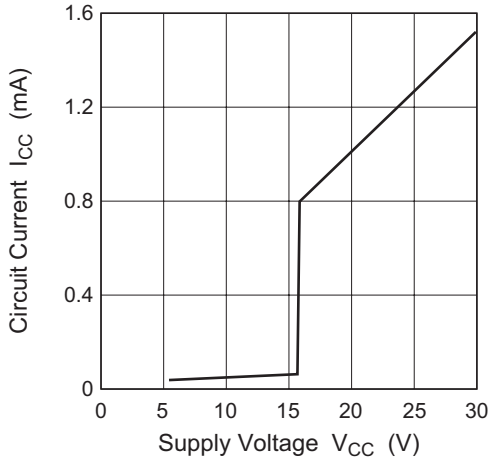


Figure 19 I_{CC} vs. V_{CC} in OFF State

OVP Circuit (Over Voltage Protection Circuit) Section

OVP circuit is basically positive feedback circuit constructed by Q2, Q3 as shown in figure 20.

Q2, Q3 turn on and the circuit operation of IC stops, when the input signal is applied to OVP terminal. (threshold voltage ≈ 750 mV)

The current value of I2 is about 150 μA when the OVP does not operates but it decreases to about 2 μA when OVP operates.

It is necessary to input the sufficient larger current (800 μA to 8 mA) than I2 for triggering the OVP operation.

The reason to decrease I2 is that it is necessary that I_{CC} at the OVP rest supply voltage is small.

It is necessary that OVP state holds by circuit current from R1 in the application example, so this IC has the characteristic of small I_{CC} at the OVP reset supply voltage (≈stand-by current +20 μA)

On the other hand, the circuit current is large in the higher supply voltage, so the supply voltage of this IC doesn't become so high by the voltage drop across R1.

This characteristic is shown in figure 21.

The OVP terminal input current in the voltage lower than the OVP threshold voltage is based on I2 and the input current in the voltage higher than the OVP threshold voltage is the sum of the current flowing to the base of Q3 and the current flowing from the collector of Q2 to the base.

For holding in the latch state, it is necessary that the OVP terminal voltage is kept in the voltage higher than V_{BE} of Q3.

So if the capacitor is connected between the OVP terminal and GND, even though Q2 turns on in a moment by the surge voltage, etc. this latch action does not hold if the OVP terminal voltage does not become higher than V_{BE} of Q3 by charging this capacitor.

For resetting OVP state, it is necessary to make the OVP terminal voltage lower than the OVP L threshold voltage or make V_{CC} lower than the OVP reset supply voltage.

As the OVP reset voltage is settled on the rather high voltage of 9.0 V, SMPS can be reset in rather short time from the switch-off of the AC power source if the smoothing capacitor is not so large value.

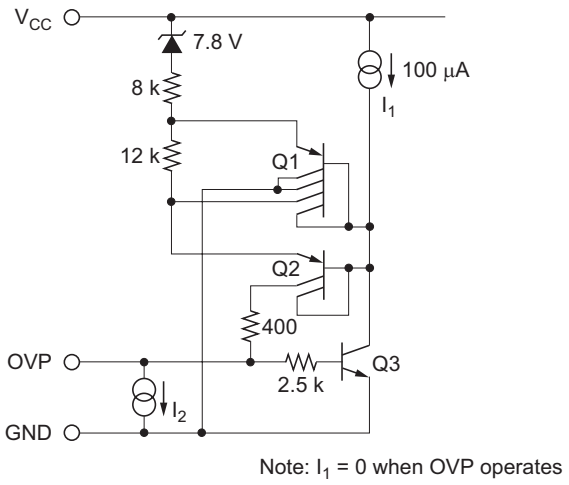


Figure 20 Detail Diagram of OVP Circuit

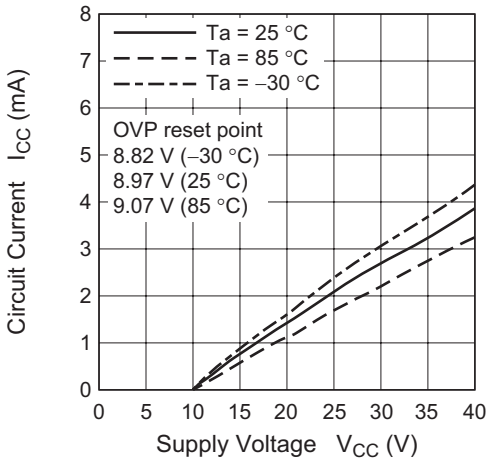


Figure 21 Circuit Current vs. Supply Voltage (OVP Operation)

Output Section

It is required that the output circuit has the high sink and source abilities for MOS FET drive. It is well known that the totempole circuit has high sink and source ability. However, it has the demerit of high through current.

For example, the through current may reach such the high current level of 1 A, if type M51995A has the “conventional” totempole circuit. For the high frequency application such as higher than 100 kHz, this through current is very important factor and will cause not only the large I_{CC} current and the inevitable heat-up of IC but also the noise voltage.

This IC uses the improved totempole circuit, so without deteriorating the characteristic of operating speed, its through current is approximately 100 mA.

Application Note of Type M51995AP/AFP

Design of Start-up Circuit and the Power Supply of IC

1. The start-up circuit when it is not necessary to set the start and stop input voltage

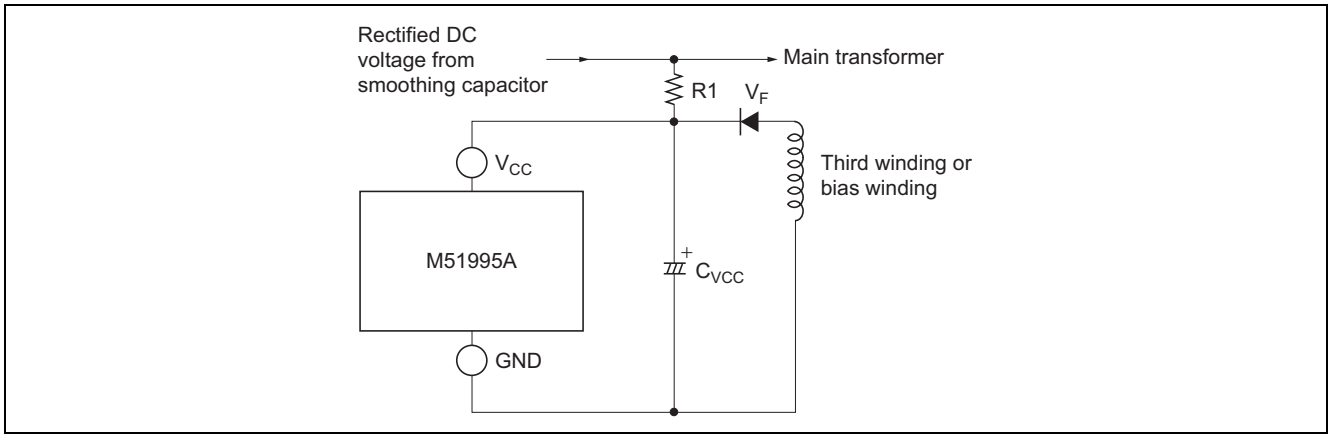


Figure 22 Start-up Circuit Diagram (when it is not necessary to set the start and stop input voltage)

Figure 22 shows one of the example circuit diagram of the start–up circuit which is used when it is not necessary to set the start and stop voltage.

It is recommended that the current more than 300 μA flows through R1 in order to overcome the operation start-up current $I_{CC(START)}$ and C_{VCC} is in the range of 10 to 47 μF. The product of R1 by C_{VCC} causes the time delay of operation, so the response time will be long if the product is too much large.

Just after the start-up, the I_{CC} current is supplied from C_{VCC}, however, under the steady state condition, IC will be supplied from the third winding or bias winding of transformer, the winding ratio of the third winding must be designed so that the induced voltage may be higher than the operation-stop voltage $V_{CC(STOP)}$.

The V_{CC} voltage is recommended to be 12 V to 17 V as the normal and optimum gate voltage is 10 to 15 V and the output voltage (V_{OH}) of type M51995AP/AFP is about (V_{CC} – 2 V).

It is not necessary that the induced voltage is settled higher than the operation start-up voltage $V_{CC(START)}$, and the high gate drive voltage causes high gate dissipation, on the other hand, too low gate drive voltage does not make the MOS FET fully on-state or the saturation state.

2. The start-up circuit when it is not necessary to set the start and stop input voltage

It is recommend to use the third winding of “forward winding” or “positive polarity” as shown in figure 23, when the DC source voltages at both the IC operation start and stop must be settled at the specified values.

The input voltage ($V_{IN(START)}$), at which the IC operation starts, is decided by R1 and R2 utilizing the low start-up current characteristics of type M51995AP/AFP.

The input voltage ($V_{IN(STOP)}$), at which the IC operation stops, is decided by the ratio of third winding of transformer.

The $V_{IN(START)}$ and $V_{IN(STOP)}$ are given by following equations.

$$V_{IN\ (START)} \approx R1 \times I_{CCL} + \left(\frac{R1}{R2} + 1\right) \times V_{CC\ (START)} \quad \cdots\cdots\cdots \quad (9)$$

$$V_{IN\ (STOP)} \approx (V_{CC\ (STOP)} - V_F) \times \frac{N_P}{N_B} + \frac{1}{2} V'_{IN\ RIP\ (P\text{-}P)} \quad \cdots\cdots \quad (10)$$

Where

I_{CCL} is the operation start-up current of IC
$V_{CC(START)}$ is the operation start-up voltage of IC
$V_{CC(STOP)}$ is the operation stop voltage of IC
V_F is the forward voltage of rectifier diode
$V'_{IN(P-P)}$ is the peak to peak ripple voltage of

$$V_{CC}\ \text{terminal} \approx \frac{N_B}{N_P} V'_{IN\ RIP\ (P\text{-}P)}$$

It is required that the $V_{IN(START)}$ must be higher than $V_{IN(STOP)}$.

When the third winding is the “fly back winding” or “reverse polarity”, the $V_{IN(START)}$ can be fixed, however, $V_{IN(STOP)}$ can not be settled by this system, so the auxiliary circuit is required.

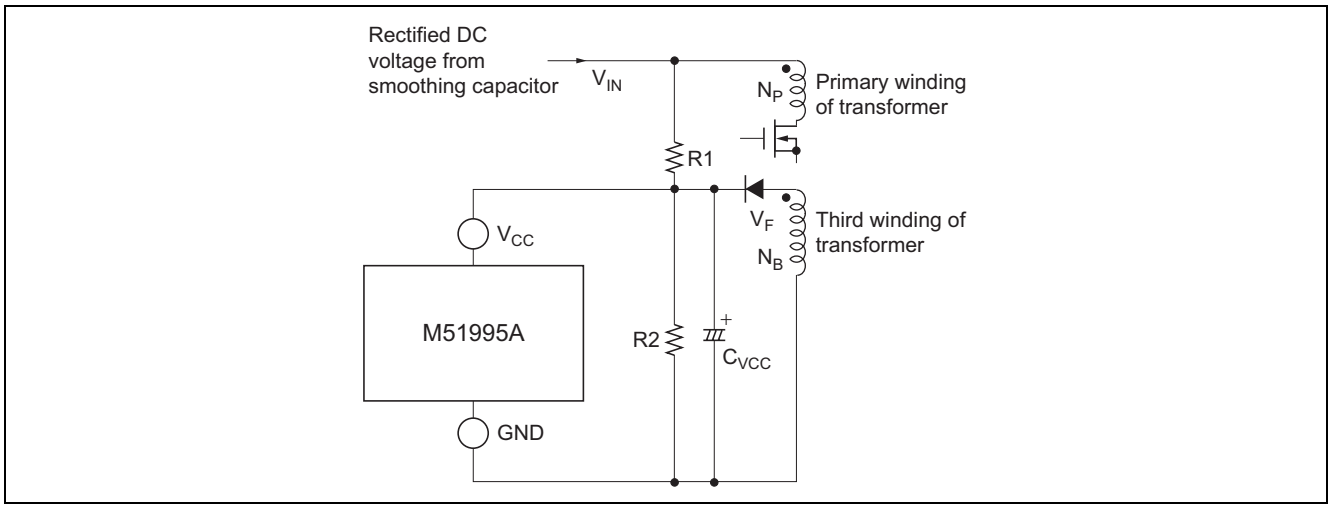


Figure 23 Start-up Circuit Diagram (when it is not necessary to set the start and stop input voltage)

3. Notice to the V_{CC}, V_{CC} line and GND line

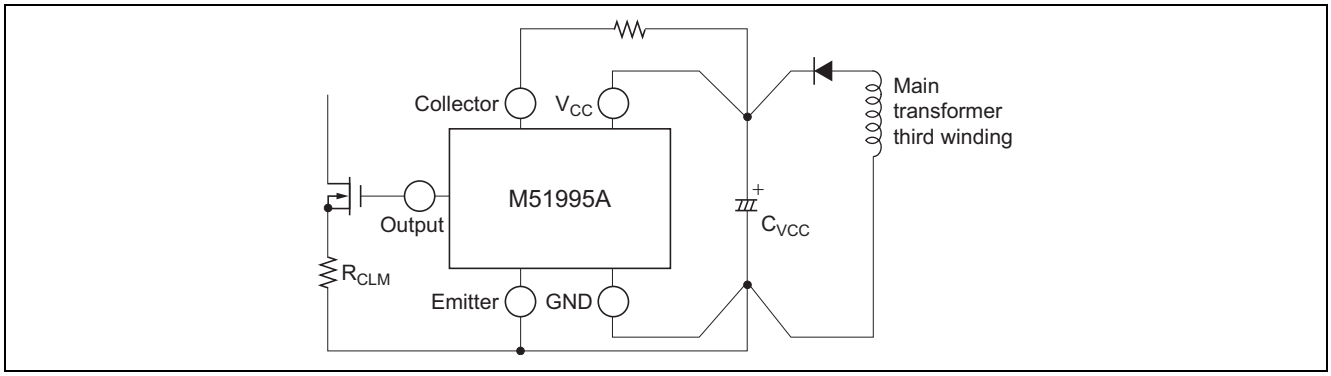


Figure 24 How to Design the Conductor-pattern of Type M51995A on PC Board (schematic example)

To avoid the abnormal IC operation, it is recommended to design the V_{CC} is not vary abruptly and has few spike voltage, which is induced from the stray capacity between the winding of main transformer.
To reduce the spike voltage, the C_{VCC}, which is connected between V_{CC} and ground, must have the good high frequency characteristics.
To design the conductor-pattern on PC board, following cautions must be considered as shown in figure 24.
(1) To separate the emitter line of type M51995A from the GND line of the IC
(2) The locate the C_{VCC} as near as possible to type M51995A and connect directly
(3) To separate the collector line of type M51995A from the V_{CC} line of the IC
(4) To connect the ground terminals of peripheral parts of IC_S to GND of type M51995A as short as possible

4. Power supply circuit for easy start-up

When IC starts to operate, the voltage of the C_{VCC} begins to decrease till the C_{VCC} becomes to be charged from the third winding of main-transformer as the I_{CC} of the IC increases abruptly. In case shown in figure 22 and 23, some "unstable start-up" or "fall to start-up" may happen, as the charging interval of C_{VCC} is very short duration; that is the charging does occur only the duration while the induced winding voltage is higher than the C_{VCC} voltage, if the induced winding voltage is nearly equal to the "operation-stop voltage" of type M51995.

It is recommended to use the 10 to 47 μF for $C_{VCC1,}$ and about 5 times capacity bigger than C_{VCC1} for C_{VCC2} in figure 25.

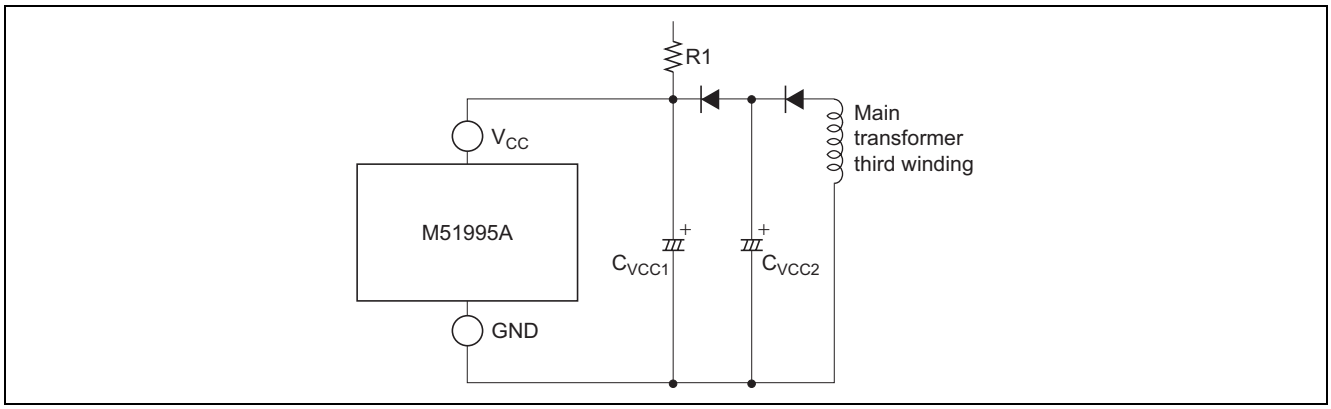


Figure 25 DC Source Circuit for Stable Start-up

OVP Circuit

(1) To avoid the miss operation of OVP

It is recommended to connect the capacitor between OVP terminal and GND for avoiding the miss operation by the spike noise.

The OVP terminal is connected with the sink current source (≈150 μA) in IC when OVP does not operate, for absorbing the leak current of the photo coupler in the application.

So the resistance between the OVP terminal and GND for leak-cut is not necessary.

If the resistance is connected, the supply current at the OVP reset supply voltage becomes large.

As the result, the OVP reset supply voltage may become higher than the operation stop voltage.

In that case, the OVP action is reset when the OVP is triggered at the supply voltage a little high than the operation stop voltage.

So it should be avoided absolutely to connect the resistance between the OVP terminal and GND.

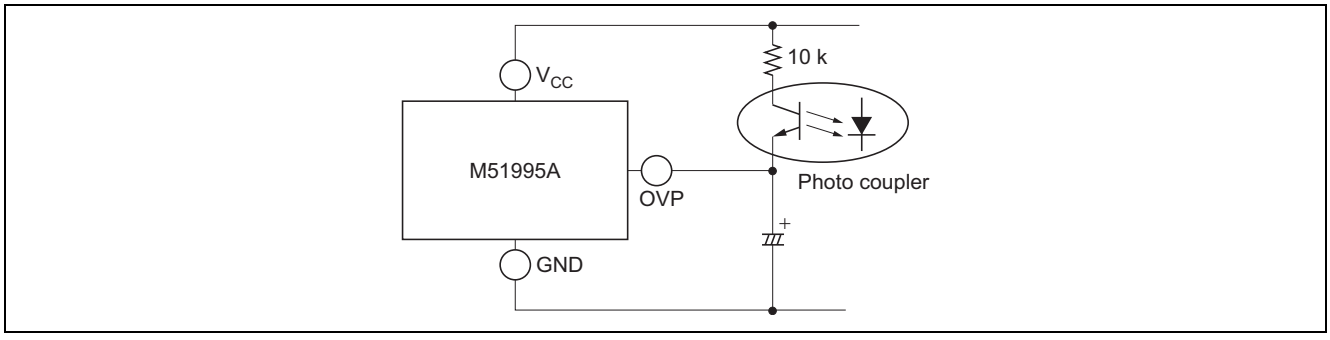


Figure 26 Peripheral Circuit of OVP Terminal

2. Application circuit to make the OVP-reset time fast
   The reset time may becomes problem when the discharge time constant of C_{FIN} • (R1 + R2) is long. Under such the circuit condition, it is recommended to discharge the C_{VCC} forcedly and to make the V_{CC} low value. This makes the OVP-reset time fast.

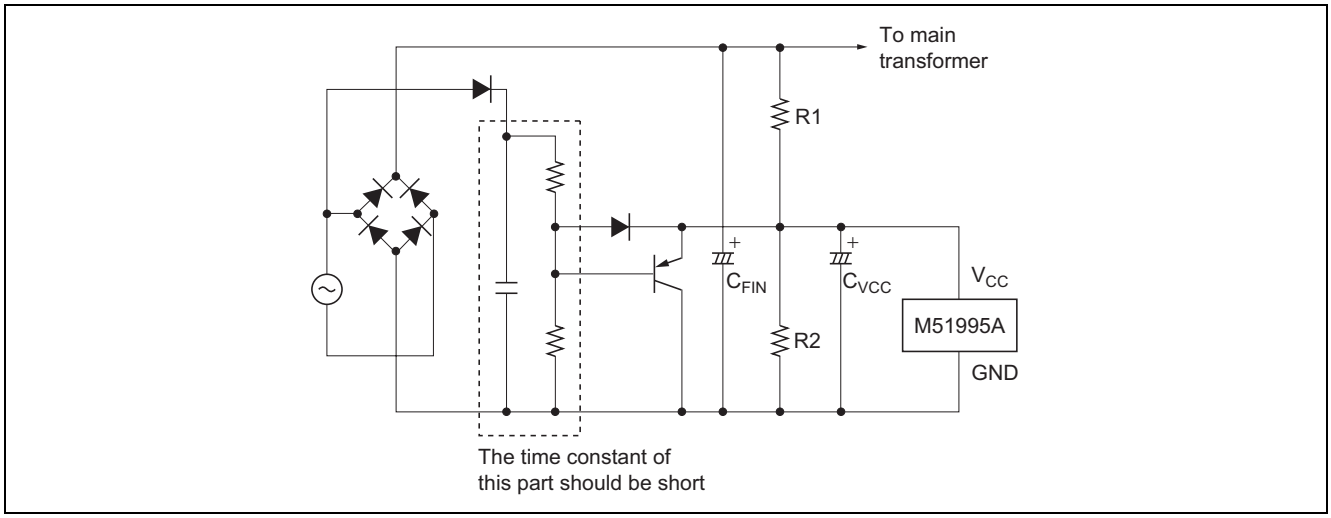


Figure 27 Example Circuit Diagram to Make the OVP-Reset-Time Fast

3. OVP setting method using the induced third winding voltage on fly back system
   For the over voltage protection (OVP), the induced fly back type third winding voltage can be utilized, as the induced third winding voltage depends on the output voltage. Figure 28 shows one of the example circuit diagram.

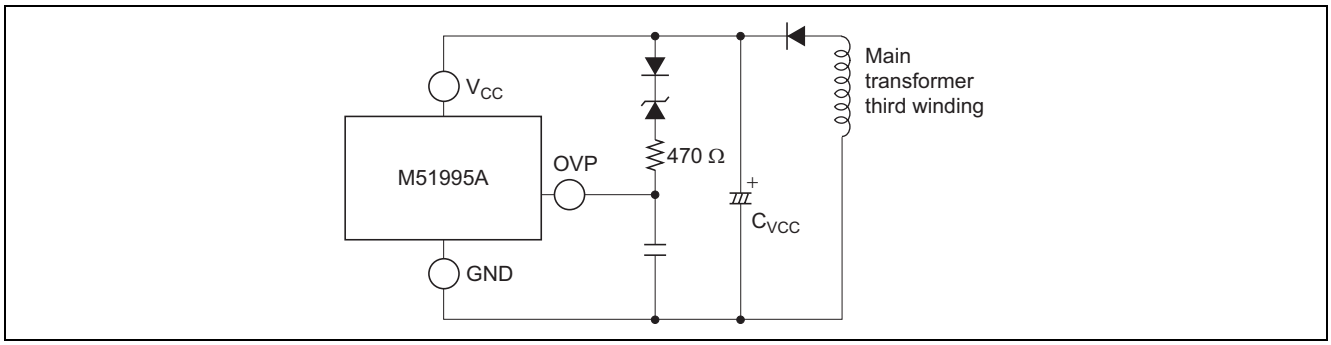


Figure 28 OVP Setting Method Using the Induced Third Winding Voltage on Fly Back System

Current Limiting Circuit

1. Peripheral circuit of CLM+, CLM– terminal

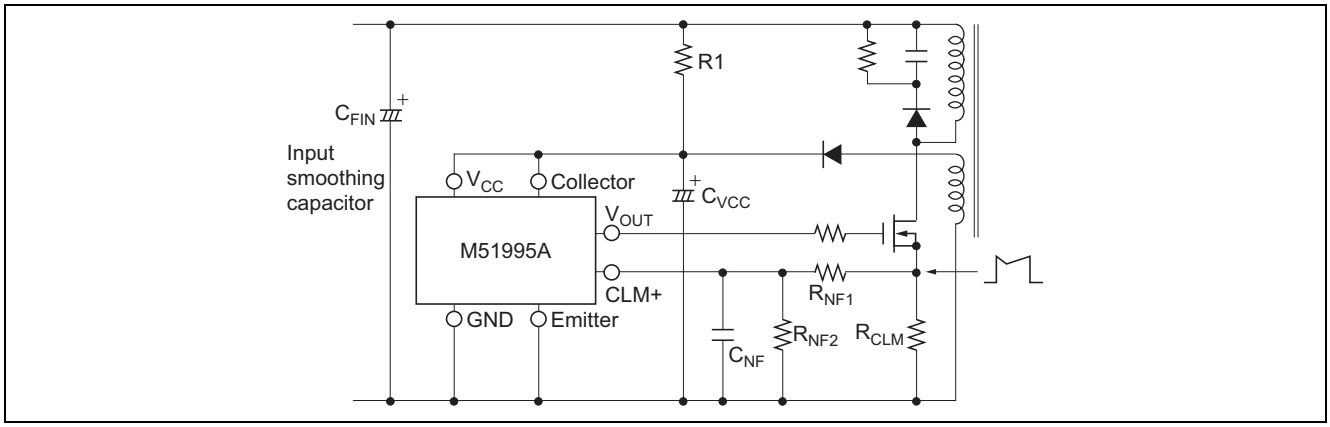


Figure 29 Peripheral Circuit Diagram of CLM+ Terminal

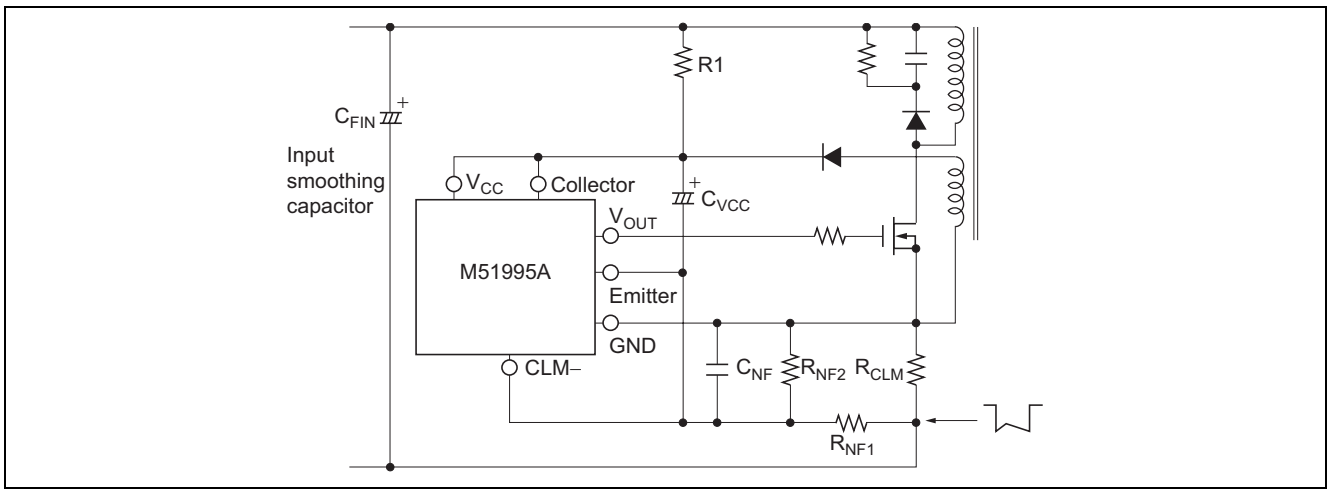


Figure 30 Peripheral Circuit Diagram of CLM– Terminal

Figure 29 and 30 show the example circuit diagrams around the CLM+ and CLM– terminal. It is required to connect the low pass filter, as the main current or drain current contains the spike current especially during the turn-on duration of MOS FET.

1,000 pF to 22,000 pF is recommended for C_{NF} and the R_{NF1} and R_{NF2} have the functions both to adjust the "current-detecting-sensitivity" and to consist the low pass filter.

To design the R_{NF1} and R_{NF2}, it is required to consider the influence of CLM terminal source current (I_{INCLM+} or I_{NFCLM-}), which value is in the range of 90 to 270 μA.

In order to be not influenced from these resistor paralleled value of R_{NF1} and R_{NF2}, (R_{NF1}/R_{NF2}) is recommended to be less than 100 Ω.

The R_{CLM} should be the non-inductive resistor.

2. Over current limiting curve
   (1) In case of feed forward system

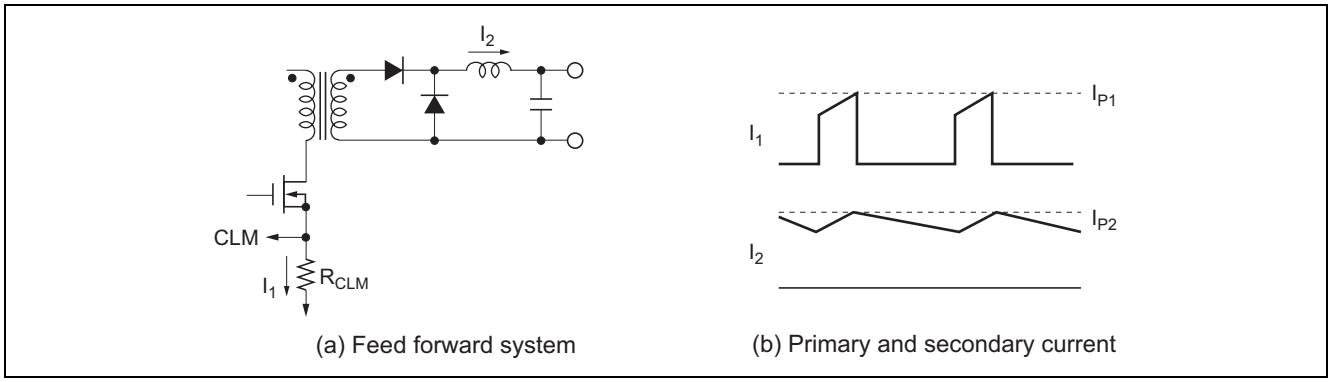


Figure 31 Primary and Secondary Current Waveforms Under the Current Limiting Operation Condition on Feed Forward System

Figure 31 shows the primary and secondary current wave-forms under the current limiting operation.
At the typical application of pulse-by-pulse primary current detecting circuit, the secondary current depends on the primary current. As the peak value of secondary current is limited to specified value, the characteristics curve of output voltage versus output current become to the one as shown in figure 32.
The demerit of the pulse by pulse current limiting system is that the output pulse width can not reduce to less than some value because of the delay time of low pass filter connected to the CLM terminal and propagation delay time T_{PDCLM} from CLM terminal to output terminal of type M51995A. The typical T_{PDCLM} is 100 ns.
As the frequency becomes higher, the delay time must be shorter. And as the secondary output voltage becomes higher, the dynamic range of on-duty must be wider; it means that it is required to make the on-duration much more narrower.
So this system has the demerit at the higher oscillating frequency and higher output voltage applications.

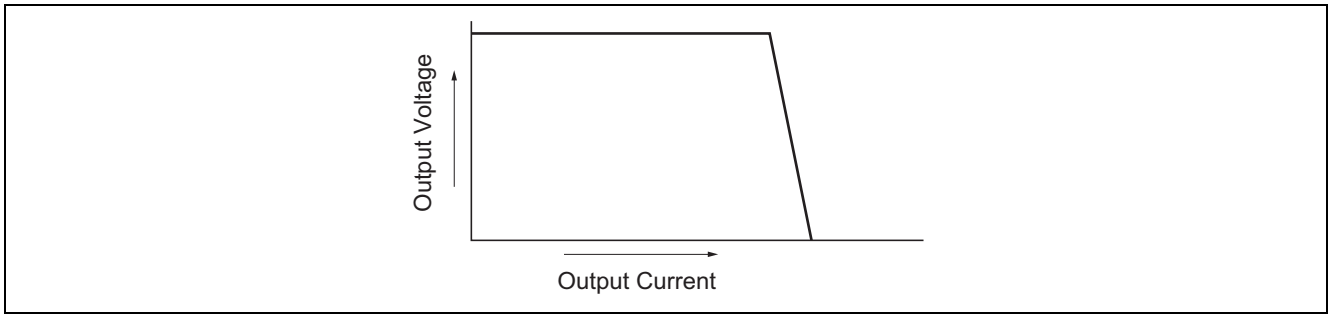


Figure 32 Over Current Limiting Curve on Feed Forward System

To improve these points, the oscillating frequency is set low using the characteristics of VF terminal.
When the current limiting circuit operates under the over current condition, the oscillating frequency decreases in accordance with the decrease of VF terminal voltage, if the VF is lower than 3.5V.And also the dead time becomes longer.
Under the condition of current limiting operation, the output current I2 continues as shown in figure 31. So the output voltage depends on the product of the input primary voltage V_{IN} and the on-duty.
If the third winding polarity is positive, the V_{CC} depends on V_{IN}, so it is concluded that the smoothed voltage of V_{OUT} terminal depends on the output DC voltage of the SMPS.
So the sharp current limiting characteristics will be got, if the V_{OUT} voltage if feed back to VF terminal through low pass filter as shown in figure 33.
It is recommended to use 15 kΩ for R_{VFFB}, and 10,000 pF for C_{VFFB} in figure 33.

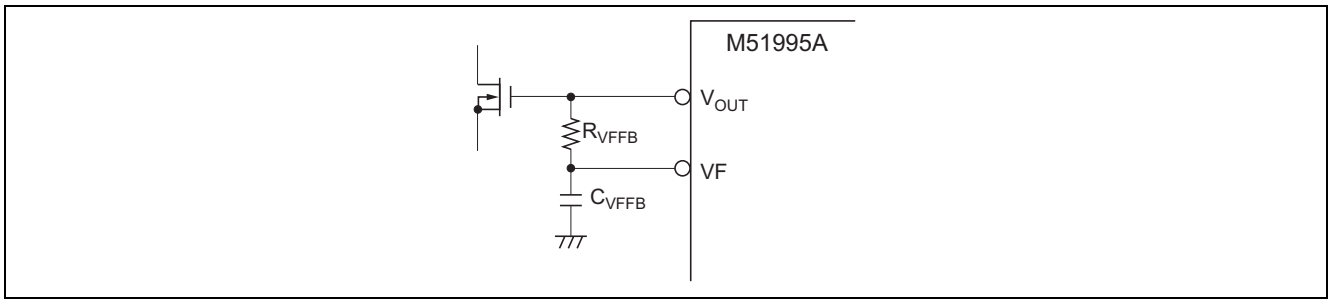


Figure 33 Feed Back Loop through Low Pass Filter from V_{OUT} to V_F Terminal

Figure 34 shows how to control the knee point where the frequency becomes decrease,

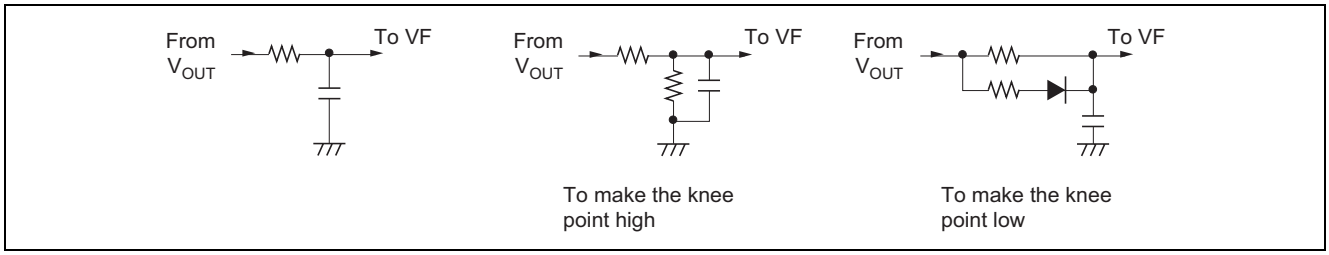


Figure 34 How to Control the Knee Point

(2) In case of fly back system

The DC output voltage of SMPS depends on the V_{CC} Voltage of type M51995A when the polarity of the third winding is negative and the system is fly back. So the operation of type M51995A will stop when the V_{CC} becomes lower than “Operation-stop voltage” of M51995A when the DC output voltage of SMPS decreases under specified value at over load condition.

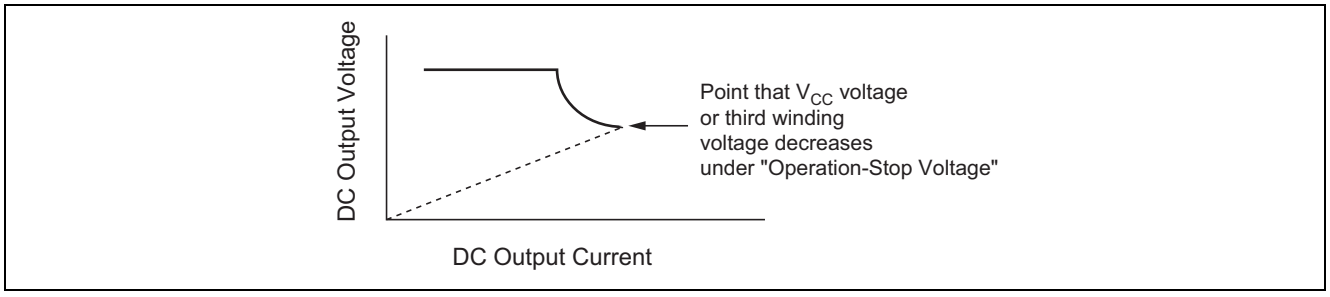


Figure 35 Over Current Limiting Curve on Fly Back System

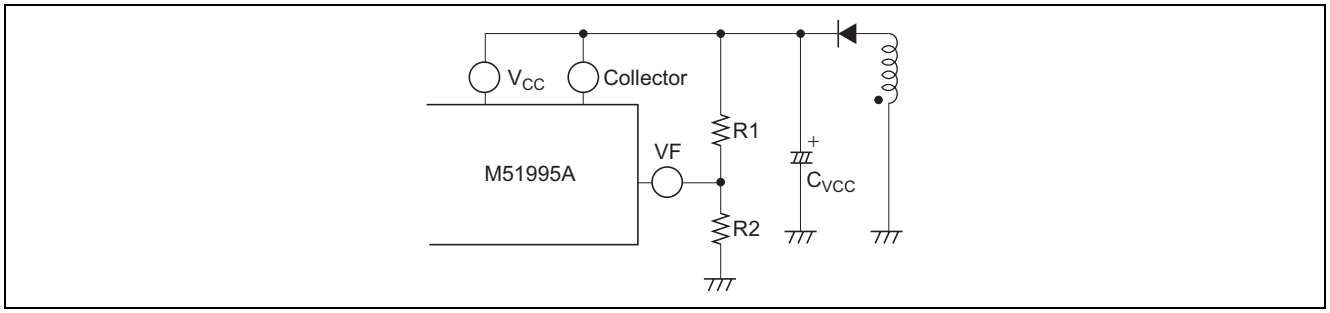


Figure 36 Circuit Diagram to make Knee Point Low on Fly Back System

However, the M51995A will non-operate and operate intermittently, as the V_{CC} voltage rises in accordance with the decrease of I_{CC} current.

The fly back system has the constant output power characteristics as shown in figure 35 when the peak primary current and the operating frequency are constant.

To control the increase of DC output current, the operating frequency is decreased using the characteristics of VF terminal when the over current limiting function begins to operate.

The voltage which mode by dividing the V_{CC} is applied to VF terminal as shown in figure 36, as the induced third winding voltage depends on the DC output voltage of SMPS.

15 kΩ or less is recommended for R_2 in figure 36, it is noticed that the current flows through R_1 and R_2 will superpose on the $I_{CC(START)}$ current.

If the R_1 is connected to C_{VCC2} in figure 25, the current flows through R_1 and R_2 is independent of the $I_{CC(START)}$.

(3) Application circuit to keep the non-operating condition when over load current condition will continue for specified duration

The CT terminal voltage will begin to rise and the capacitor connected to CT terminal will be charged-up, if the current limiting function starts, and VF terminal voltage decreases below V_{THTIME} (~ 3 V).

If the charged-up CT terminal voltage is applied to OVP terminal through the level-shifter consisted of buffer transistor and resistor, it makes type M51995A keep non-operating condition.

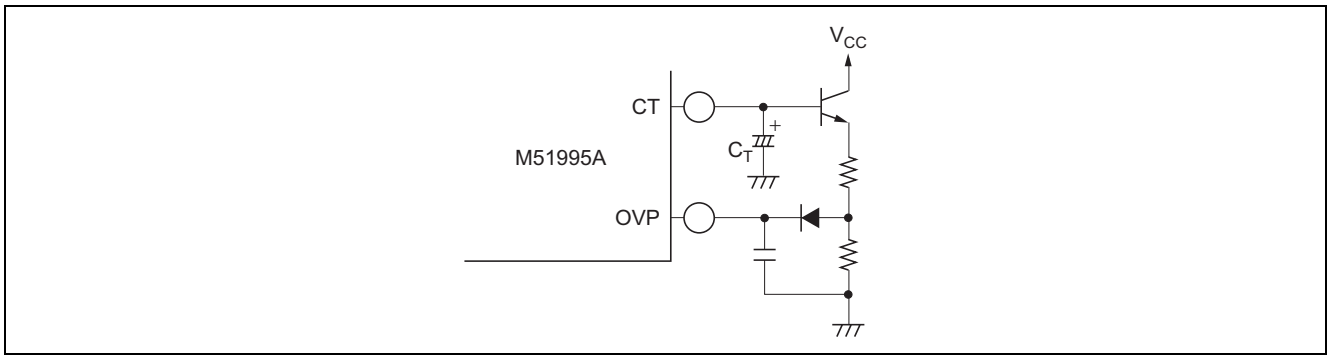


Figure 37 Application Circuit Diagram to Keep the Non-Operating Condition when Over Load Current Condition will Continue for Specified Duration

Output Circuit

1. The output terminal characteristics at the V_{CC} voltage lower than the “Operation-stop” voltage

   The output terminal has the current sink ability even though the V_{CC} voltage lower than the “Operation-stop” voltage or $V_{CC(STOP)}$ (It means that the terminal is “Output low state” and please refer characteristics of output low voltage versus sink current.)

   This characteristics has the merit not to damage the MOS FET at the stop of operation when the V_{CC} voltage decreases lower than the voltage of $V_{CC\,(STOP)}$, as the gate charge of MOS FET, which shows the capacitive load characteristics to the output terminal, is drawn out rapidly.

   The output terminal has the draw-out ability above the V_{CC} voltage of 2 V, however, lower than the 2 V, it loses the ability and the output terminal potential may rise due to the leakage current.

   In this case, it is recommended to connect the resistor of 100 kΩ between gate and source of MOS FET as shown in figure 38.

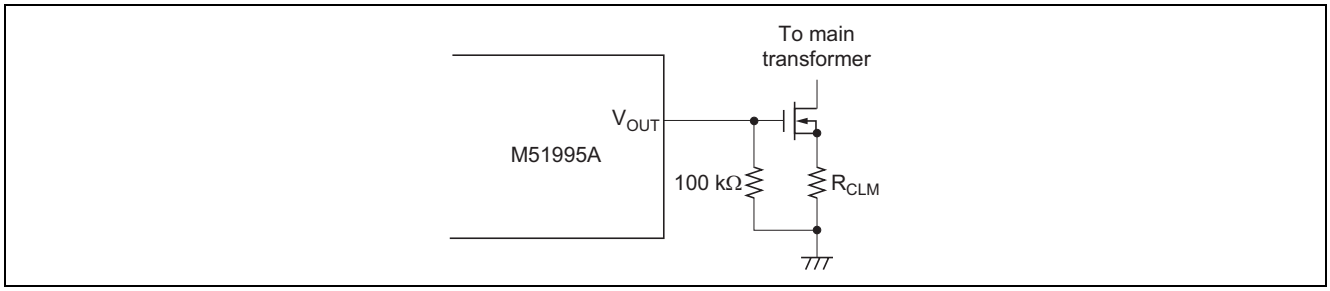


Figure 38 Circuit Diagram to Prevent the MOS FET Gate Potential Rising

2. MOS FET gate drive power dissipation
   Figure 39 shows the relation between the applied gate voltage and the stored gate charge.
   In the region 1, the charge is mainly stored at C_{GS} as the depletion is spread and C_{GD} is small owing to the off-state of MOS FET and the high drain voltage.
   In the region 2, the C_{GD} is multiplied by the "mirror effect" as the characteristics of MOS FET transfers from off-state to on-state.
   In the region 3, both the C_{GD} and C_{GS} affect to the characteristics as the MOS FET is on-state and the drain voltage is low.

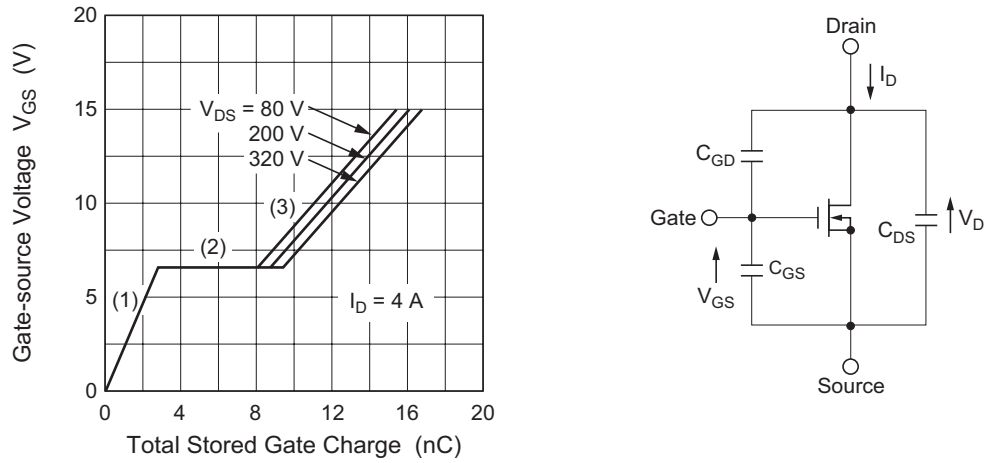


Figure 39 The Relation between Applied Gate-Source Voltage and Stored Gate Charge

The charging and discharging current caused by this gate charge makes the gate power dissipation. The relation between gate drive current I_D and total gate charge Q_{GSH} is shown by following equation;

$$I_D = Q_{GSH} \bullet f_{OSC} \quad \cdots\cdots (11)$$

Where

f_{osc} is switching frequency

As the gate drive current may reach up to several tenths milliamperes at 500 kHz operation, depending on the size of MOS FET, the power dissipation caused by the gate current can not be neglected.
In this case, following action will be considered to avoid heat up of type M51995A.
(1) To attach the heat sink to type M51995A
(2) To use the printed circuit board with the good thermal conductivity
(3) To use the buffer circuit shown next section

3. Output buffer circuit
   It is recommended to use the output buffer circuit as shown in figure 40, when type M51995A drives the large capacitive load or bipolar transistor.

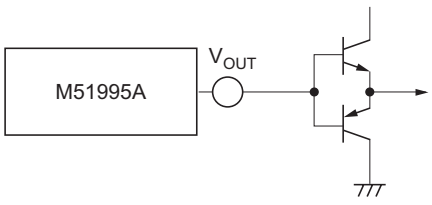


Figure 40 Output Buffer Circuit Diagram

DET Circuit

Figure 41 shows how to use the DET circuit for the voltage detector and error amplifier.

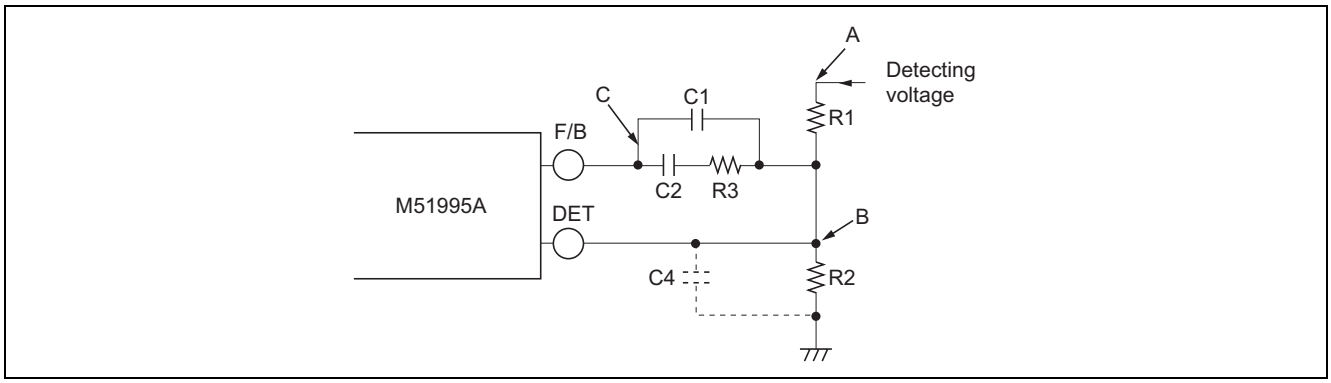


Figure 41 How to use the DET Circuit for the Voltage Detector

For the phase shift compensation, it is recommended to connected the CR network between DET terminal and F/B terminal.

Figure 42 shows the gain-frequency characteristics between point B and point C shown in figure 41.

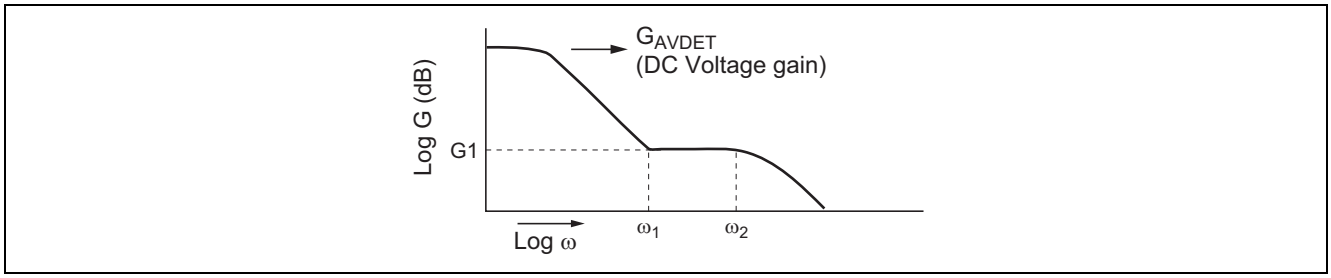


Figure 42 Gain-Frequency Characteristics between Point B and C shown in Figure 41

The G1, ω_1 and ω_2 are given by following equations;

$$G1 = \frac{R3}{R1 / R2} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (12)$$

$$\omega_1 = \frac{1}{C2 \bullet R3} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (13)$$

$$\omega_2 = \frac{C1 + C2}{C1 \bullet C2 \bullet R3} \quad \cdots\cdots\cdots\cdots\cdots\cdots \quad (14)$$

At the start of the operation, there happen to be no output pulse due to F/B terminal current through C1 and C2, as the potential of F/B terminal rises sharply just after the start of the operation.

Not to lack the output pulse, is recommended to connect the capacitor C4 as shown by broken line.

Please take notice that the current flows through the R1 and R2 are superposed to $I_{CC(START)}$. Not to superpose, R1 is connected to C_{VCC2} as shown in figure 25.

How to Get the Narrow Pulse Width During the Start of Operation

Figure 43 shows how to get the narrow pulse width during the start of the operation. If the pulse train of forcedly narrowed pulse-width continues too long, the misstart of operation may happen, so it is recommended to make the output pulse width narrow only for a few pulse at the start of operation. 0.1μF is recommended for the C.

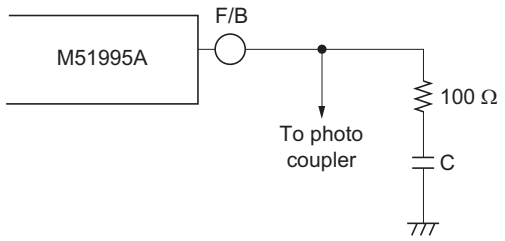


Figure 43 How to Get the Narrow Pulse Width During the Start of Operation

How to Synchronize with External Circuit

Type M51995A has no function to synchronize with external circuit, however, there is some application circuit for synchronization as shown in figure 44. If this circuit is used, the synchronization may be out of order at the overload condition when the current limiting function starts to operate and VF terminal voltage becomes lower than 3 V.

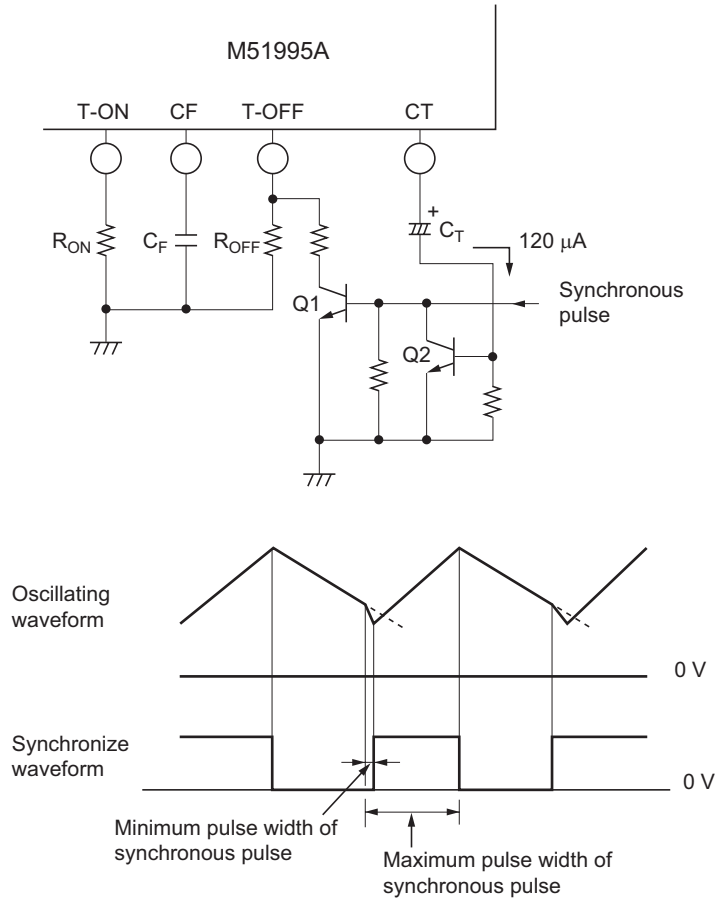


Figure 44 How to Synchronize with External Circuit

Driver Circuit for Bipolar Transistor

When the bipolar transistor is used instead of MOS FET, the base current of bipolar transistor must be sinked by the negative base voltage source for the switching-off duration, in order to make the switching speed of bipolar transistor fast one.

In this case, over current can not be detected by detecting resistor in series to bipolar transistor, so it is recommended to use the CT (current transformer).

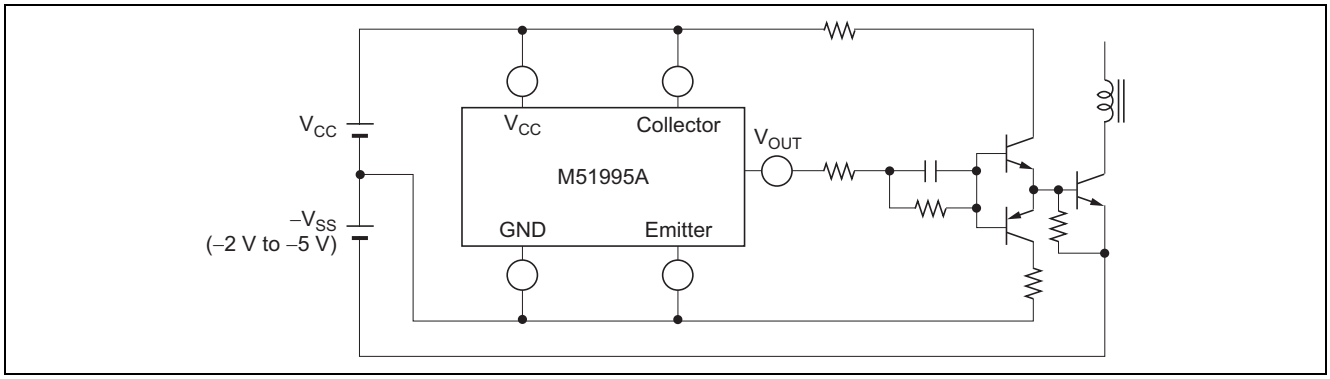


Figure 45 Driver Circuit Diagram (1) for Bipolar Transistor

For the low current rating transistor, type M51995A can drive it directly as shown in figure 46.

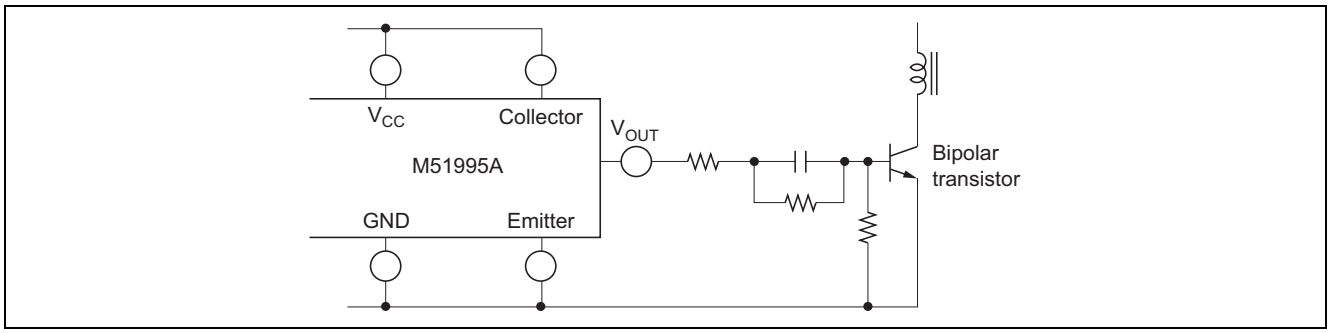


Figure 46 Driver Circuit Diagram (2) for Bipolar Transistor

Attention for Heat Generation

The maximum ambient temperature of type M51995A is +85°C, however, the ambient temperature in vicinity of the IC is not uniform and varies place by place, as the amount of power dissipation is fearfully large and the power dissipation is generated locally in the switching regulator.

So it is one of the good idea to check the IC package temperature.

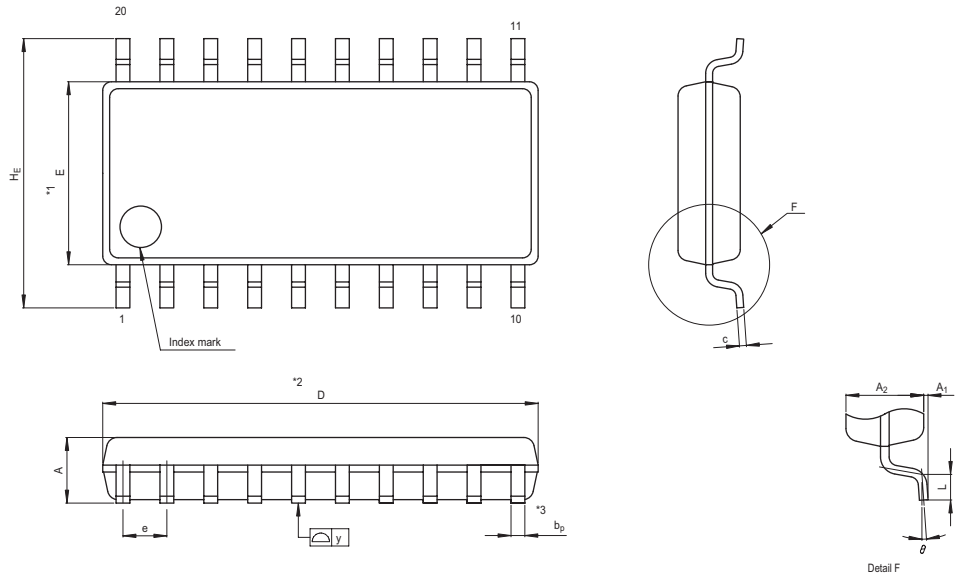
The temperature difference between IC junction and the surface of IC package is 15°C or less, when the IC junction temperature is measured by temperature dependency of forward voltage of pin junction, and IC package temperature is measured by “thermo-viewer”, and also the IC is mounted on the “phenol-base” PC board in normal atmosphere.

So it is concluded that the maximum case temperature (surface temperature of IC) rating is 120°C with adequate margin.

As type M51995 has the modified totempole driver circuit, the transient through current is very small and the total power dissipation is decreased to the reasonable power level.

Package Dimensions

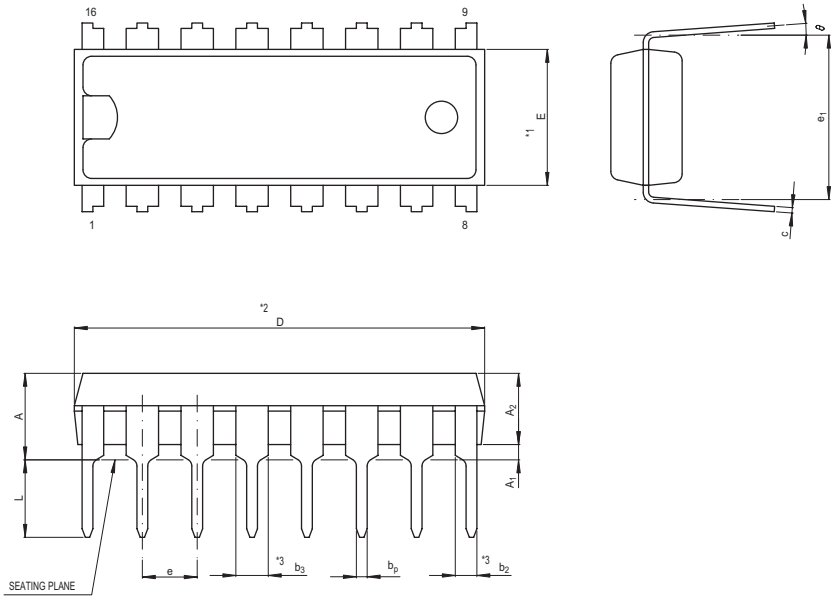
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.3x12.6-1.27	PRSP0020DA-A	20P2N-A	0.3g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	12.5	12.6	12.7
E	5.2	5.3	5.4
A_2	—	1.8	—
A_1	0	0.1	0.2
A	—	—	2.1
b_p	0.35	0.4	0.5
c	0.18	0.2	0.25
θ	0°	—	8°
H_E	7.5	7.8	8.1
e	1.12	1.27	1.42
y	—	—	0.1
L	0.4	0.6	0.8

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19-2.54	PRDP0016AA-A	16P4	1.0g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	18.8	19.0	19.2
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.4	0.5	0.6
b_2	0.9	1.0	1.3
b_3	1.4	1.5	1.8
c	0.22	0.27	0.34
θ	0°	—	15°
e	2.29	2.54	2.79
L	3.0	—	—

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