普誠科技股份有限公司
Princeton Technology Corp.
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# DESCRIPTION

PT2315A is a two-channel digital audio processor utilizing CMOS Technology. Volume, Bass, Treble and Balance Controls are incorporated into a single chip. Loudness Function is also provided to build a highly effective electronic audio processor having the highest performance and reliability with the least external components. All functions are programmable using the $I^2C$ Bus. The pin assignments and application circuit are optimized for easy PCB layout and cost saving advantage for audio application. Housed in a 20-pin DIP and SOP, PT2315A is pin-to-pin compatible with TDA7315 and is very similar in performance with the later.



# FEATURES

- CMOS Technology
- Least External Components
- Treble and Bass Control
- Loudness Function
- Input/Output for External Noise Reduction System/Equalizer
- 2 Independent Speaker Controls for Balance Function
- Independent Mute Function
- Volume Control in 1.25dB/step
- Low Distortion
- Low Noise and DC Stepping
- Controlled by $I^2C$ Bus Micro-Processor Interface
- Pin-to-pin Compatible with TDA7315

# APPLICATIONS

- Car Stereo (Audio)
- Hi-Fi Audio System
- Can be used in all I2C System Applications

Note:
Purchase of $I^2C$ Component of Princeton Technology Corporation (PTC) conveys a license under Philips $I^2C$ Patent Right to use these components in any $I^2C$ System, provided that the system conforms to the $I^2C$ Standard Specification defined by Philips

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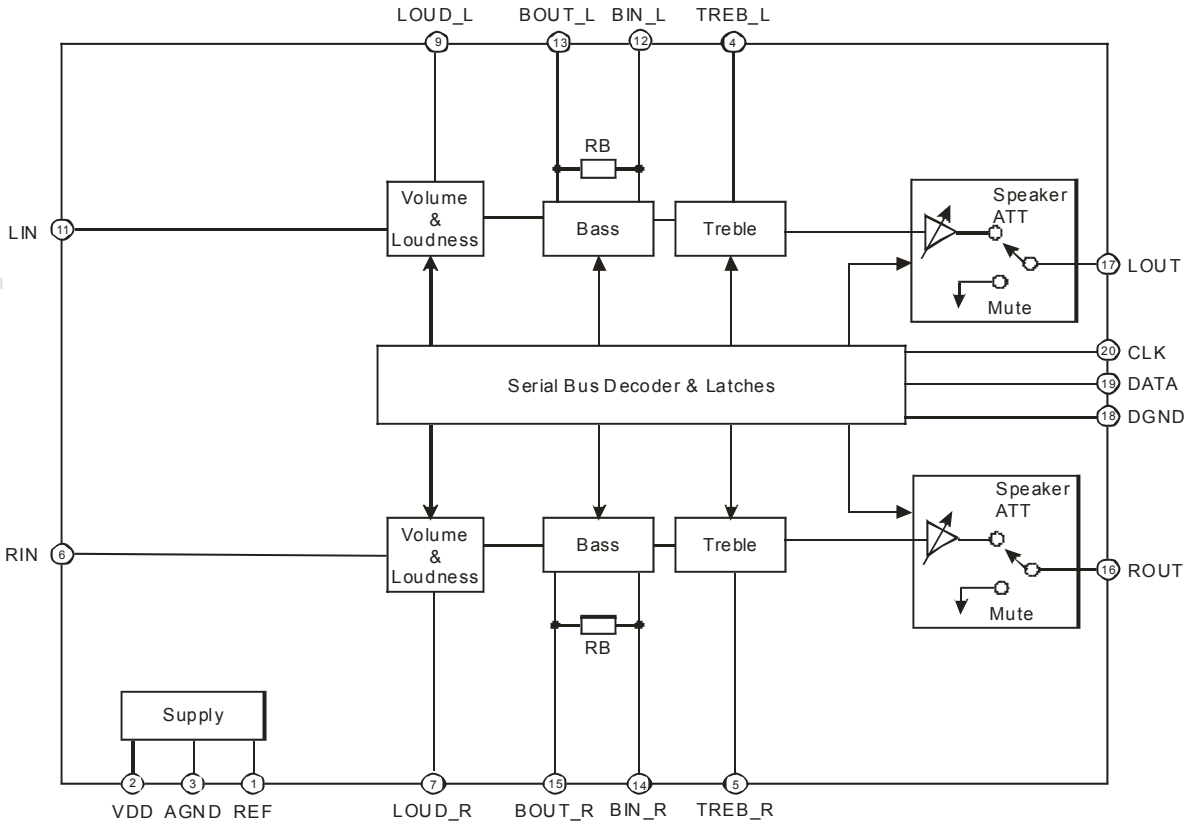
# BLOCK DIAGRAM



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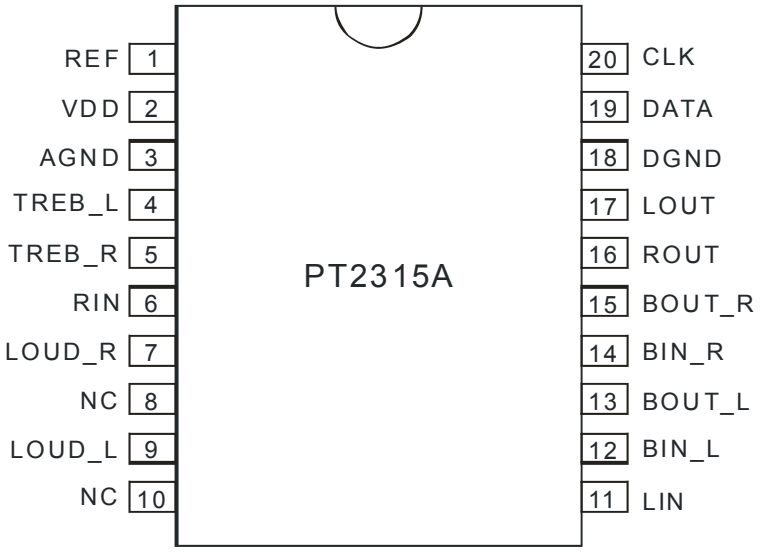
# PIN CONFIGURATION






# PIN DESCRIPTION

| Pin Name | I/O | Description | Pin No. |
|---|---|---|---|
| REF | - | Analog Reference Voltage (1/2 VDD) | 1 |
| VDD | - | Supply Input Voltage | 2 |
| AGND | - | Analog Ground | 3 |
| TREB_L | I | Left Channel Input for Treble Controller | 4 |
| TREB_R | I | Right Channel Input for Treble Controller | 5 |
| RIN | I | Audio Processor Right Channel Input | 6 |
| LOUD_R | I | Right Channel Loudness Input | 7 |
| NC | - | No Connection | 8, 10 |
| LOUD_L | I | Left Channel Loudness Input | 9 |
| LIN | I | Audio Processor Left Channel Input | 11 |
| BIN_L | I | Left Bass Controller Input Channel | 12 |
| BOUT_L | O | Left Bass Controller Output Channel | 13 |
| BIN_R | I | Right Channel Input for Bass Controller | 14 |
| BOUT_R | O | Right Channel Output for Bass Controller | 15 |
| ROUT | O | Right Speaker Output | 16 |
| LOUT | O | Left Speaker Output | 17 |
| DGND | - | Digital Ground | 18 |
| DATA | I | Control Data Input | 19 |
| CLK | I | Clock Input for Serial Data Transmission | 20 |

# FUNCTION DESCRIPTION

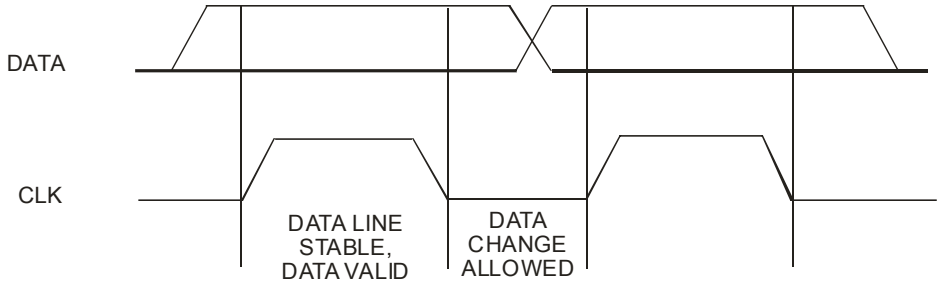
## *I²C BUS INTERFACE*

Data are transmitted to and from the microprocessor to the PT2315A via the DATA and CLK. The DATA and CLK make up the BUS Interface.

## *DATA VALIDITY*



A data on the DATA Line is considered valid and stable only when the CLK Signal is in HIGH State. The HIGH and LOW State of the DATA Line can only change when the CLK signal is LOW. Please refer to the figure below.

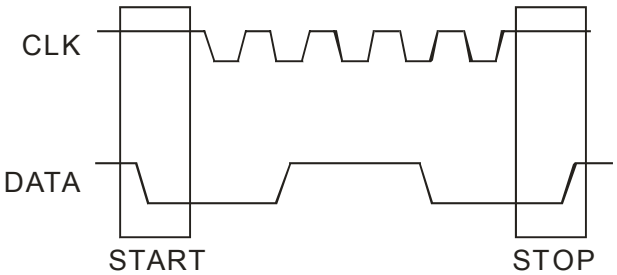



## *START AND STOP CONDITIONS*

A Start Condition is activated when
1) CLK is set to HIGH and
2) DATA shifts from HIGH to LOW State.

The Stop Condition is activated when
1) CLK is set to HIGH and
2) DATA shifts from LOW to HIGH State.

Please refer to the timing diagram below.



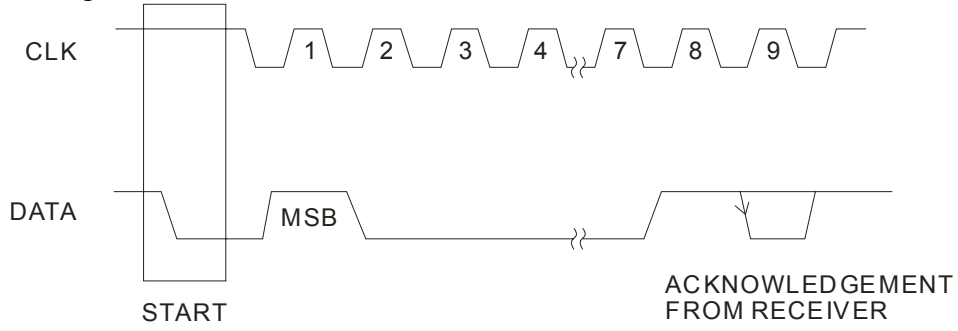
## BYTE FORMAT

Every byte transmitted to the DATA Line consist of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

## ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master (μP) puts a resistive HIGH level on the DATA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the DATA line during the Acknowledge Clock Pulse so that the DATA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.






The audio processor that has been addressed has to generate an acknowledge after receiving each byte, otherwise, the DATA Line will remain at the High Level during the ninth ($9^{th}$) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

## TRANSMISSION WITHOUT ACKNOWLEDGE

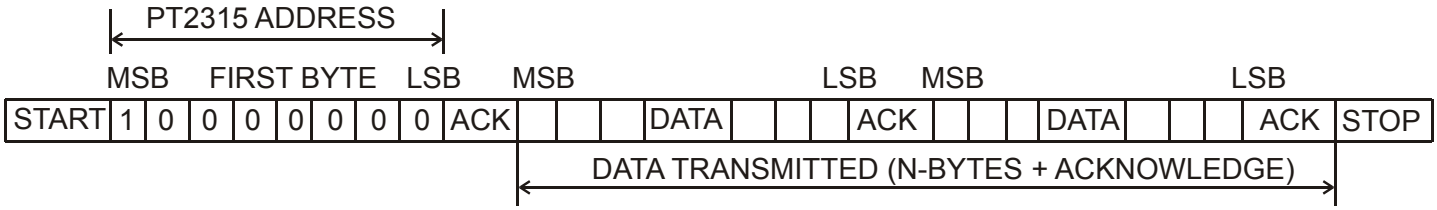
If you want to avoid the acknowledge detection of the audio processor, a simpler μP transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.

## INTERFACE PROTOCOL

The interface protocol consists of the following:

- A Start Condition
- A Chip Address Byte including the PT2315A address. The $8^{th}$ Bit of the Byte must be “0”. PT2315A must always acknowledge the end of each transmitted byte.
- A Data Sequence (N-Bytes + Acknowledge)
- A Stop Condition

Please refer to the diagram below:




Notes:
1. ACK=Acknowledge
2. Max. Clock Speed=100K Bits/s



# *SOFTWARE SPECIFICATION*

## PT2315A ADDRESS

PT2315A Address is shown below.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1<br>MSB | 0 | 0 | 0 | 0 | 0 | 0 | 0<br>LSB |

## DATA BYTES

| MSB | | | | | | | LSB | Function |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | B2 | B1 | B0 | A2 | A1 | A0 | Volume Control |
| 1 | 0 | 0 | B1 | B0 | A2 | A1 | A0 | Speaker ATT L |
| 1 | 0 | 1 | B1 | B0 | A2 | A1 | A0 | Speaker ATT R |
| 0 | 1 | 0 | * | * | L | * | * | Loudness Control |
| 0 | 1 | 1 | 0 | C3 | C2 | C1 | C0 | Bass Control |
| 0 | 1 | 1 | 1 | C3 | C2 | C1 | C0 | Treble Control |

where Ax=1.25dB steps; Bx=10dB steps; Cx=2dB steps; *=no effect

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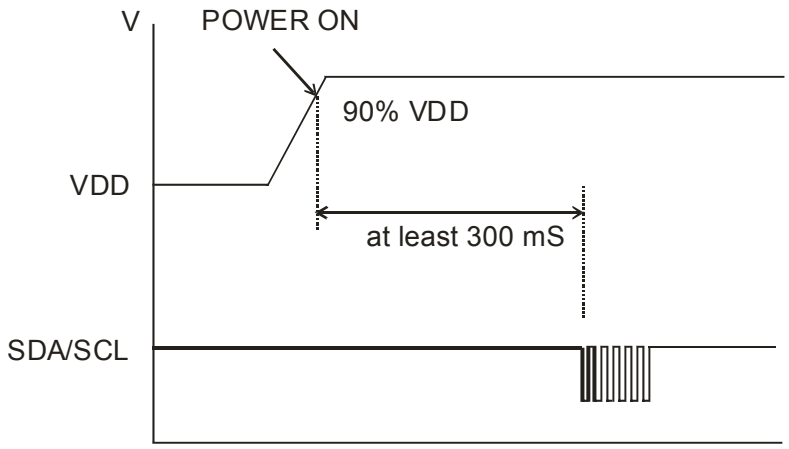
## *I²C BUS INTERFACE START TIME*

After Power is turned ON, PT2315A needs to wait for a short time in order to insure stability. This waiting period is relative to the value of Cref. As the Cref value is 10μf, the waiting time period for PT2315A to send I²C Bus Signal is at least 300ms. If the waiting time period is less than 300ms, I²C Control may fail. Please refer to the diagram below.



## *VOLUME*

The table below gives a detailed description of the Volume Data Bytes. For example, a volume of -37.5dB is given by 0 0 0 1 1 1 1 0.



| MSB | | | | | | | LSB | Function |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | B2 | B1 | B0 | A2 | A1 | A0 | Volume 1.25dB steps |
| | | | | | 0 | 0 | 0 | 0 |
| | | | | | 0 | 0 | 1 | -1.25 |
| | | | | | 0 | 1 | 0 | -2.5 |
| | | | | | 0 | 1 | 1 | -3.75 |
| | | | | | 1 | 0 | 0 | -5 |
| | | | | | 1 | 0 | 1 | -6.25 |
| | | | | | 1 | 1 | 0 | -7.5 |
| | | | | | 1 | 1 | 1 | -8.75 |
| 0 | 0 | B2 | B1 | B0 | A2 | A1 | A0 | Volume 10dB steps |
| | | 0 | 0 | 0 | | | | 0 |
| | | 0 | 0 | 1 | | | | -10 |
| | | 0 | 1 | 0 | | | | -20 |
| | | 0 | 1 | 1 | | | | -30 |
| | | 1 | 0 | 0 | | | | -40 |
| | | 1 | 0 | 1 | | | | -50 |
| | | 1 | 1 | 0 | | | | -60 |
| | | 1 | 1 | 1 | | | | -70 |

## SPEAKER ATTENUATORS

The table below gives a detailed description of the speaker attenuators data bytes. For example, an attenuation of 30dB on the Speaker L (Left) is given by 1 0 0 1 1 0 0 0.

| MSB | | | | | | | LSB | Function |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | B1 | B0 | A2 | A1 | A0 | Speaker L |
| 1 | 0 | 1 | B1 | B0 | A2 | A1 | A0 | Speaker R |
| | | | | | 0 | 0 | 0 | 0 |
| | | | | | 0 | 0 | 1 | -1.25 |
| | | | | | 0 | 1 | 0 | -2.5 |
| | | | | | 0 | 1 | 1 | -3.75 |
| | | | | | 1 | 0 | 0 | -5 |
| | | | | | 1 | 0 | 1 | -6.25 |
| | | | | | 1 | 1 | 0 | -7.5 |
| | | | | | 1 | 1 | 1 | -8.75 |
| | | | 0 | 0 | | | | 0 |
| | | | 0 | 1 | | | | -10 |
| | | | 1 | 0 | | | | -20 |
| | | | 1 | 1 | | | | -30 |
| | | | 1 | 1 | 1 | 1 | 1 | Mute |



## LOUDNESS FUNCTION

The following table shows the detailed description of the Loudness Function. For example, when the Loudness Function is turned ON, the code format is 0 1 0 0 0 0 0 0

| MSB | | | | | | | LSB | Function |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 0 | * | * | L | * | * | Loudness Control |
| | | | | | 0 | | | Loudness ON |
| | | | | | 1 | | | Loudness OFF |

Note: *=No Effect

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## *BASS AND TREBLE DATA BYTES*

The following table shows a detailed description of the Bass and Treble Data Byte. For example a Treble at -12dB is given by 0 1 1 1 0 0 0 1.



| MSB | | | | | | | LSB | Function |
|---|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 0 | C3 | C2 | C1 | C0 | Bass |
| 0 | 1 | 1 | 1 | C3 | C2 | C1 | C0 | Treble |
| | | | | 0 | 0 | 0 | 0 | -14 |
| | | | | 0 | 0 | 0 | 1 | -12 |
| | | | | 0 | 0 | 1 | 0 | -10 |
| | | | | 0 | 0 | 1 | 1 | -8 |
| | | | | 0 | 1 | 0 | 0 | -6 |
| | | | | 0 | 1 | 0 | 1 | -4 |
| | | | | 0 | 1 | 1 | 0 | -2 |
| | | | | 0 | 1 | 1 | 1 | 0 |
| | | | | | | | | |
| | | | | 1 | 1 | 1 | 1 | 0 |
| | | | | 1 | 1 | 1 | 0 | 2 |
| | | | | 1 | 1 | 0 | 1 | 4 |
| | | | | 1 | 1 | 0 | 0 | 6 |
| | | | | 1 | 0 | 1 | 1 | 8 |
| | | | | 1 | 0 | 1 | 0 | 10 |
| | | | | 1 | 0 | 0 | 1 | 12 |
| | | | | 1 | 0 | 0 | 0 | 14 |

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# ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Operating supply voltage | $V_S$ | - | 10.5 | V |
| Input current, any pin except supplies | Iin | -10 | 10 | mA |
| Input voltage (see Note) | Vin | -0.3 | $V_S$+0.3 | V |
| Operating temperature | Topr | -40 | 85 | ℃ |
| Storage temperature | Tstg | -65 | 150 | ℃ |



Note: Transient Currents of up to 100mA will not cause SCR latch-up.

# QUICK REFERENCE DATA

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_S$ | 6 | 9 | 10 | V |
| Max. input signal handling | $V_{CL}$ | 2 | 2.5 | - | Vrms |
| Total harmonic distortion (V = 1Vrms, f = 1KHz) | THD | - | 0.03 | 0.07 | % |
| Signal to noise ratio | S/N | - | 95 | - | dB |
| Channel separation (f=1KHz) | Sc | - | 85 | - | dB |
| Volume control 1.25dB step | | -75 | - | 0 | dB |
| Bass & treble control 2dB step | | -14 | - | +14 | dB |
| Balance control 1.25dB step | | -37.5 | - | 0 | dB |
| Mute attenuation | | - | 95 | - | dB |

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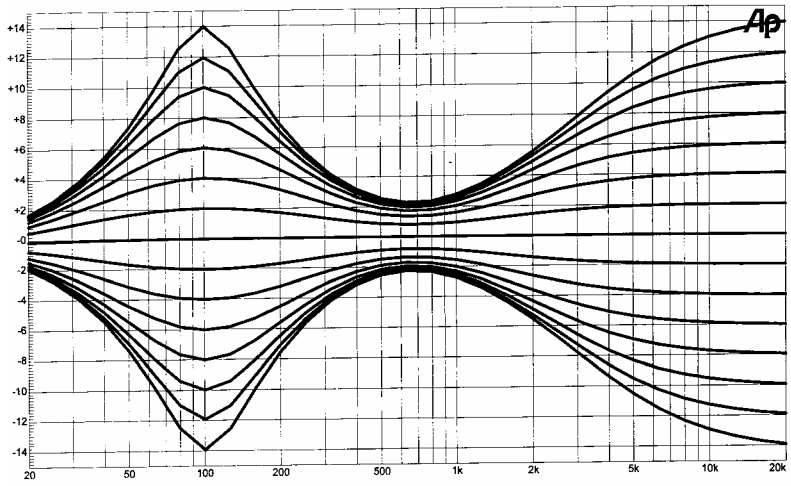
# ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃, $V_{DD}$=9V, $R_L$=100KΩ, Rg=600Ω, all controls flat<G=0>, f=1KHz)

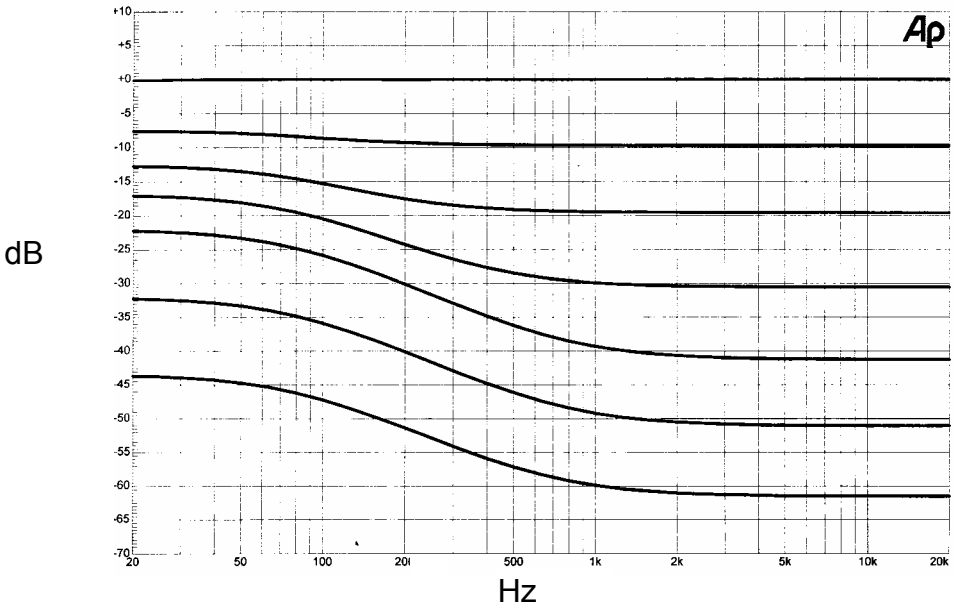
| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Supply** | | | | | | |
| Supply voltage | $V_{DD}$ | | 6 | 9 | 10 | V |
| Supply current | $I_S$ | | - | 30 | 40 | mA |
| **Volume Control** | | | | | | |
| Input resistance | $R_{IV}$ | | 15 | 25 | 35 | KΩ |
| Control range | $C_{RANGE}$ | | 70 | 75 | 80 | dB |
| Min. attenuation | $A_{VMIN}$ | | -1 | 0 | 1 | dB |
| Max. attenuation | $A_{VMAX}$ | | 70 | 75 | 80 | dB |
| Step resolution | $A_{STEP}$ | | 0.5 | 1.25 | 1.75 | dB |
| Attenuation set error | $E_A$ | $A_V$=0 to -20dB<br>$A_V$=-20 to -60dB | -1.25<br>-3.0 | 0 | 1.25<br>2.0 | dB<br>dB |
| **Speaker Attenuators** | | | | | | |
| Control range | $C_{RANGE}$ | | 35 | 37.5 | 40 | dB |
| Step resolution | $S_{STEP}$ | | 0.5 | 1.25 | 1.75 | dB |
| Attenuation set error | $E_A$ | | - | - | 1.5 | dB |
| Output mute attenuation | $A_{MUTE}$ | | 90 | 95 | - | dB |
| **Bass Control (see Note)** | | | | | | |
| Control range | Gb | Max. Boost/Cut | ±12 | ±14 | ±16 | dB |
| Step resolution | $B_{STEP}$ | | 1 | 2 | 3 | dB |
| Internal feedback resistance | $R_B$ | | 40 | 50 | 60 | KΩ |
| **Treble Control (see Note)** | | | | | | |
| Control range | Gt | Max. Boost/Cut | ±13 | ±14 | ±15 | dB |
| Step resolution | $T_{STEP}$ | | 1 | 2 | 3 | dB |
| **Audio Outputs** | | | | | | |
| Clipping level | $V_{OCL}$ | AV=-8.75dB, d=0.3% | 2 | 2.5 | - | Vrms |
| Output resistance | $R_{OUT}$ | | - | 40 | 45 | Ω |
| DC voltage level | $V_{OUT}$ | | 4.2 | 4.5 | 4.8 | V |
| Load impedance | $R_L$ | | 10 | - | - | KΩ |

| Parameter | Symbol | Test Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **General** | | | | | | |
| Output noise | $N_O$ | BW=20~20KHz, flat<br>Output Muted<br>All gains=0dB | - | -100<br>-95 | - | dB |
| | | A Curve<br>All Gains=0dB | - | -98 | - | dB |
| Signal to noise ratio | S/N | All Gains=0dB<br>$V_O$=1Vrms | - | 95 | - | dB |
| Distortion | D | $A_V$=0,$V_{IN}$=1Vrms<br>$A_V$=0dB,<br>$V_{IN}$=0.2Vrms | - | 0.03<br>0.03 | 0.07<br>0.05 | % |
| Channel separation left/right | Sc | | 80 | 90 | - | dB |
| **Bus Inputs** | | | | | | |
| Input low voltage | $V_{IL}$ | | - | - | 1 | V |
| Input high voltage | $V_{IH}$ | | 3 | - | - | V |
| Input current | $I_{IN}$ | | -5 | - | +5 | μA |
| Output voltage SDA acknowledge | $V_O$ | $I_O$=1.6mA | - | - | 0.4 | V |

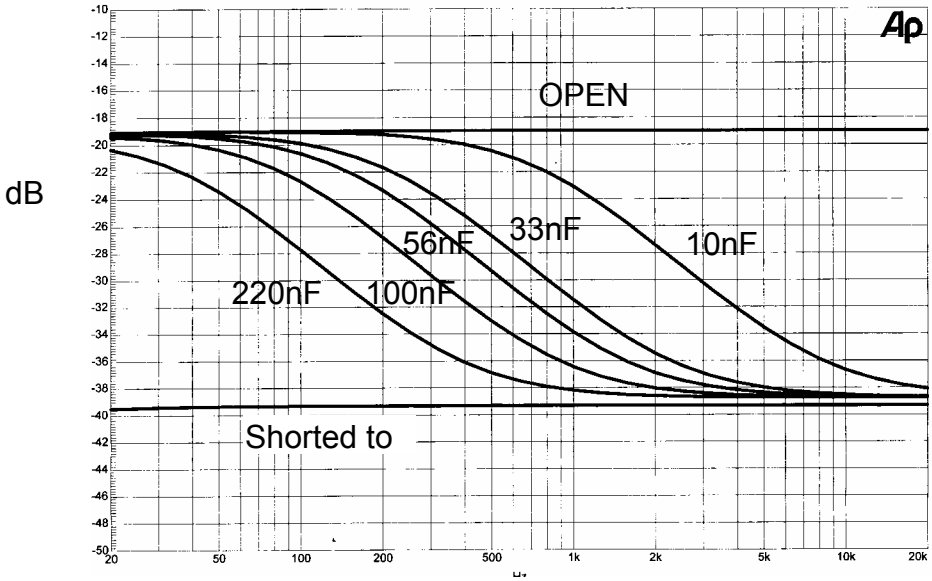
Note: For the Bass and Treble Response, please refer to the diagram below. The center frequency and quality of the resonance behavior can be selected by the external circuitry. A standard first order bass response can realized by a standard feedback network.




**Typical Tone Response**



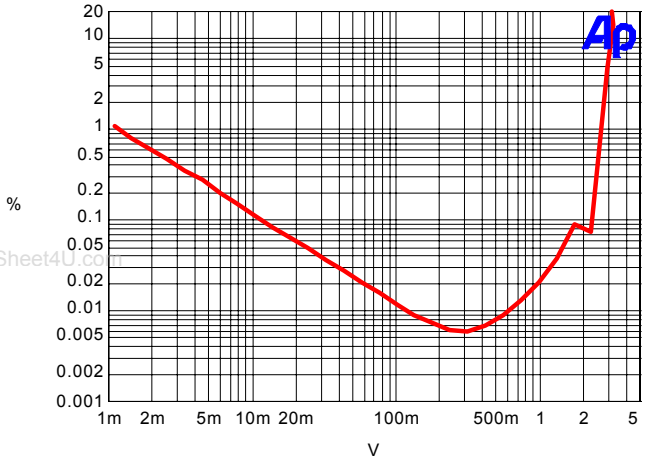

**Loudness vs Volume Attenuation Frequency Response ($C_{10}$=$C_{11}$=100nF)**



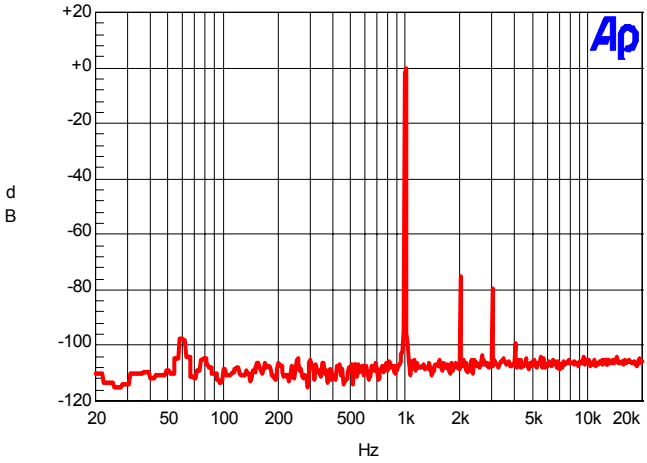



**$C_{10}$, $C_{11}$ vs. Loudness Frequency Response (Volume=-40dB, All other controls are flat)**

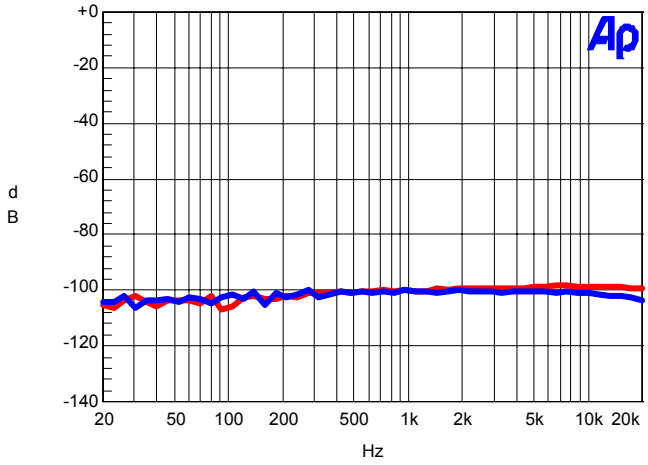
# ELECTRICAL CHARACTERISTICS DIAGRAMS




Total Harmonic Distortion and Amplitude

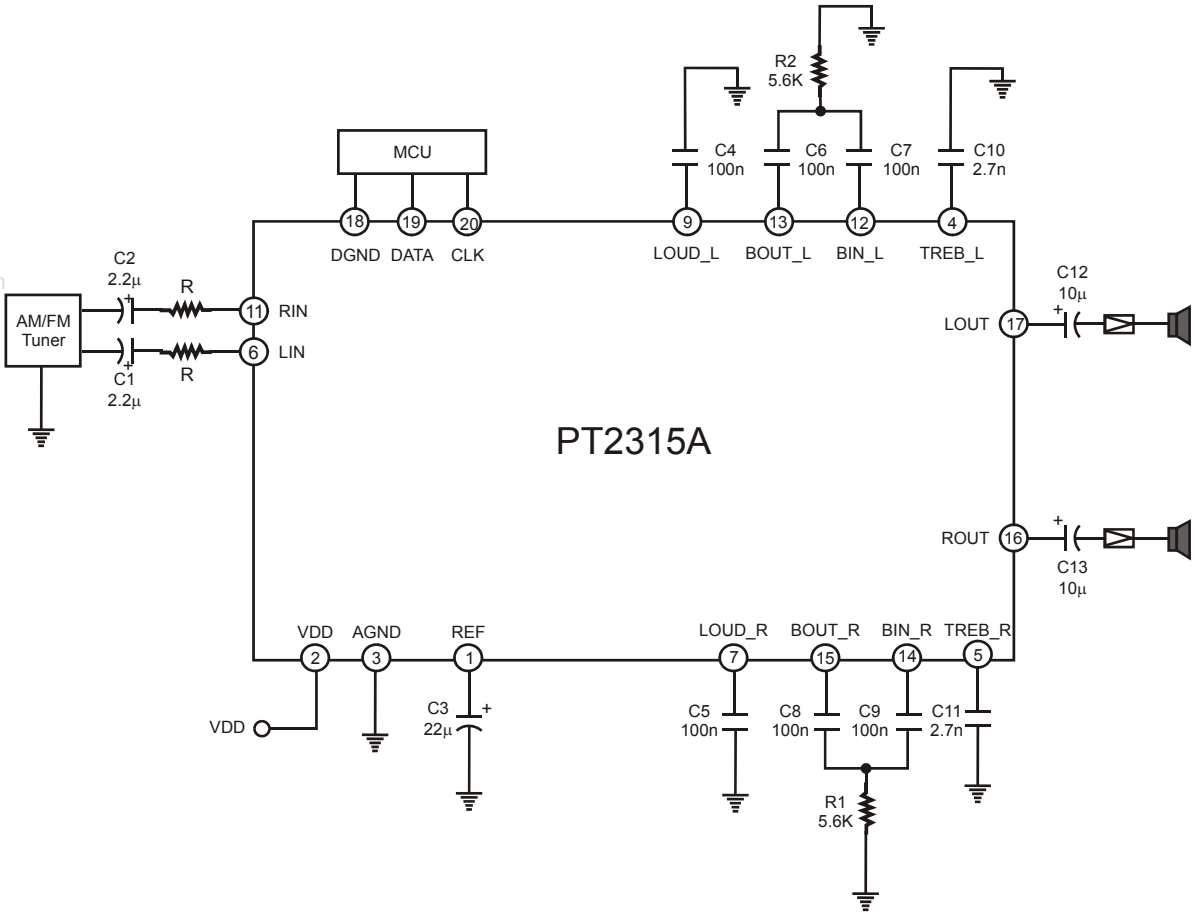



1Vrms Output FFT Analysis




Left and Right Channel Crosstalk

# APPLICATION CIRCUIT




Notes:
1. It is suggested that you use Mylar Capacitor for capacitors, C4 ~ C11.
2. Recommended Value of Resistor (R)=1K.

# ORDER INFORMATION

| Valid Part Number | Package Information | Top Code |
|---|---|---|
| PT2315A-D | 20 Pins, DIP, 300mil | PT2315A-D |
| PT2315A | 20 Pins, SOP, 300mil | PT2315A |
| PT2315A-D (L) | 20 Pins, DIP, 300mil | PT2315A-D |
| PT2315A (L) | 20 Pins, SOP, 300mil | PT2315A |



Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the date code.

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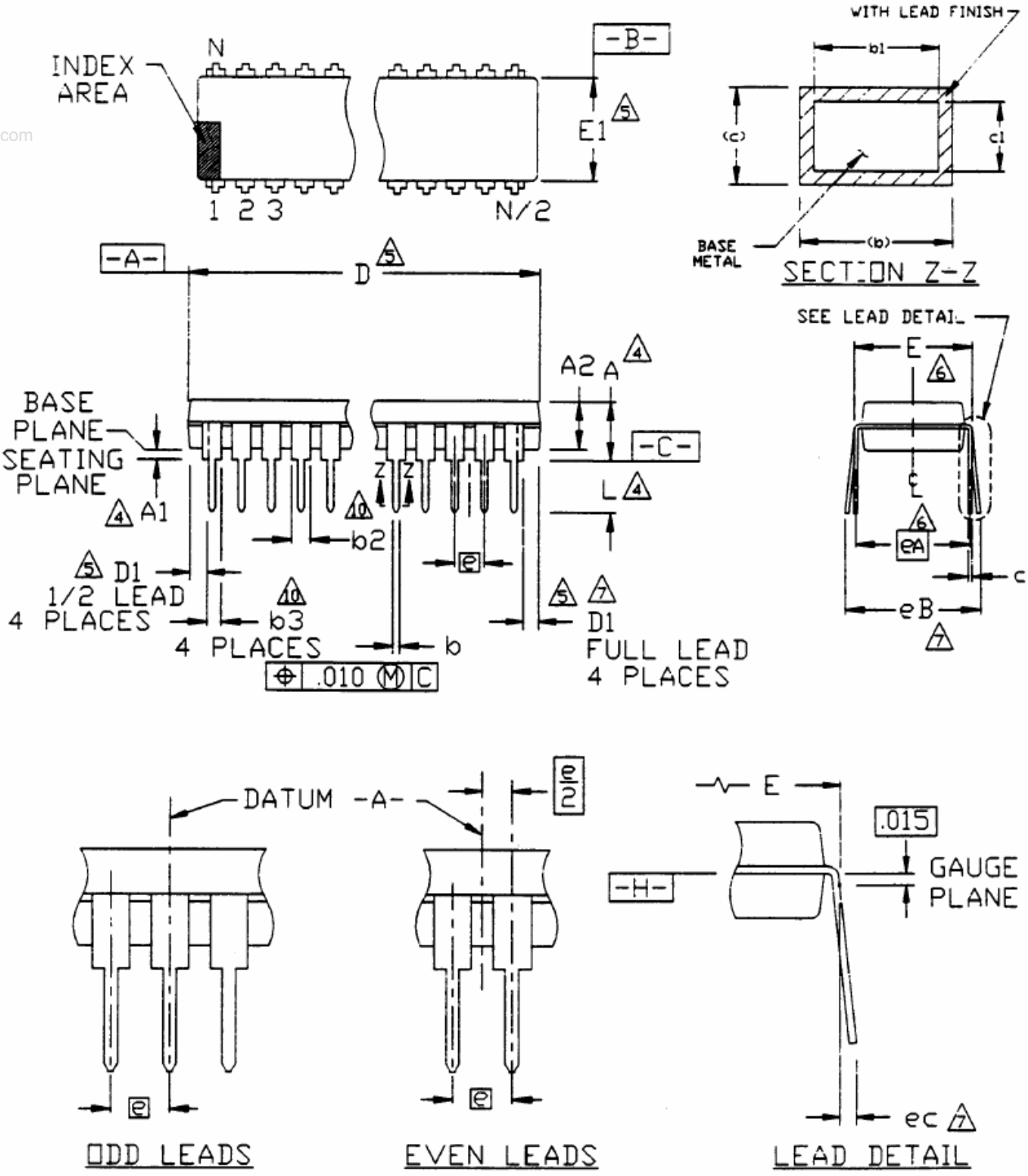
# PACKAGE INFORMATION

## *20 PINS, DIP, 300MIL*





| Symbol | Min. | Nom. | Max. |
|---|---|---|---|
| A | | | 0.210 |
| A1 | 0.015 | | |
| A2 | 0.115 | 0.130 | 0.195 |
| b | 0.014 | 0.018 | 0.022 |
| b1 | 0.014 | 0.018 | 0.020 |
| b2 | 0.045 | 0.060 | 0.070 |
| b3 | 0.030 | 0.039 | 0.045 |
| c | 0.008 | 0.010 | 0.014 |
| c1 | 0.008 | 0.010 | 0.011 |
| D | 0.980 | 1.030 | 1.060 |
| D1 | 0.005 | | |
| E | 0.300 | 0.310 | 0.325 |
| E1 | 0.240 | 0.250 | 0.280 |
| e | | 0.100 bsc. | |
| eA | | 0.300 bsc. | |
| eB | | | 0.430 |
| eC | 0.000 | | 0.060 |
| L | 0.115 | 0.130 | 0.150 |



Notes:
1. All dimensions are in INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension ”A”, ”A1” and ”L” are measured with the package seated in JEDEC Seating Plane Gauge GS-3
4. “D”，”D1” and “E1” dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. “E” and “eA” measured with the leads constrained to be perpendicular to datum -c- .
6. “eB” and “eC” are measured at the lead tips with the leads unconstrained.
7. N is the number of the terminal positions (N=20)
8. Pointed or rounded lead tips are preferred to ease insertion.
9. “b2” and “b3” maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm)
10. Distance between leads including Dambar protrusions to be 0.005 inch minimum.
11. Datum plane -H- coincident with the bottom of lead, where lead exits body.
12. Refer to JEDEC MS-001, Variation AD.

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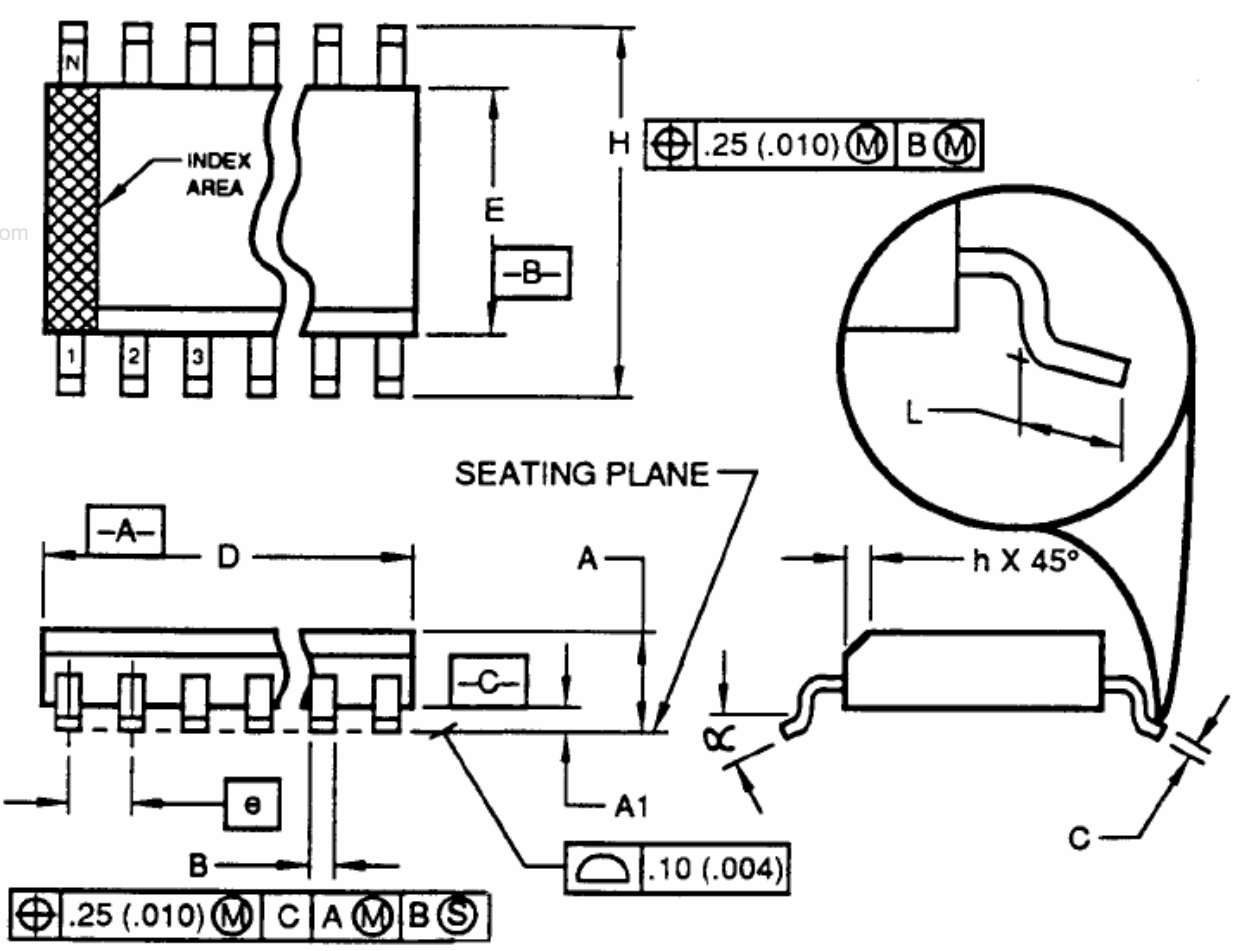
## *20 PINS, SOP, 300MIL*






| Symbol | Min. | Nom. | Max. |
|---|---|---|---|
| A | 2.35 | | 2.65 |
| A1 | 0.10 | | 0.30 |
| B | 0.33 | | 0.51 |
| C | 0.23 | | 0.32 |
| D | 12.60 | | 13.00 |
| E | 7.40 | | 7.60 |
| e | | 1.27 bsc. | |
| H | 10.00 | | 10.65 |
| h | 0.25 | | 0.75 |
| L | 0.40 | | 1.27 |
| $\alpha$ | 0° | | 8° |

Notes:
1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold Flash, protrusion or gate burrs shall not exceed 0.15 mm (0.006 in) per side.
3. Dimension “E” does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25 mm (0.010 in) per side.
4. The chamfer on the body is optional. It is not present, a visual index feature must be located within the crosshatched area.
5. “L” is the length of the terminal for soldering to a substrate.
6. N is the number of the terminal positions (N=20)
7. The lead width “B” as measured 0.36 mm (0.014 in) or greater above the seating plane, shall not exceed a maximum value of 0.61 mm (0.24 in).
8. Controlling dimension: MILLIMETER.
9. Refer to JEDEC MS-013, Variation AC.

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