Atmel ATmega169A/PA/329A/PA/3290A/PA/649A/P/6490A/P

8-bit Atmel Microcontroller with 16/32/64KB In-System Programmable Flash

SUMMARY

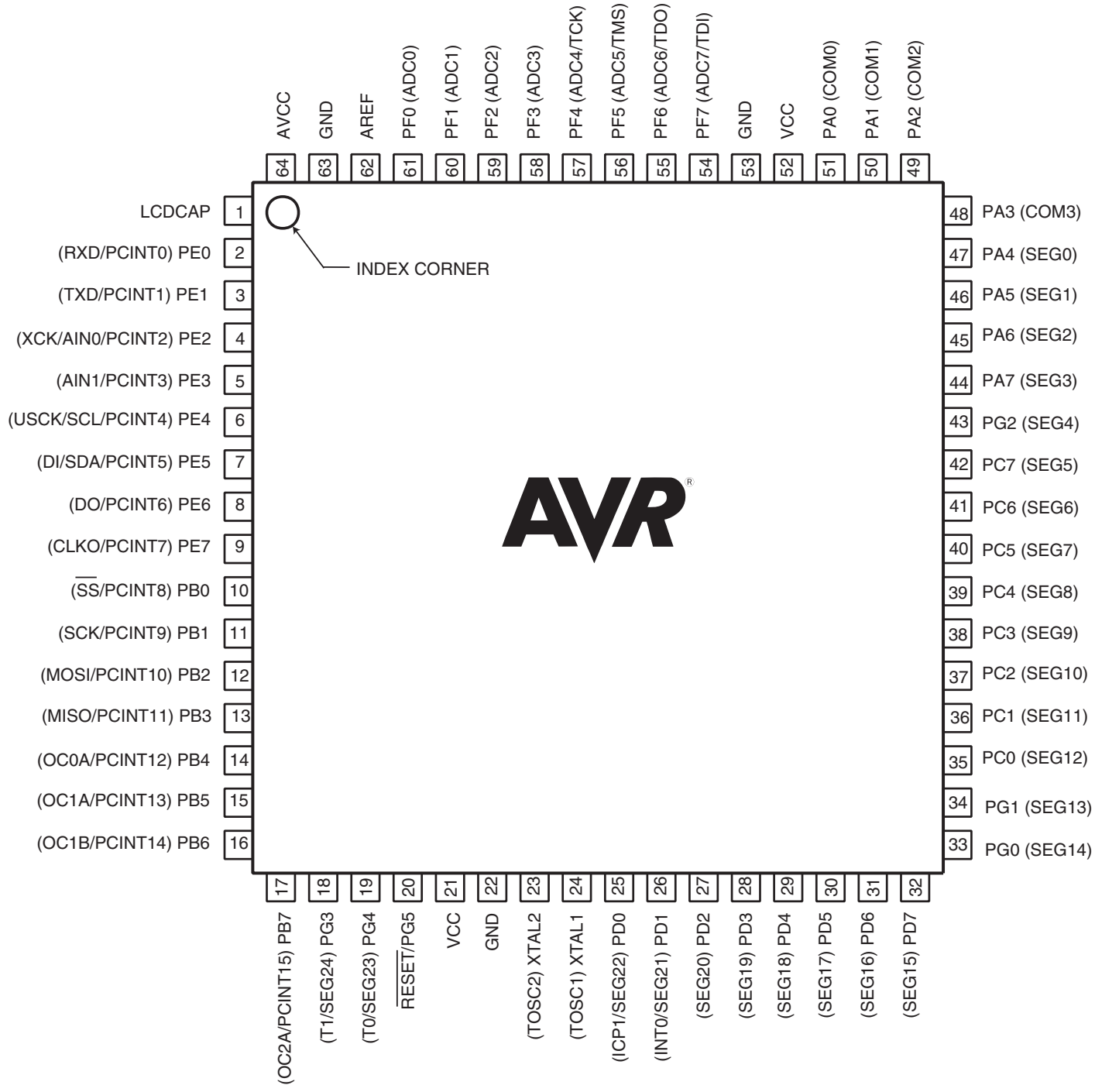
Features

- High performance, low power Atmel® AVR® 8-Bit Microcontroller
- Advanced RISC architecture
  - 130 powerful instructions – most single clock cycle execution
  - 32 × 8 general purpose working registers
  - Fully static operation
  - Up to 16MIPS throughput at16MHz (Atmel ATmega169A/169PA/649A/649P)
  - Up to 20 MIPS throughput at 20MHz (Atmel ATmega329A/329PA/3290A/3290PA/6490A/6490P)
  - On-chip 2-cycle multiplier
- High endurance non-volatile memory segments
  - In-system self-programmable flash program memory
    - 16Kbytes (Atmel ATmega169A/ATmega169PA)
    - 32Kbytes (Atmel ATmega329A/ATmega329PA/ATmega3290A/ATmega3290PA)
    - 64Kbytes (Atmel ATmega649A/ATmega649P/ATmega6490A/ATmega6490P)
  - EEPROM
    - 512bytes (ATmega169A/ATmega169PA)
    - 1Kbytes (ATmega329A/ATmega329PA/ATmega3290A/ATmega3290PA)
    - 2Kbytes (ATmega649A/ATmega649P/ATmega6490A/ATmega6490P)
  - Internal SRAM
    - 1Kbytes (ATmega169A/ATmega169PA)
    - 2Kbytes (ATmega329A/ATmega329PA/ATmega3290A/ATmega3290PA)
    - 4Kbytes (ATmega649A/ATmega649P/ATmega6490A/ATmega6490P)
  - Write/erase cyles: 10,000 flash/100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C [1]
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True read-while-write operation
  - Programming lock for software security
- Atmel QTouch® library support
  - Capacitive touch buttons, sliders and wheels
  - Atmel QTouch and QMatrix acquisition
  - Up to 64 sense channels
- JTAG (IEEE std. 1149.1 compliant) Interface
  - Boundary-scan capabilities according to the JTAG standard
  - Extensive on-chip debug support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral features
  - 4 × 25 segment LCD driver (ATmega169A/ATmega169PA/ATmega329A/ATmega329PA/ATmega649A/ATmega649P)
  - 4 × 40 segment LCD driver (ATmega3290A/ATmega3290PA/ATmega6490A/ATmega6490P)
  - Two 8-bit Timer/Counters with Separate Prescaler and Compare mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare mode, and Capture mode
  - Real Time Counter with separate oscillator
  - Four PWM channels
  - 8-channel, 10-bit ADC
  - Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Universal Serial Interface with Start Condition Detector
  - Programmable Watchdog Timer with Separate On-chip oscillator
  - On-chip analog comparator
  - Interrupt and Wake-up on pin change
- Special microcontroller features
  - Power-on reset and programmable Brown-out detection
  - Internal calibrated oscillator
  - External and internal interrupt sources
  - Five sleep modes: Idle, ADC Noise Reduction, Power-save, Power-down, and Standby
- I/O and packages
  - 54/69 programmable I/O lines
  - 64/100-lead TQFP, 64-pad QFN/MLF, and 64-pad DRQFN
- Speed Grade:
  - ATmega169A/169PA/649A/649P:
    - 0 - 16MHz @ 1.8 - 5.5V
  - ATmega3290A/3290PA/6490A/6490P:
    - 0 - 20MHz @ 1.8 - 5.5V
- Temperature range:
  - -40°C to 85°C industrial
- Ultra-low power consumption (picoPower® devices)
  - Active mode:
    - 1MHz, 1.8V: 215µA
    - 32kHz, 1.8V: 8µA (including oscillator)
    - 32kHz, 1.8V: 25µA (including oscillator and LCD)
  - Power-down mode:
    - 0.1µA at 1.8V
  - Power-save mode:
    - 0.6µA at 1.8V (Including 32kHz RTC)
    - 750nA at 1.8V

1. Pin configurations

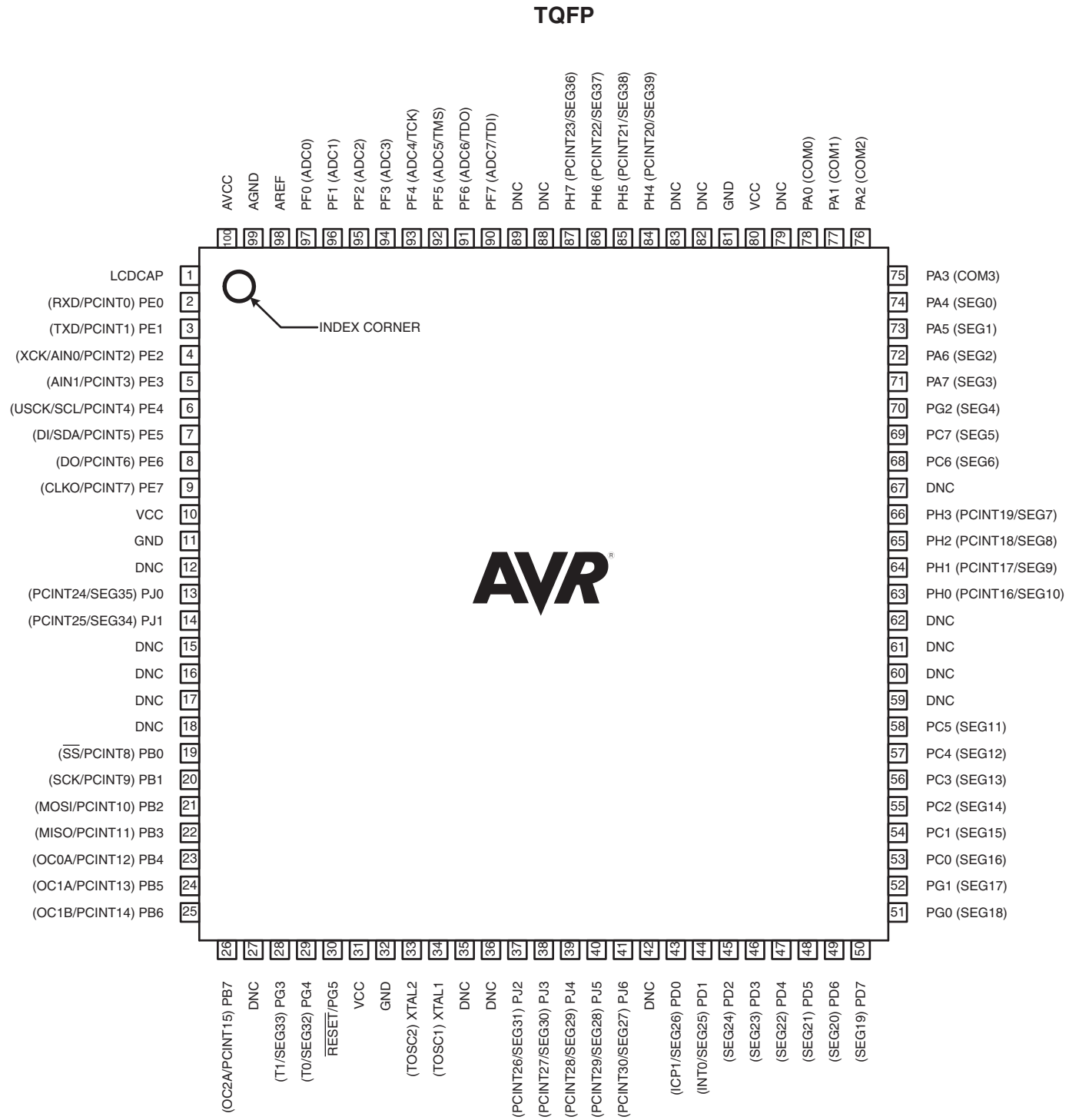
1.1 Pinout - 64A (TQFP) and 64M1 (QFN/MLF)

Figure 1-1. Pinout Atmel ATmega169A/ATmega169PA/ATmega329A/ATmega329PA/ATmega649A/ATmega649P.



1.2 Pinout - 100A (TQFP)

Figure 1-2. Pinout Atmel ATmega3290A/ATmega3290PA/ATmega6490A/ATmega6490P.



Note: The large center pad underneath the QFN/MLF packages is made of metal and internally connected to GND. It should be soldered or glued to the board to ensure good mechanical stability. If the center pad is left unconnected, the package might loosen from the board.

1.3 Pinout - 64MC (DRQFN)

Figure 1-3. Pinout Atmel ATmega169A/ATmega169PA.

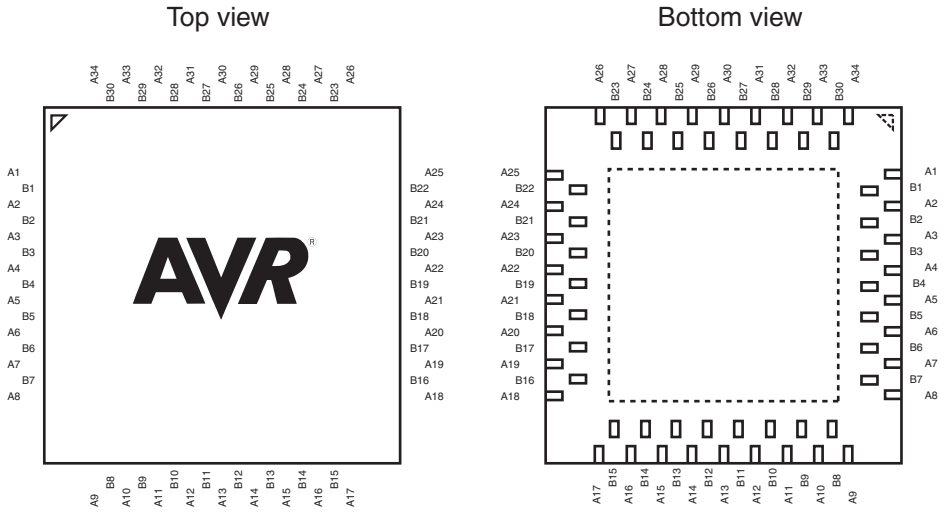


Table 1-1. DRQFN-64 Pinout ATmega169A/ATmega169PA.

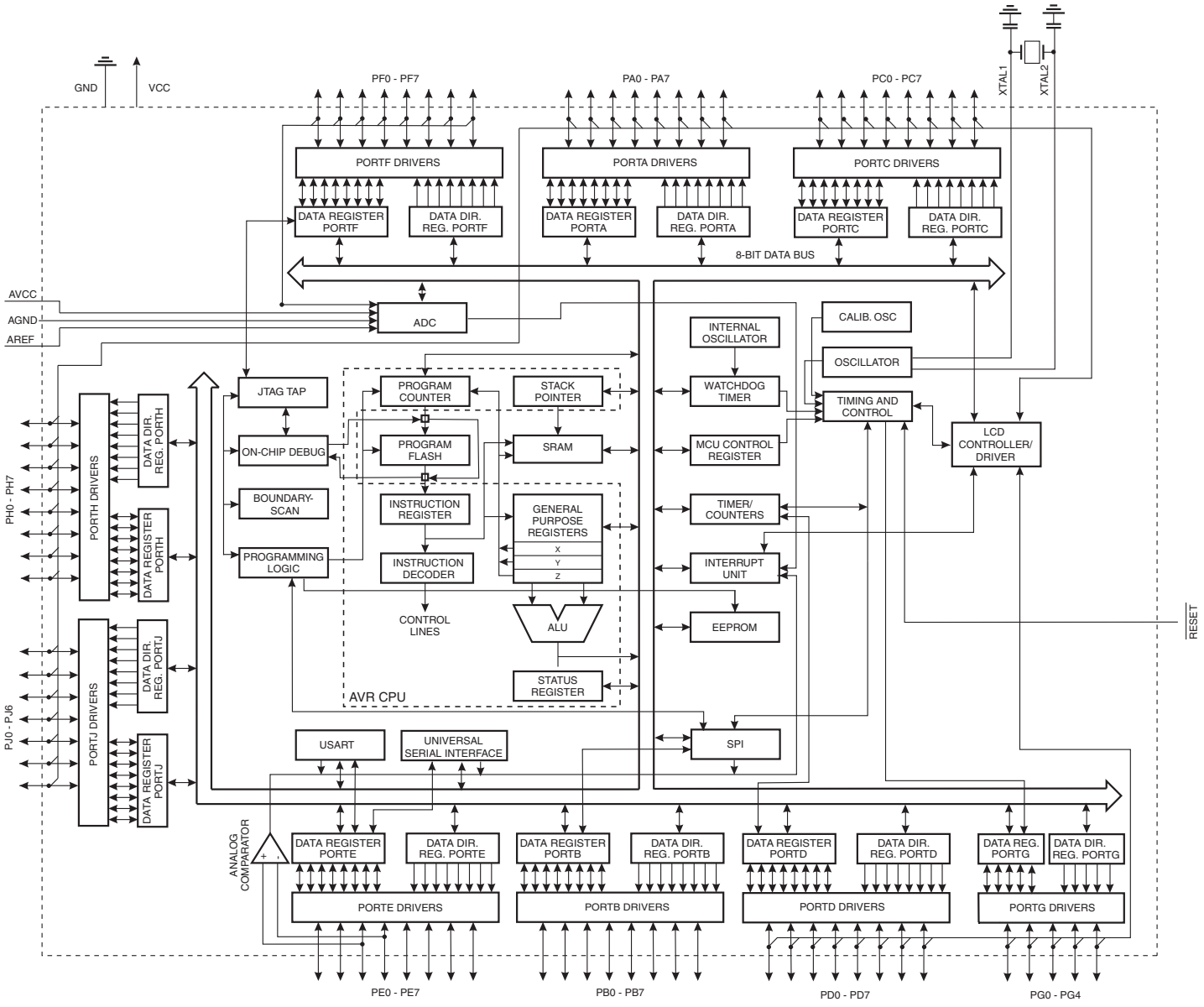
A1	PE0	**A9**	PB7	**A18**	PG1 (SEG13)	**A26**	PA2 (COM2)
B1	VLCDCAP	**B8**	PB6	**B16**	PG0 (SEG14)	**B23**	PA3 (COM3)
A2	PE1	**A10**	PG3	**A19**	PC0 (SEG12)	**A27**	PA1 (COM1)
B2	PE2	**B9**	PG4	**B17**	PC1 (SEG11)	**B24**	PA0 (COM0)
A3	PE3	**A11**	$\overline{\text{RESET}}$	**A20**	PC2 (SEG10)	**A28**	VCC
B3	PE4	**B10**	VCC	**B18**	PC3 (SEG9)	**B25**	GND
A4	PE5	**A12**	GND	**A21**	PC4 (SEG8)	**A29**	PF7
B4	PE6	**B11**	XTAL2 (TOSC2)	**B19**	PC5 (SEG7)	**B26**	PF6
A5	PE7	**A13**	XTAL1 (TOSC1)	**A22**	PC6 (SEG6)	**A30**	PF5
B5	PB0	**B12**	PD0 (SEG22)	**B20**	PC7 (SEG5)	**B27**	PF4
A6	PB1	**A14**	PD1 (SEG21)	**A23**	PG2 (SEG4)	**A31**	PF3
B6	PB2	**B13**	PD2 (SEG20)	**B21**	PA7 (SEG3)	**B28**	PF2
A7	PB3	**A15**	PD3 (SEG19)	**A24**	PA6 (SEG2)	**A32**	PF1
B7	PB5	**B14**	PD4 (SEG18)	**B22**	PA4 (SEG0)	**B29**	PF0
A8	PB4	**A16**	PD5 (SEG17)	**A25**	PA5 (SEG1)	**A33**	AREF
		B15	PD7 (SEG15)			**B30**	AVCC
		A17	PD6 (SEG16)			**A34**	GND

2. Overview

The Atmel ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P is a low-power CMOS 8-bit microcontroller based on the Atmel®AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block diagram

Figure 2-1. Block diagram.



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The Atmel ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P provides the following features: 16K/32K/64K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512/1K/2K bytes EEPROM, 1K/2K/4K byte SRAM, 54/69 general purpose I/O lines, 32 general purpose working registers, a JTAG interface for Boundary-scan, On-chip Debugging support and programming, a complete On-chip LCD controller with internal contrast control, three flexible Timer/Counters with compare modes, internal and external interrupts, a serial programmable USART, Universal Serial Interface with Start Condition Detector, an 8-channel, 10-bit ADC, a programmable Watchdog Timer with internal Oscillator, an SPI serial port, and five software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or hardware reset. In Power-save mode, the asynchronous timer and the LCD controller continues to run, allowing the user to maintain a timer base and operate the LCD display while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except asynchronous timer, LCD controller and ADC, to minimize switching noise during ADC conversions. In Standby mode, the XTAL/resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low-power consumption.

Atmel offers the QTouch library for embedding capacitive touch buttons, sliders and wheels functionality into AVR microcontrollers. The patented charge-transfer signal acquisition offers robust sensing and includes fully debounced reporting of touch keys and includes Adjacent Key Suppression® (AKS®) technology for unambiguous detection of key events. The easy-to-use QTouch Suite toolchain allows you to explore, develop and debug your own touch applications.

The device is manufactured using the Atmel high density non-volatile memory technology. The On-chip In-System re-Programmable (ISP) Flash allows the program memory to be reprogrammed In-System through an SPI serial interface, by a conventional non-volatile memory programmer, or by an On-chip Boot program running on the AVR core. The Boot program can use any interface to download the application program in the Application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation.

By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P AVR is supported with a full suite of program and system development tools including: C Compilers, Macro Assemblers, Program Debugger/Simulators, In-Circuit Emulators, and Evaluation kits.

2.2 Comparison between Atmel ATmega169A/169PA/329A/329PA/649A/649P/3290A/3290PA/6490A/6490P

Table 2-1. Differences between: ATmega169A/169PA/329A/329PA/649A/649P/3290A/3290PA/6490A/6490P.

Device	Flash	EEPROM	RAM	LCD Segments
ATmega169A	16Kbyte	512Bytes	1Kbyte	4 × 25
ATmega169PA	16Kbyte	512Bytes	1Kbyte	4 × 25
ATmega329A	32Kbyte	1Kbyte	2Kbyte	4 × 25
ATmega329PA	32Kbyte	1Kbyte	2Kbyte	4 × 25
ATmega3290A	32Kbytes	1Kbyte	2Kbyte	4 × 40
ATmega3290PA	32Kbyte	1Kbyte	2Kbyte	4 × 40
ATmega649A	64Kbyte	2Kbyte	4Kbyte	4 × 25
ATmega649P	64Kbyte	2Kbyte	4Kbyte	4 × 25
ATmega6490A	64Kbyte	2Kbyte	4Kbyte	4 × 40
ATmega6490P	64Kbyte	2Kbyte	4Kbyte	4 × 40

2.3 Pin descriptions

The following section describes the I/O-pin special functions.

2.3.1 V_{CC}

Digital supply voltage.

2.3.2 GND

Ground.

2.3.3 Port A (PA7...PA0)

Port A is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the Atmel ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on page 73.

2.3.4 Port B (PB7...PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B has better driving capabilities than the other ports.
Port B also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on page 74.

2.3.5 Port C (PC7...PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on page 77.

2.3.6 Port D (PD7...PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on page 78.

2.3.7 Port E (PE7...PE0)

Port E is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port E output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port E pins that are externally pulled low will source current if the pull-up resistors are activated. The Port E pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port E also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on page 80.

2.3.8 Port F (PF7...PF0)

Port F serves as the analog inputs to the A/D Converter.

Port F also serves as an 8-bit bi-directional I/O port, if the A/D Converter is not used. Port pins can provide internal pull-up resistors (selected for each bit). The Port F output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port F pins that are externally pulled low will source current if the pull-up resistors are activated. The Port F pins are tri-stated when a reset condition becomes active, even if the clock is not running. If the JTAG interface is enabled, the pull-up resistors on pins PF7(TDI), PF5(TMS), and PF4(TCK) will be activated even if a reset occurs.

Port F also serves the functions of the JTAG interface.

2.3.9 Port G (PG5...PG0)

Port G is a 6-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port G output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port G pins that are externally pulled low will source current if the pull-up resistors are activated. The Port G pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port G also serves the functions of various special features of the ATmega169A/169PA/329A/329PA/3290A/3290PA/649A/649P/6490A/6490P as listed on page 84.

2.3.10 Port H (PH7...PH0)

Port H is a 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port H output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port H pins that are externally pulled low will source current if the pull-up resistors are activated. The Port H pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port H also serves the functions of various special features of the ATmega3290PA/6490P as listed on page 86.

2.3.11 Port J (PJ6...PJ0)

Port J is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port J output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port J pins that are externally pulled low will source current if the pull-up resistors are activated. The Port J pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port J also serves the functions of various special features of the ATmega3290PA/6490P as listed on page 88.

2.3.12 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in ”System and reset characteristics” on page 334. Shorter pulses are not guaranteed to generate a reset.

2.3.13 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.3.14 XTAL2

Output from the inverting Oscillator amplifier.

2.3.15 AVCC

AVCC is the supply voltage pin for Port F and the A/D Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.3.16 AREF

This is the analog reference pin for the A/D Converter.

2.3.17 LCDCAP

An external capacitor (typical > 470 nF) must be connected to the LCDCAP pin as shown in Figure 24-2, if the LCD module is enabled and configured to use internal power. This capacitor acts as a reservoir for LCD power (V_{LCD}). A large capacitance reduces ripple on V_{LCD} but increases the time until V_{LCD} reaches its target value.

3. Resources

A comprehensive set of development tools, application notes and datasheets are available for download on http://www.atmel.com/avr.

4. Data retention

Reliability Qualification results show that the projected data retention failure rate is much less than 1 PPM over 20 years at 85°C or 100 years at 25°C.

5. About code examples

This documentation contains simple code examples that briefly show how to use various parts of the device. These code examples assume that the part specific header file is included before compilation. Be aware that not all C compiler vendors include bit definitions in the header files and interrupt handling in C is compiler dependent. Please confirm with the C compiler documentation for more details.

For I/O Registers located in extended I/O map, “IN”, “OUT”, “SBIS”, “SBIC”, “CBI”, and “SBI” instructions must be replaced with instructions that allow access to extended I/O. Typically “LDS” and “STS” combined with “SBRS”, “SBRC”, “SBR”, and “CBR”.

6. Capacitive touch sensing

The Atmel® QTouch® Library provides a simple to use solution to realize touch sensitive interfaces on most Atmel AVR® microcontrollers. The QTouch Library includes support for the QTouch and QMatrix® acquisition methods.

Touch sensing can be added to any application by linking the appropriate Atmel QTouch Library for the AVR Microcontroller. This is done by using a simple set of APIs to define the touch channels and sensors, and then calling the touch sensing API’s to retrieve the channel information and determine the touch sensor states.

The QTouch Library is FREE and downloadable from the Atmel website at the following location: www.atmel.com/qtouchlibrary. For implementation details and other information, refer to the Atmel QTouch Library User Guide - also available for download from the Atmel website.

7. Ordering information

7.1 Atmel ATmega169A

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
16	1.8 - 5.5V	ATmega169A-AU ATmega169A-AUR (4) ATmega169A-MU ATmega169A-MUR (4) ATmega169A-MCH ATmega169A-MCHR (4)	64A 64A 64M1 64M1 64MC 64MC	Industrial (-40°C to 85°C)
		ATmega169A-AN ATmega169A-ANR (4) ATmega169A-MN ATmega169A-MNR (4)	64A 64A 64M1 64M1	Extended (-40°C to 105°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC}, see Figure 29-1 on page 332.
4. Tape & Reel.

Package type	
64A	64-lead, thin (1.0mm) plastic Gull Wing Quad Flat Package (TQFP)
64M1	64-pad, 9 × 9 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
64MC	64-lead (2-row Staggered), 7 × 7 × 1.0mm body, 4.0 × 4.0 mm Exposed Pad, Quad Flat No-Lead Package (QFN)

7.2 Atmel ATmega169PA

Speed [MHz] [3]	Power supply	Ordering code [2]	Package type[1]	Operational range
16	1.8 - 5.5V	ATmega169PA-AU ATmega169PA-AUR[4] ATmega169PA-MU ATmega169PA-MUR[4] ATmega169PA-MCH ATmega169PA-MCHR[4]	64A 64A 64M1 64M1 64MC 64MC	Industrial (-40°C to 85°C)
		ATmega169PA-AN ATmega169PA-ANR[4] ATmega169PA-MN ATmega169PA-MNR[4]	64A 64A 64M1 64M1	Extended (-40°C to 105°C)[5]

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC}, see Figure 29-1 on page 332.
4. Tape & Reel.
5. See characterization specification at 105°C.

Package type	
64A	64-lead, thin (1.0mm) plastic Gull Wing Quad Flat Package (TQFP)
64M1	64-pad, 9 × 9 × 1.0mm body, lead pitch 0.50mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)
64MC	64-lead (2-row Staggered), 7 × 7 × 1.0mm body, 4.0 × 4.0mm Exposed Pad, Quad Flat No-Lead Package (QFN)

7.3 Atmel ATmega329A

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
20	1.8 - 5.5V	ATmega329A-AU ATmega329A-AUR (4) ATmega329A-MU ATmega329A-MUR (4)	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)
		ATmega329A-AN ATmega329A-ANR (4) ATmega329A-MN ATmega329A-MNR (4)	64A 64A 64M1 64M1	Extended (-40°C to 105°C)(5)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-2 on page 332.
4. Tape & Reel.
5. See characterization specifications at 105°C.

Package type	
64A	64-lead, 14 × 14 × 1.0mm, thin profile plastic Quad Flat Package (TQFP)
64M1	64-pad, 9 × 9 × 1.0mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

7.4 Atmel ATmega329PA

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
20	1.8 - 5.5V	ATmega329PA-AU ATmega329PA-AUR(4) ATmega329PA-MU ATmega329PA-MUR(4)	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)
		ATmega329PA-AN ATmega329PA-ANR(4) ATmega329PA-MN ATmega329PA-MNR(4)	64A 64A 64M1 64M1	Extended (-40°C to 105°C)(5)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-2 on page 332.
4. Tape &Reel.
5. See characterization specification at 105°C.

Package type	
64A	64-lead, 14 × 14 × 1.0mm, thin profile Plastic Quad Flat Package (TQFP)
64M1	64-pad, 9 × 9 × 1.0mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

7.5 Atmel ATmega3290A

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
20	1.8 - 5.5V	ATmega3290A-AU ATmega3290A-AUR (4)	100A 100A	Industrial (-40°C to 85°C)
		ATmega3290A-AN ATmega3290A-ANR (4)	100A 100A	Extended (-40°C to 105°C)(5)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-2 on page 332.
4. Tape & Reel.
5. See characterization specification at 105°C.

Package type	
100A	100-lead, 14 × 14 × 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

7.6 Atmel ATmega3290PA

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
20	1.8 - 5.5V	ATmega3290PA-AU ATmega3290PA-AUR(4)	100A 100A	Industrial (-40°C to 85°C)
		ATmega3290PA-AN ATmega3290PA-ANR(4)	100A 100A	Industrial (-40°C to 105°C)(5)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-2 on page 332.
4. Tape & Reel.
5. See characterization specification at 105°C.

Package type	
100A	100-lead, 14 × 14 × 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

7.7 Atmel ATmega649A

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
16	1.8 - 5.5V	ATmega649A-AU ATmega649A-AUR (4) ATmega649A-MU ATmega649A-MUR (4)	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-1 on page 332.
4. Tape & Reel.

Package type	
64A	64-lead, 14 × 14 × 1.0mm, Thin Profile Plastic Quad Flat Package (TQFP)
64M1	64-pad, 9 × 9 × 1.0mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

7.8 Atmel ATmega649P

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
16	1.8 - 5.5 V	ATmega649P-AU ATmega649P-AUR (4) ATmega649P-MU ATmega649P-MUR (4)	64A 64A 64M1 64M1	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-1 on page 332.
4. Tape & Reel.

Package type	
64A	64-lead, 14 × 14 × 1.0mm, Thin Profile Plastic Quad Flat Package (TQFP)
64M1	64-pad, 9 × 9 × 1.0mm, Quad Flat No-Lead/Micro Lead Frame Package (QFN/MLF)

7.9 Atmel ATmega6490A

Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
20	1.8 - 5.5V	ATmega6490A-AU ATmega6490A-AUR (4)	100A 100A	Industrial (-40°C to 85°C)

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-2 on page 332.
4. Tape & Reel.

Package type	
100A	100-lead, 14 × 14 × 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

7.10 Atmel ATmega6490P

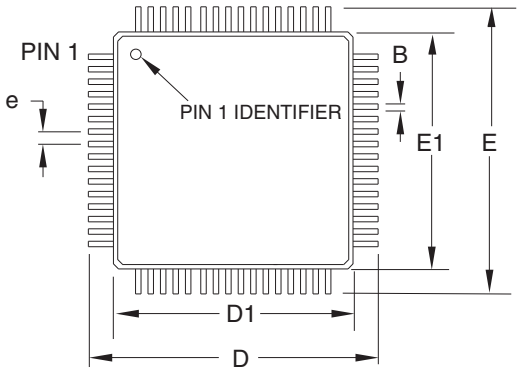
Speed [MHz] (3)	Power supply	Ordering code (2)	Package type (1)	Operational range
20	1.8 - 5.5V	ATmega6490P-AU ATmega6490P-AUR (4)	100A 100A	Industrial (-40°C to 85°C)

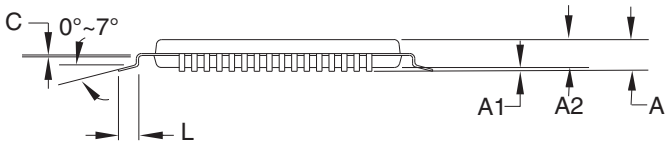
Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. For Speed vs. V_{CC} see Figure 29-2 on page 332.
4. Tape & Reel.

Package Type	
100A	100-lead, 14 × 14 × 1.0mm, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)

8. Packaging Information

8.1 64A





COMMON DIMENSIONS
(Unit of measure = mm)

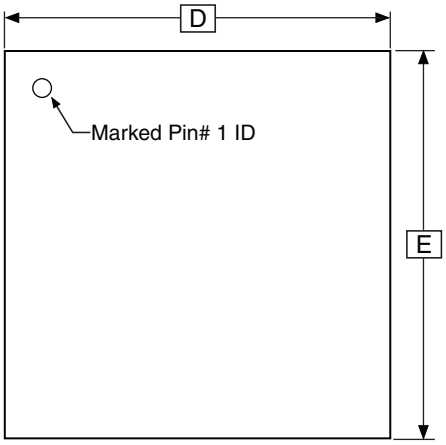
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AEB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

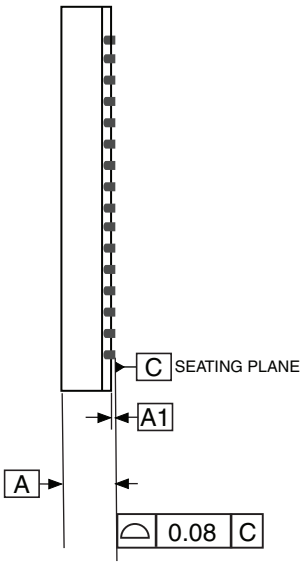
2010-10-20

	TITLE	DRAWING NO.	REV.
Atmel 2325 Orchard Parkway San Jose, CA 95131	**64A,** 64-lead, 14 x 14mm Body Size, 1.0mm Body Thickness, 0.8mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	64A	C

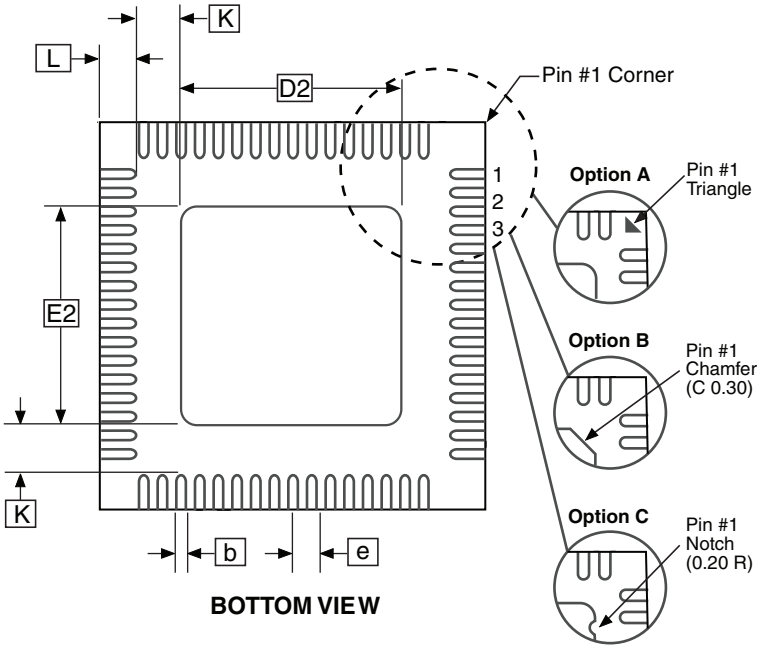
8.2 64M1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

COMMON DIMENSIONS
(Unit of Measure = mm)

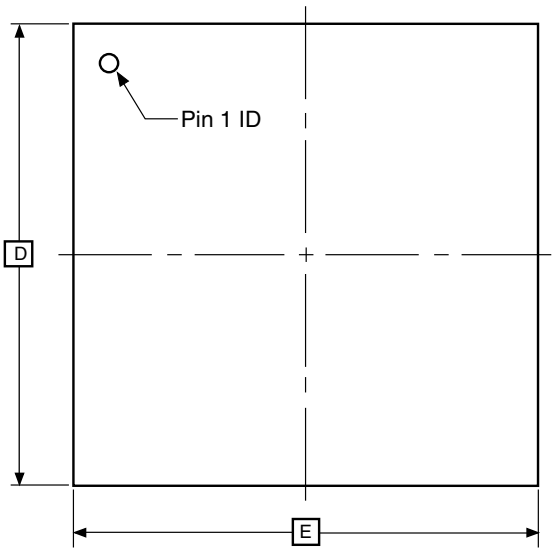
SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
b	0.18	0.25	0.30	
D	8.90	9.00	9.10	
D2	5.20	5.40	5.60	
E	8.90	9.00	9.10	
E2	5.20	5.40	5.60	
e	0.50 BSC			
L	0.35	0.40	0.45	
K	1.25	1.40	1.55	

Notes:
1. JEDEC Standard MO-220, (SAW Singulation) Fig. 1, VMMD.
2. Dimension and tolerance conform to ASMEY14.5M-1994.

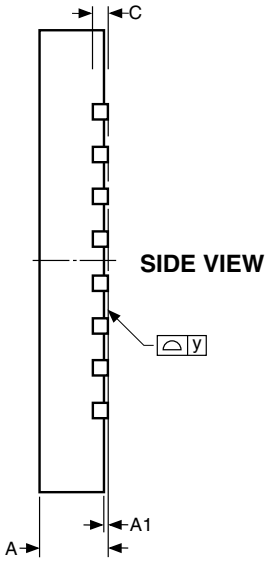
2010-10-19

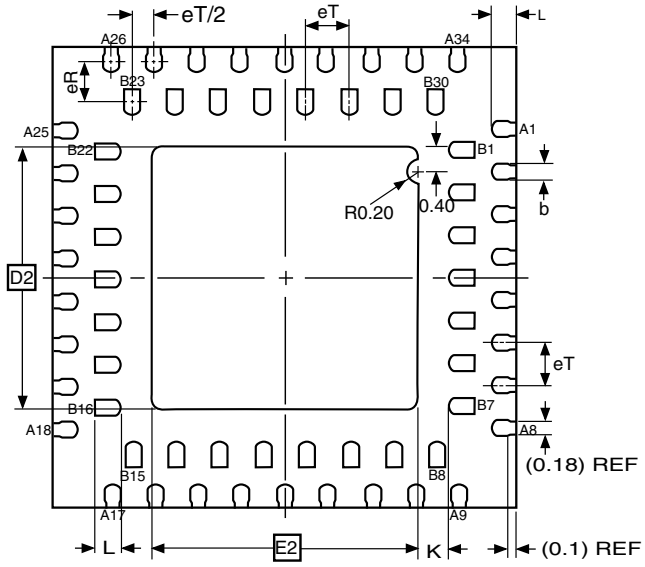
	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**64M1**, 64-pad, 9 x 9 x 1.0 mm Body, Lead Pitch 0.50 mm, 5.40 mm Exposed Pad, Micro Lead Frame Package (MLF)	64M1	H

8.3 64MC



TOP VIEW





BOTTOM VIEW

Note: 1. The terminal #1 ID is a Laser-marked Feature.

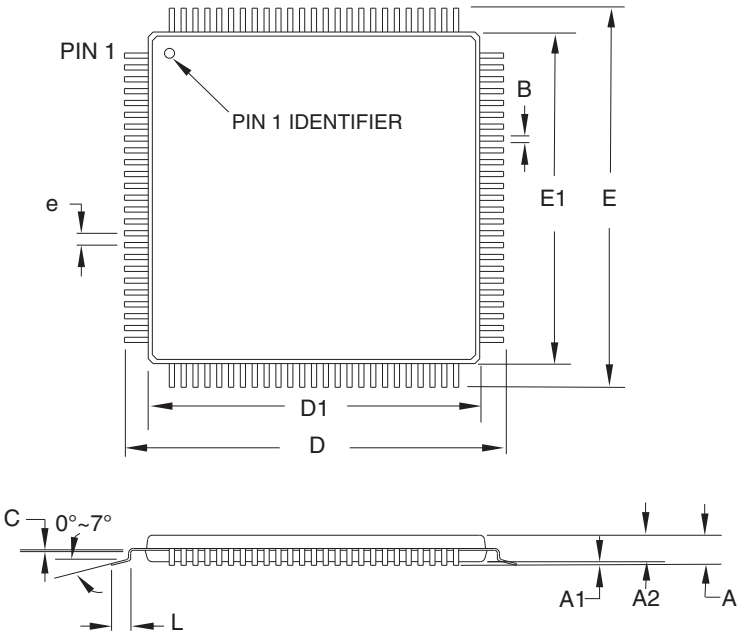
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	0.00	0.02	0.05	
b	0.18	0.23	0.28	
C		0.20 REF		
D	6.90	7.00	7.10	
D2	3.95	4.00	4.05	
E	6.90	7.00	7.10	
E2	3.95	4.00	4.05	
eT	–	0.65	–	
eR	–	0.65	–	
K	0.20	–	–	(REF)
L	0.35	0.40	0.45	
y	0.00	–	0.075	

10/3/07

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**64MC,** 64QFN (2-Row Staggered), 7 x 7 x 1.00 mm Body, 4.0 x 4.0 mm Exposed Pad, Quad Flat No Lead Package	ZXC	64MC	A

8.4 100A



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	15.75	16.00	16.25	
D1	13.90	14.00	14.10	Note 2
E	15.75	16.00	16.25	
E1	13.90	14.00	14.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation AED.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08mm maximum.

2010-10-20

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**100A,** 100-lead, 14 x 14mm Body Size, 1.0mm Body Thickness, 0.5mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP)	100A	D

9. Errata

9.1 Atmel ATmega169A

No known errata

9.2 Atmel ATmega169A/169PA Rev. A to F

Not sampled.

9.3 Atmel ATmega169PA Rev. G

No known errata.

9.4 Atmel ATmega329A/329PA rev. A

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **Using BOD disable will make the chip reset**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

2. **Using BOD disable will make the chip reset**

   If the part enters sleep with the BOD turned off with the BOD disable option

   enabled, a BOD reset will be generated at wakeup and the chip will reset.

   Problem Fix/Workaround

   Do not use BOD disable

9.5 Atmel ATmega329A/329PA rev. B

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

9.6 Atmel ATmega329A/329PA rev. C

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

9.7 Atmel ATmega3290A/3290PA rev. A

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**
- **Using BOD disable will make the chip reset**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

2. **Using BOD disable will make the chip reset**

   If the part enters sleep with the BOD turned off with the BOD disable option

   enabled, a BOD reset will be generated at wakeup and the chip will reset.

   Problem Fix/Workaround

   Do not use BOD disable

9.8 Atmel ATmega3290A/3290PA rev. B

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**

1. **Interrupts may be lost when writing the timer registers in the asynchronous timer**

   The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

   Problem Fix/ Workaround

   Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

9.9 Atmel ATmega3290A/3290PA rev. C

- **Interrupts may be lost when writing the timer registers in the asynchronous timer**

1. Interrupts may be lost when writing the timer registers in the asynchronous timer

The interrupt will be lost if a timer register that is synchronous timer clock is written when the asynchronous Timer/Counter register (TCNTx) is 0x00.

Problem Fix/ Workaround

Always check that the asynchronous Timer/Counter register neither have the value 0xFF nor 0x00 before writing to the asynchronous Timer Control Register (TCCRx), asynchronous Timer Counter Register (TCNTx), or asynchronous Output Compare Register (OCRx).

9.10 Atmel ATmega649A/649P/ATmega6490A/6490P

No known errata.

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Atmel Corporation
1600 Technology Drive
San Jose, CA 95110
USA
Tel: (+1) (408) 441-0311
Fax: (+1) (408) 487-2600
www.atmel.com

Atmel Asia Limited
Unit 01-5 & 16, 19F
BEA Tower, Millennium City 5
418 Kwun Tong Roa
Kwun Tong, Kowloon
HONG KONG
Tel: (+852) 2245-6100
Fax: (+852) 2722-1369

Atmel Munich GmbH
Business Campus
Parkring 4
D-85748 Garching b. Munich
GERMANY
Tel: (+49) 89-31970-0
Fax: (+49) 89-3194621

Atmel Japan G.K.
16F Shin-Osaki Kangyo Bldg
1-6-4 Osaki, Shinagawa-ku
Tokyo 141-0032
JAPAN
Tel: (+81) (3) 6417-0300
Fax: (+81) (3) 6417-0370