RAiO

RA8835A

Dot Matrix

LCD Controller

Specification

Version 1.0

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RAiO Technology Inc.

1. Overview

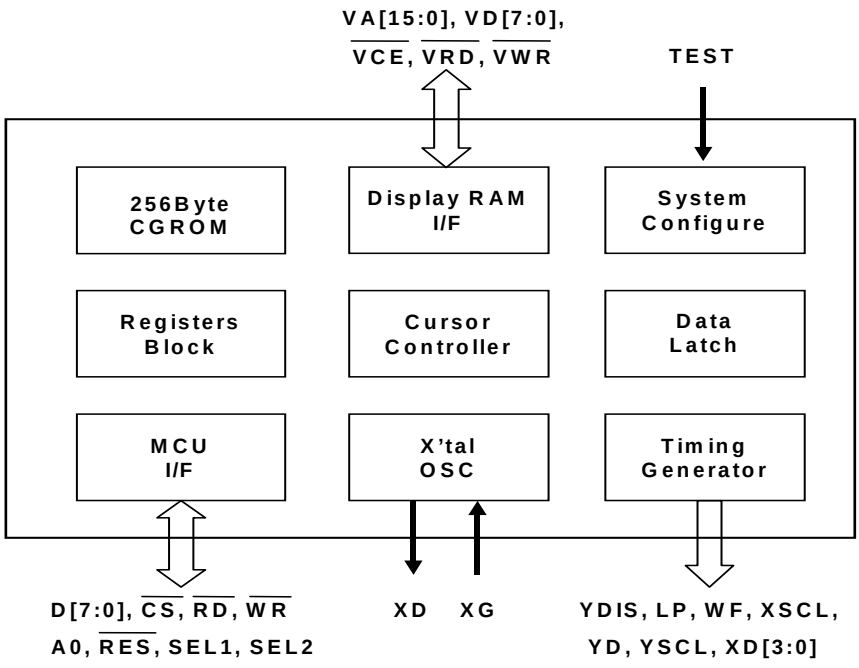
The RA8835A is a controller IC that can display text and graphics on LCD panel. It can display layered text and graphics, scroll the display in any direction and partition the display into multiple screens. It also stores text, character codes and bitmapped graphics data in external frame buffer memory. Display controller functions include transferring data from the controlling microprocessor to the buffer memory, reading memory data, converting data to display pixels and generating timing signals for the buffer memory, LCD panel.

The RA8835A has an internal character generator with 160, 5 X 7 pixel characters in internal mask ROM. The character generators support up to 64, 8 X 16 pixel characters in external character generator RAM and up to 256, 8 X 16 pixel characters in external character generator ROM.

2. Features

- Text, graphics and combined text/graphics display modes
- Three overlapping screens in graphics mode
- Up to 640 X 256 pixel LCD panel display resolution
- Programmable cursor control
- Smooth horizontal and vertical scrolling of all or part of the display
- 1/2-duty to 1/256-duty LCD drive
- Up to 640 X 256 pixel LCD panel display resolution memory
- 160, 5 X 7 pixel characters in internal mask-programmed character generator ROM
- Up to 64, 8 X 16 pixel characters in external character generator RAM
- Up to 256, 8 X 16 pixel characters in external character generator ROM
- 6800 and 8080 family microprocessor interfaces
- Low power consumption—3.5 mA operating current (V_{DD} = 3.5V), 0.05 μA standby current
- Package:
  RA8835AP3N: QFP-60 pin (Lead Free)
  RA8835AP4N: TQFP-60 pin (Lead Free)
- Power: 2.7 to 5.5 V

3. Block Diagram



4. Package

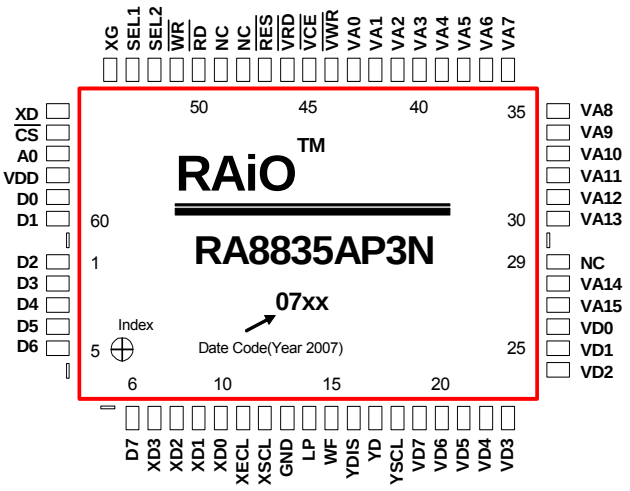


Figure 4-1: RA8835AP3N(QFP-60 Pin)

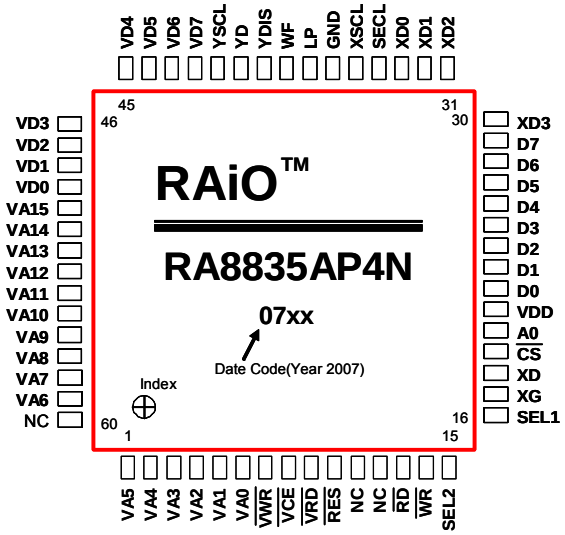


Figure 4-2: RA8835AP4N (TQFP-60 Pin)

5. Pin Descriptions

5.1.1. MCU Interface

Pin Name	Function
D0 to D7	**MCU Data Bus.** Tri-state input/output pins. Connect these pins to an 8- or 16-bit microprocessor bus.
SEL1, SEL2	**MCU Interface Select.** The RA8835A series supports both 8080 family processors (such as the 8085 and Z80®) and 6800 family processors (such as the 6802 and 6809). SEL1 should be tied directly to VDD or VSS to prevent noise. If noise does appear on SEL1, decouple it to ground using a capacitor placed as close to the pin as possible.
$\overline{RD}$ or E	**Read Control or Enable.** When the 8080 family interface is selected, this signal acts as the active-LOW read strobe. The RA8835A series output buffers are enabled when this signal is active. When the 6800 family interface is selected, this signal acts as the active-HIGH enable clock. Data is read from or written to the RA8835A series when this clock goes HIGH.

SEL1	SEL2*	Interface	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$
0	0	8080 family	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$
1	0	6800 family	A0	E	R/$\overline{W}$	$\overline{CS}$

<table>
<tr><td>$\overline{WR}$
or
R/$\overline{W}$</td><td>Write Control or Read/Write Control.
When the 8080 family interface is selected, this signal acts as the active-LOW write strobe. The bus data is latched on the rising edge of this signal.
When the 6800 family interface is selected, this signal acts as the read/write control signal. Data is read from the RA8835A series if this signal is HIGH, and written to the RA8835A series if it is LOW.</td></tr>
<tr><td>$\overline{CS}$</td><td>Chip Select.
This active-LOW input enables the RA8835A series. It is usually connected to the output of an address decoder device that maps the RA8835A series into the memory space of the controlling microprocessor.</td></tr>
<tr><td>A0</td><td>Command/Data Select.
8080 Family Interface:
<table>
<tr><th>A0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>Function</th></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Status flag read</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Display data and cursor address read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Display data and parameter write</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Command write</td></tr>
</table>
6800 Family Interface:
<table>
<tr><th>A0</th><th>R/$\overline{W}$</th><th>E</th><th>Function</th></tr>
<tr><td>0</td><td>1</td><td>1</td><td>Status flag read</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Display data and cursor address read</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Display data and parameter write</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Command write</td></tr>
</table></td></tr>
<tr><td>$\overline{RES}$</td><td>Hardware Reset.
This active-LOW input performs a hardware reset on the RA8835A series. It is an Schmitt-trigger input for enhanced noise immunity; however, care should be taken to ensure that it is not triggered if the supply voltage is lowered.</td></tr>
</table>

5.1.2 Display Memory Control

The RA8835A series can directly access static RAM and PROM. The designer may use a mixture of these two types of memory to achieve an optimum trade-off between low cost and low power consumption.

Pin Name	Function
VA0 to VA15	**16-bit Display Memory Address.** When accessing character generator RAM or ROM, VA0 to VA3, reflect the lower 4 bits of the RA8835A row counter.
VD0 to VD7	**Display Memory Data Bus.** 8-bit tri-state display memory data bus. These pins are enabled when $\overline{VRD}$ or $\overline{VWR}$ is LOW.
$\overline{VWR}$	**Display Memory Write Control.** Active-LOW display memory write control output.
$\overline{VRD}$	**Display Memory Read Control.** Active-LOW display memory read control output.

$\overline{VCE}$	**Display Memory Chip Select.** Active-LOW static memory standby control signal. $\overline{VCE}$ can be used with $\overline{CS}$.

5.1.3 LCD Drive Signals

In order to provide effective low-power drive for LCD matrixes, the RA8835A series can directly control both the X- and Y-drivers using an enable chain.

Pin Name	Function
XD0 to XD3	**Data Output for Driver.** 4-bit X-driver (column drive) data outputs. Connect these outputs to the inputs of the X-driver chips.
XSCL	**Latch Clock.** The falling edge of XSCL latches the data on XD0 to XD3 into the input shift registers of the X-drivers. To conserve power, this clock halts between LP and the start of the following display line (See section 6.3.7).
XECL	**Trigger Clock for Chain Cascade.** The falling edge of XECL triggers the enable chain cascade for the X-drivers. Every 16th clock pulse is output to the next X-driver.
LP	**Latch Pulse.** LP latches the signal in the X-driver shift registers into the output data latches. LP is a falling-edge triggered signal, and pulses once every display line. Connect LP to the Y-driver shift clock on modules.
WF	**AC Drive Output.** The WF period is selected to be one of two values with SYSTEM SET command.
YSCL	**Latch Clock for YD.** The falling edge of YSCL latches the data on YD into the input shift registers of the Y-drivers. YSCL is not used with driver ICs which use LP as the Y-driver shift clock.
YD	**Data Pulse Output for Y Drivers.** It is active during the last line of each frame, and is shifted through the Y drivers one by one (by YSCL), to scan the display's common connections.
YDIS	**Power-down Output Signal.** YDIS is HIGH while the display drive outputs are active. YDIS goes LOW one or two frames after the sleep command is written to the RA8835A series. All Y-driver outputs are forced to an intermediate level (de-selecting the display segments) to blank the display. In order to implement power-down operation in the LCD unit, the LCD power drive supplies must also be disabled when the display is disabled by YDIS.

5.1.4. Oscillator and Power

Pin Name	Function
XG	**Crystal Connection for Internal Oscillator** This pin can be driven by an external clock source that satisfies the timing specifications of the EXT f0 signal (See section 7.3.6).
XD	**Crystal Connection for Internal Oscillator** Leave this pin open when using an external clock source.
VDD	**2.7 to 5.5V Supply.** This may be the same supply as the controlling microprocessor.

GND	**Ground**
TEST	**Test Pin.** This is a test pins. No need for connection(NC).

Note: The peak supply current drawn by the RA8835A series may be up to ten times the average supply current. The power supply impedance must be kept as low as possible by ensuring that supply lines are sufficiently wide and by placing 0.47μF decoupling capacitors that have good high-frequency response near the device's supply pins.

6. System Application