

10V Drive Nch MOSFET

R5009FNX

● Structure

Silicon N-channel MOSFET

● Features

- 1) Fast reverse recovery time (t_{rr})
- 2) Low on-resistance.
- 3) Fast switching speed.
- 4) Gate-source voltage
 V_{GSS} guaranteed to be $\pm 30V$.
- 5) Drive circuits can be simple.
- 6) Parallel use is easy.

● Application

Switching

● Packaging specifications

Type	Package	Bulk
		Basic ordering unit (pieces)
R5009FNX		○

● Absolute maximum ratings (Ta = 25°C)

Parameter	Symbol	Limits	Unit	
Drain-source voltage	V_{DSS}	500	V	
Gate-source voltage	V_{GSS}	± 30	V	
Drain current	Continuous	I_D *3	± 9	A
	Pulsed	I_{DP} *1	± 36	A
Source current (Body Diode)	Continuous	I_S *3	9	A
	Pulsed	I_{SP} *1	36	A
Avalanche Current	I_{AS} *2	4.5	A	
Avalanche Energy	E_{AS} *2	5.4	mJ	
Power dissipation (Tc=25°C)	P_D	50	W	
Channel temperature	Tch	150	°C	
Range of storage temperature	Tstg	-55 to +150	°C	

*1 $P_w \leq 10 \mu s$, Duty cycle $\leq 1\%$

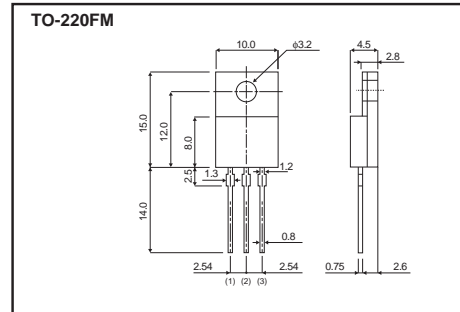
*2 $L = 500 \mu H$, $V_{DD} = 50V$, $R_g = 25 \Omega$, starting Tch = 25°C

*3 Limited only by maximum temperature allowed.

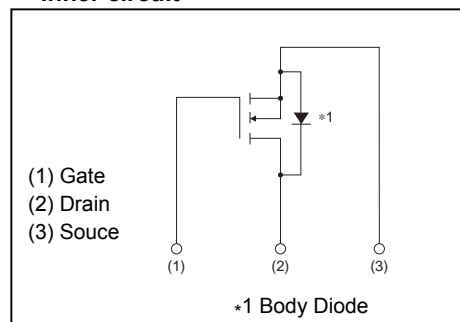
● Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to Case	$R_{th}(ch-c)$	2.5	°C / W

● Dimensions (Unit : mm)



● Inner circuit



● Electrical characteristics (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 30V, V_{DS}=0V$
Drain-source breakdown voltage	$V_{(BR)DSS}$	500	-	-	V	$I_D=1mA, V_{GS}=0V$
Zero gate voltage drain current	I_{DSS}	-	-	100	μA	$V_{DS}=500V, V_{GS}=0V$
Gate threshold voltage	$V_{GS(th)}$	2.0	-	4.0	V	$V_{DS}=10V, I_D=1mA$
Static drain-source on-state resistance	$R_{DS(on)}^*$	-	0.65	0.84	Ω	$I_D=4.5A, V_{GS}=10V$
Forward transfer admittance	$ Y_{fs} ^*$	4.0	5.7	-	S	$I_D=4.5A, V_{DS}=10V$
Input capacitance	C_{iss}	-	630	-	pF	$V_{DS}=25V$
Output capacitance	C_{oss}	-	400	-	pF	$V_{GS}=0V$
Reverse transfer capacitance	C_{rss}	-	25	-	pF	$f=1MHz$
Turn-on delay time	$t_{d(on)}^*$	-	24	-	ns	$I_D=4.5A, V_{DD}=250V$
Rise time	t_r^*	-	20	-	ns	$V_{GS}=10V$
Turn-off delay time	$t_{d(off)}^*$	-	50	-	ns	$R_L=55.6\Omega$
Fall time	t_f^*	-	40	-	ns	$R_G=10\Omega$
Total gate charge	Q_g^*	-	18	-	nC	$I_D=9.0A, V_{DD}=250V$
Gate-source charge	Q_{gs}^*	-	3.5	-	nC	$V_{GS}=10V$
Gate-drain charge	Q_{gd}^*	-	5.5	-	nC	

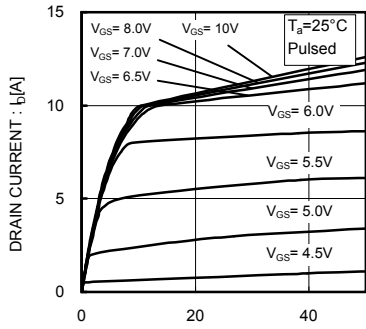
*Pulsed

● Body diode characteristics (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}^*	-	-	1.5	V	$I_s=9.0A, V_{GS}=0V$
Reverse Recovery Time	t_{rr}^*	48	78	108	ns	$I_s=9.0A, di/dt=100A/\mu s$

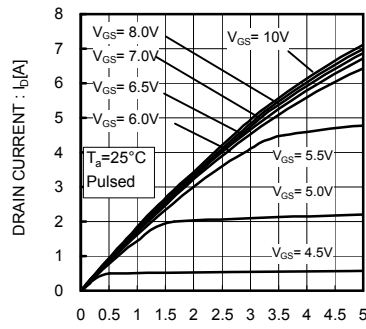
*Pulsed

●Electrical characteristics curves



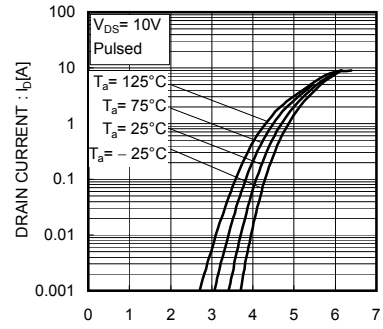
DRAIN-SOURCE VOLTAGE : V_{DS}[V]

Fig.1 Typical Output Characteristics (I)



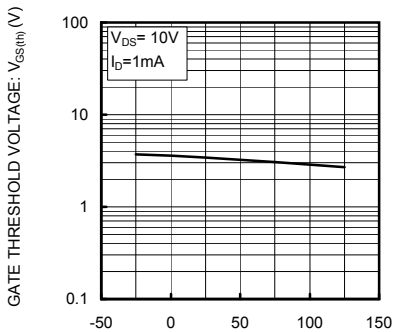
DRAIN-SOURCE VOLTAGE : V_{DS}[V]

Fig.2 Typical Output Characteristics (II)



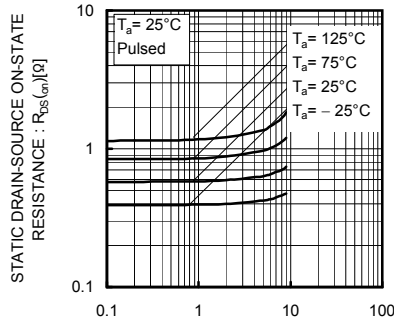
GATE-SOURCE VOLTAGE : V_{GS}[V]

Fig.3 Typical Transfer Characteristics



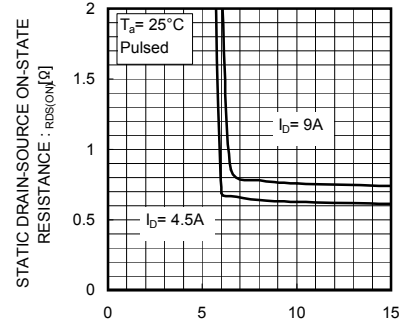
CHANNEL TEMPERATURE: T_{ch} (°C)

Fig.4 Gate Threshold Voltage vs. Channel Temperature



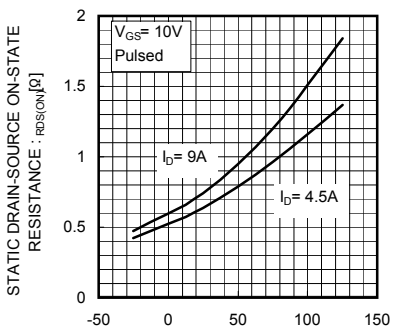
DRAIN-CURRENT : I_D[A]

Fig.5 Static Drain-Source On-State Resistance vs. Drain Current



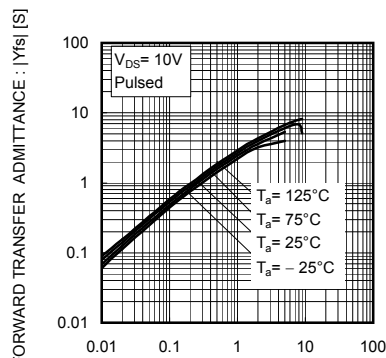
GATE-SOURCE VOLTAGE : V_{GS} (V)

Fig.6 Static Drain-Source On-State Resistance vs. Gate Source Voltage



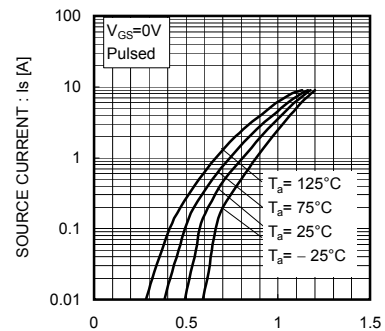
CHANNEL TEMPERATURE: T_{ch} (°C)

Fig.7 Static Drain-Source On-State Resistance vs. Channel Temperature



DRAIN-CURRENT : I_D[A]

Fig.8 Forward Transfer Admittance vs. Drain Current



SOURCE-DRAIN VOLTAGE : V_{SD} [V]

Fig.9 Reverse Drain Current vs. Source-Drain Voltage

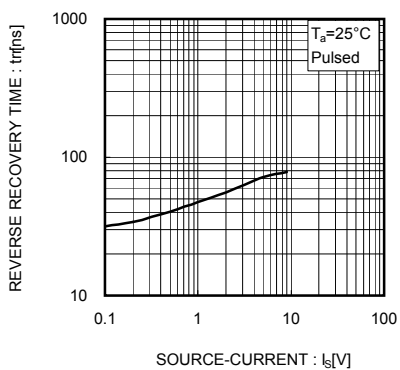


Fig. 10 Reverse Recovery Time vs. Source Current

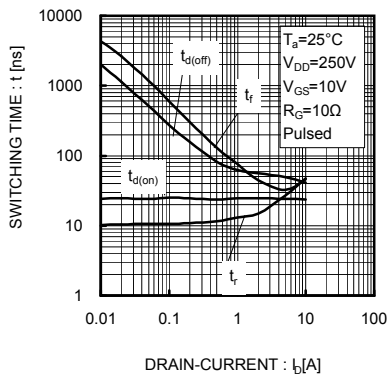


Fig. 11 Switching Characteristics

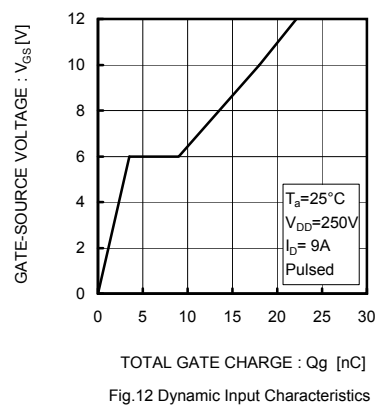


Fig. 12 Dynamic Input Characteristics

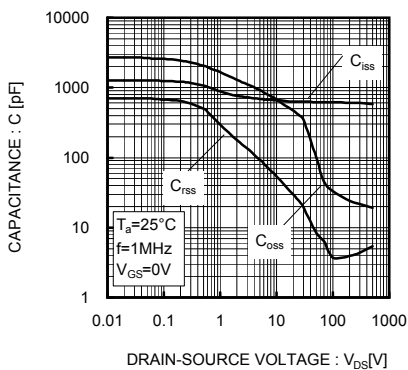


Fig. 13 Typical Capacitance vs. Drain-Source Voltage

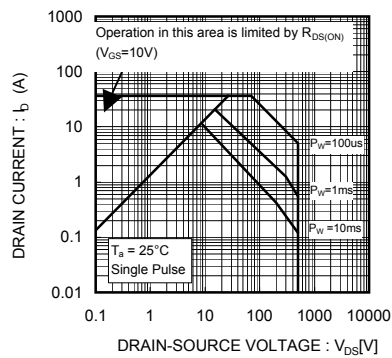


Fig. 14 Maximum Safe Operating Area

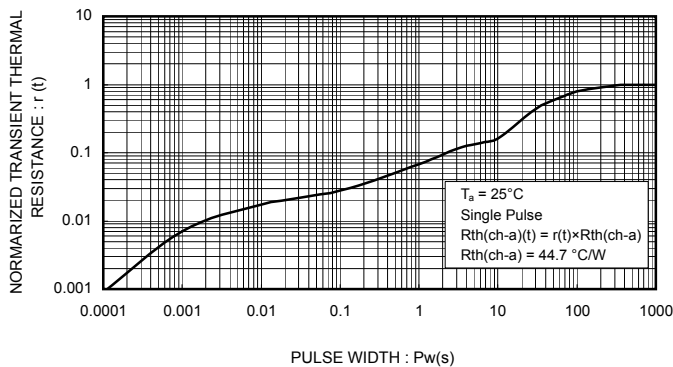


Fig. 15 Normalized Transient Thermal Resistance vs. Pulse Width

● Measurement circuits

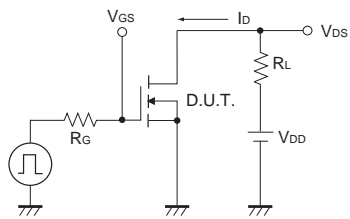


Fig.1-1 Switching Time Measurement Circuit

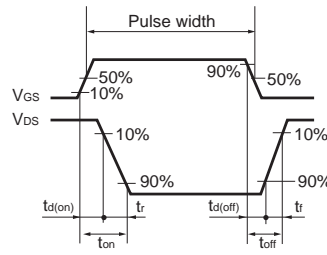


Fig.1-2 Switching Waveforms

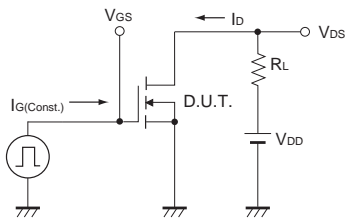


Fig.2-1 Gate Charge Measurement Circuit

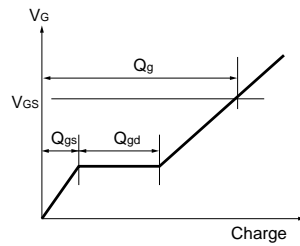


Fig.2-2 Gate Charge Waveform

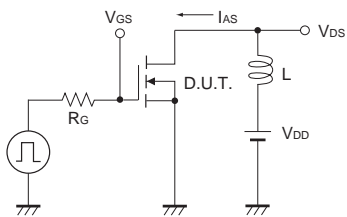


Fig.3-1 Avalanche Measurement Circuit

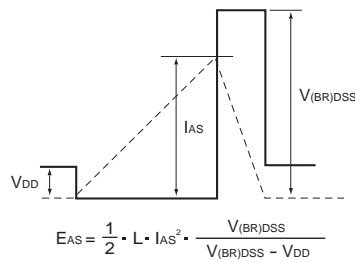


Fig.3-2 Avalanche Waveform

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