MC145414

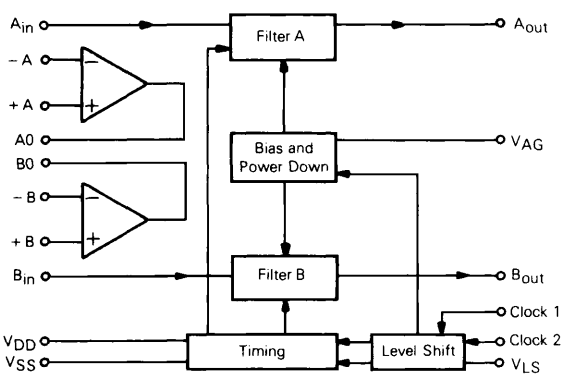
2

DUAL TUNABLE LOW PASS SAMPLED DATA FILTERS

The MC145414 is sampled data, switched capacitor filter IC intended to provide band limiting and signal restoration filtering. It is capable of operating from either a single or split power supply and can be powered-down when not in use. Included on the IC are two totally uncommitted op amps for use elsewhere in the system as I to V converters, gain adjust buffers, etc.

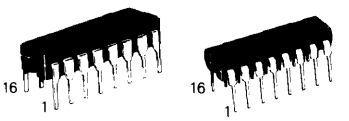
- Two General Purpose 5th Order Elliptic Low Pass Filters
- Low Operating Power Consumption — 30 mW (Typical)
- Power Down Capability — 1 mW (Maximum)
- ±5 to ±8 Volt Power Supply Ranges
- TTL or CMOS Compatible Inputs Using VLS Pin
- Two Operational Amplifiers Available to Reduce Component Count
- Useful in LPC or CVSD Speech Applications
- Passband Edges Tunable With Clock Frequency From 1.25 kHz to 10 kHz

BLOCK DIAGRAM



CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

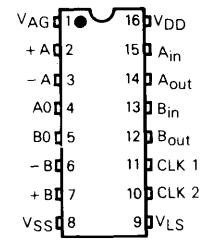
DUAL TUNABLE
LOW PASS
SAMPLED DATA FILTERS



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

PIN ASSIGNMENT



ORDERING INFORMATION

MC14XXXX
- L Ceramic Package
- P Plastic Package

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}-V_{SS}	−0.5 to 18	V
Input Voltage, All Pins	V_{in}	−0.5 to V_{DD} +0.5	V
DC Current Drain per Pin (Excluding V_{DD}, V_{SS})	I	10	mA
Operating Temperature Range	T_A	0 to 85	°C
Storage Temperature Range	T_{stg}	−65 to 150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}-V_{SS}	10	12	16	V
Clock 1, 2 Frequency	CLK 1, 2	50	128	400	kHz

DIGITAL ELECTRICAL CHARACTERISTICS (V_{SS} = 0 V)

Characteristic		Symbol	V_{DD} Vdc	25°C Min	25°C Typ	25°C Max	Unit
Operating Current		I_{DD}	12	–	2.0	4.0	mA
Power-Down Current (PDI = V_{SS})		I_{PD}	12	–	10	40	μA
Input Capacitance		C_{in}	12	–	5.0	–	pF
MODE CONTROL LOGIC LEVELS							
VLS Power-Down Mode		V_{IH}	12 15	11.5 14.5	11 13	– –	V
VLS TTL Mode		–	12 15	4.0 5.0	– –	8 9	V
VLS CMOS Mode		V_{IL}	12 15	– –	– –	0.8 0.8	V
VAG Power-Down Mode		V_{IH}	12 15	11.5 14.5	10.5 13.5	– –	V
VAG Analog-Ground Mode		V_{IL}	12 15	– –	– –	7.0 9.0	V
CMOS LOGIC LEVELS (V_{LS} = V_{SS})							
Input Current Clock 1, 2 (Internal Pulldown Resistors)	"1" Level "0" Level	I_{in}	12 12	– –	50 −0.00001	100 −0.3	μA
Input Voltage Clock 1, 2	"0" Level	V_{IL}	12 15	– –	5.25 6.75	3.0 3.5	V
	"1" Level	V_{IH}	12 15	9.0 11.5	6.75 8.25	–	V
TTL LOGIC LEVELS (VLS = 6 V, V_{SS} = 0 V)							
Input Current Clock 1, 2 (Internal Pulldown Resistor)	"1" Level "0" Level	I_{in}	12 12	– –	50 –	100 100	μA
Input Voltage Clock 1, 2	"0" Level "1" Level	V_{IL} V_{IH}	12 12	– V_{LS} + 2.0	– –	VLS + 0.8 –	V

2

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V)

Characteristic		Symbol	25°C Min	25°C Typ	25°C Max	Unit
Input Current	A_{in}, B_{in}	I_{in}	–	±0.00001	±1.0	μA
Input Current	VAG	I_{in}	–	±0.00001	±10	μA
AC Input Impedance (1 kHz)	A_{in}, B_{in}	Z_{in}	–	2	–	MΩ
Input Common Mode Voltage Range	A_{in}, B_{in}, +A, −A, +B, −B	V_{ICR}	2.0	–	10.0	V
Input Offset Current	+A to −A, +B to −B	I_{ID}	–	±10	–	nA
Input Bias Current	+A, −A, +B, −B	I_{IB}	–	±0.10	±200	nA
Input Offset Voltage	+A to −A, +B to −B	V_{ID}	–	±10	±70	mV
Output Voltage Range (R_L = 20 kΩ to VAG, R_B = ∞) (R_L = 600 Ω to VAG, R_B = 1.6 kΩ to V_{DD}) (R_L = 900 Ω to VAG, R_B = 1.8 kΩ to V_{DD})	A0, B0, A_{out}, B_{out}	V_{OR}	 1.5 3.0 2.5	 – – –	 10.5 8.3 9.0	V
Small Signal Output Impedance (1 kHz)	A_{out} B_{out}	Z_O	– –	50 50	– –	Ω
Output Current (V_O = 10.5 V) (V_O = 1.5 V)	 A_{out}, B_{out}, A0, B0 A_{out}, B_{out}, A0, B0	 I_{OH} I_{OL}	 −200 5	 −400 7.5	 – –	 μA mA
Unity Gain Output Noise	A0, B0	–	–	15	–	μVrms

FILTER A SPECIFICATIONS

($V_{DD} - V_{SS}$ = 12 V, Clock 1, 2 = 128 kHz, V_{in} = −28 dBm0, full scale = +3 dBm0, 7 V p-p)

Characteristic		25°C Min	25°C Typ	25°C Max	Unit
Gain (1020 Hz)		17.4	18	18.6	dB
Passband Ripple (50 Hz to 3000 Hz)		–	0.24	1.0	dB
Out of Band Response 3400 Hz 4000 Hz-4600 Hz 4600 Hz-64 kHz		 – −10 −25	 −0.8 −15.5 −33.0	 −1.5 – –	dB
Output Noise (A_{in} = VAG)	ref to 900 Ω	–	10	17	dBrnc0
Dynamic Range		76	83	–	dB
Differential Group Delay 1150 to 2300 Hz Delay 1000 to 2500 Hz Delay 800 to 2700 Hz Delay		 – – –	 – – –	 – – –	μs
Power Supply Rejection Ratio (V_{DD} = 12 V +0.1 V_{RMS} @ 1 kHz)		–	36	–	dB
Crosstalk (A_{in} = VAG, B_{in} = 0 dBm0 Output at A_{out} at 3 kHz)		–	76	–	dB

FILTER B SPECIFICATIONS ($V_{DD} - V_{SS}$ = 12 V, Clock 1, 2 = 128 kHz, V_{in} = −10 dBm0, full scale = +3 dBm0, 7 V p-p)

Characteristic	25°C Min	25°C Typ	25°C Max	Unit
Gain (1020 Hz)	−0.7	±0.15	+0.7	dB
Passband Ripple (300 Hz to 3000 Hz)	–	0.22	1.0	dB
Response 3400 Hz 4000 Hz-4600 Hz 4600 Hz-64 kHz	 – −10 −28	 −0.8 −15.5 −33.0	 −1.7 – –	dB
Output Noise (300 Hz-3400 Hz)	–	8	14	dBrnc0
Dynamic Range (7 V p-p Max)	79	87	–	dB
Differential Group Delay 1150 to 2300 Hz Delay 1000 to 2500 Hz Delay 800 to 2700 Hz Delay	 – – –	 – – –	 – – –	μs
Crosstalk (B_{in} = VAG, A_{in} = OdBm0 @ 3 kHz Output at B_{out} @ 3 kHz)	–	76	–	dB
Power Supply Rejection Ratio	–	36	–	dB

SWITCHING CHARACTERISTICS ($V_{DD} - V_{SS} = 10$ V, $T_A = 25°C$)

Characteristics		Symbol	0 to 70°C			Units
			Min	Typ	Max	
Input Rise Time Input Fall Time	Clock 1, 2	t_{TLH} t_{THL}	–	–	4	μs
Pulse Width	Clock 1, 2	t_{WH}	200	–	–	ns
Clock Pulse Frequency	Clock 1, 2	f_{CL}	50	–	400	kHz
Clock 1, 2 Duty Cycle		–	40	–	60	%

2

FUNCTIONAL DESCRIPTION OF PINS

Pin 1 — V_{AG} (Analog Ground)
This pin should be held at approximately (V_{DD}-V_{EE})/2. All analog inputs and outputs are referenced to this pin. If this pin is brought to within approximately 1.0 V of V_{DD}, the chip will be powered down.

Pin 2 — +A
Non-inverting input of op-amp A.

Pin 3 — −A
Inverting input of op-amp A.

Pin 4 — A0
Output of uncommitted op-amp A.

Pin 5 — B0
Output of uncommitted op-amp B.

Pin 6 — −B
Inverting input of op-amp B.

Pin 7 — +B
Non-inverting input of op-amp B.

Pin 8 — V_{SS}
This is the most negative supply pin and digital ground for the package.

Pin 9 — V_{LS} (Logic Shift Voltage)
The voltage on this pin determines the logic compatibility for the Clock 1, 2 inputs. If V_{LS} is within 0.8 V of V_{SS}, the thresholds will be for CMOS operating between V_{DD} and V_{SS}. If VLS is within 1.0 V of V_{DD}, the chip will power down. If V_{LS} is between $V_{DD} - 2$ V and $V_{SS} + 2$ V, the thresholds for logic inputs at Clock 1, 2 will be between $V_{LS} + 0.8$ V and $V_{LS} + 2.0$ V for TTL compatibility.

Pin 10 — Clock 1
Always tie clock 1 and clock 2 together.

Pin 11 — Clock 2
Always tie clock 1 and clock 2 together.

Pin 12 — B_{out} (Lowpass Filter B)
This is the output of B lowpass filter.

Pin 13 — B_{in} (Lowpass Filter B)
This is the input to filter B.

Pin 14 — A_{out} (Low pass Filter A)
This pin is the output to filter A.

Pin 15 — A_{in} (Lowpass Filter A)
This is the input to filter A.

Pin 16 — V_{DD}
Nominally 12 volts.

NOTE: Both VAG and VLS are high-impedance inputs.

FILTER DESCRIPTION

FILTER A DESCRIPTION

Filter A of the MC145414 is a 5-pole elliptic tunable lowpass filter operating at a sampling rate determined by clock 1 and clock 2. This filter provides band limiting that is a direct function of clock 1 and clock 2. With a 128 kHz clock, the band limiting frequency is 3.6 kHz. By dividing the clock in half to 64 kHz, the band limiting frequency is cut in half to 1.8 kHz (as illustrated in Figure 1). Likewise by doubling the clock, the cutoff point will double (as illustrated in Figures 3 and 4). The clock frequency can be varied from 50 kHz to 400 kHz. Filter A, unlike filter B, has a gain of 18 db. Because the MC145414 is a switch capacitance filter, the sampled output signal will have switching noise present near multiples of the switching frequency; a single-pole RC filter may be required to reduce this.

To provide 50/60 Hz and 15 Hz rejection, a 3-pole Chebychev highpass filter can be externally realized with the MC145414 by using the uncommitted op-amps as an active filter. This is shown in Figure 5 and 6.

FILTER B DESCRIPTION

Filter B in the MC145414 consists of a 5-pole elliptic tunable lowpass filter operating at a sampled rate determined by clock 1 and clock 2. Filter B is functionally similar to filter A, except filter B has unity gain.

Clock 1 and 2

Logic levels of these signals can be either TTL or CMOS compatible. Choice of logic level can be user determined by applying the appropriate voltage to the level shift control pin, VLS. Clock 1, 2 pins should be tied together.

Power Down

The MC145414 may be powered down by bringing VAG to within 1.7 V of V_{CC} or by bringing VLS to within 1.7 V of V_{DD}

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FIGURE 1 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 64 kHz

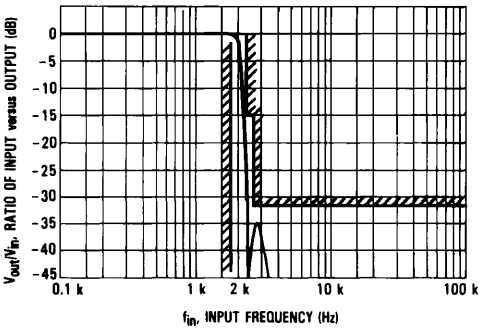


FIGURE 2 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 128 kHz

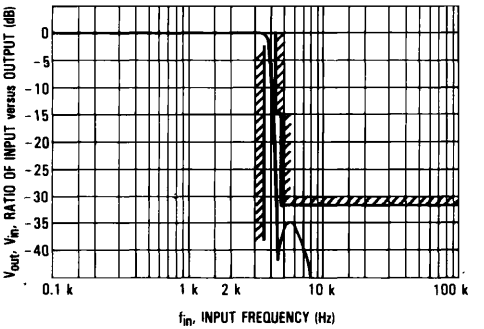


FIGURE 3 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 256 kHz

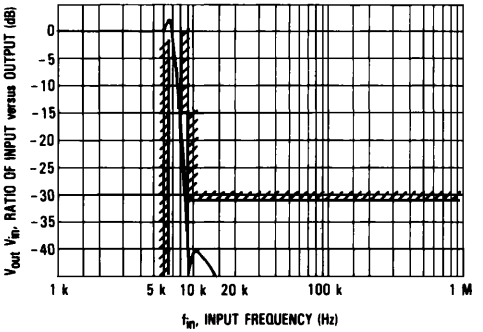


FIGURE 4 — FILTER A AND B LOWPASS CHARACTERISTICS WITH CLOCK 1 AND 2 AT 400 kHz

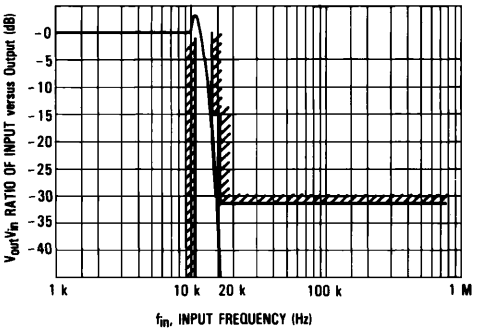
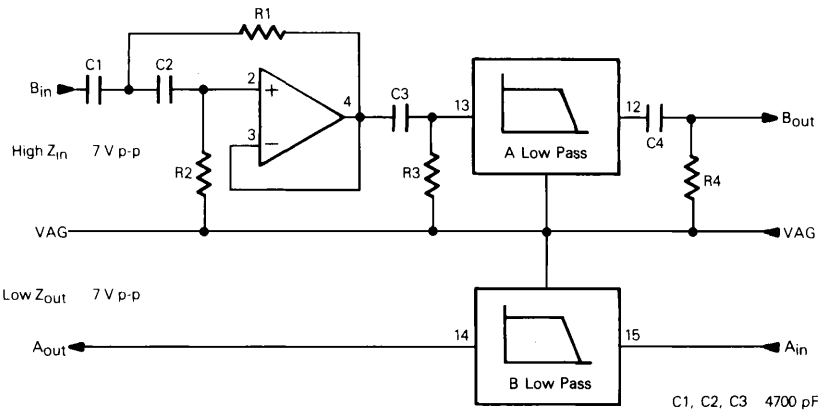


FIGURE 5 — FILTER SCHEMATIC FOR MC145414 WITH 60 Hz REJECT FILTER



C1, C2, C3	4700 pF	± 1%
C4	0.2 μF	− 20% + 80%
R1	112 kΩ ¼ W	1%
R2	620 kΩ ¼ W	1%
R3	223 kΩ ¼ W	1%
R4	100 kΩ ¼ W	10%

NOTE: In noisy environment, R1-R4 should be 10 kΩ or less to minimize pickup.

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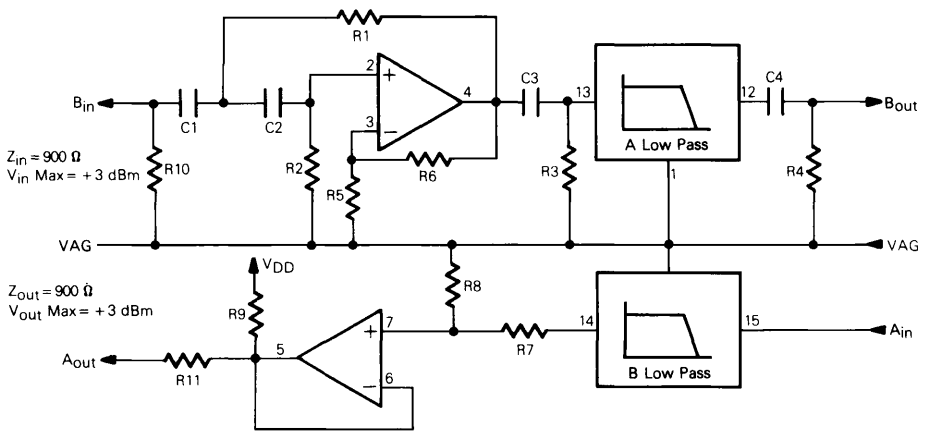
FIGURE 6 — FILTER SCHEMATIC FOR MC145414 WITH 60 Hz REJECTION AND 900 TERMINATION



C1, C2, C3	4700 pF	± 1%	R6	169 kΩ ¼ W	1%
C4	0.2 μF	− 20% + 80%	R7	24 kΩ ¼ W	1%
R1	236 kΩ ¼ W	1%	R8	33 kΩ ¼ W	1%
R2	294 kΩ ¼ W	1%	R9	1.8 kΩ ¼ W	10%
R3	223 kΩ ¼ W	1%	R10	900 Ω ¼ W	1%
R4	100 kΩ ¼ W	10%	R11	900 Ω ¼ W	1%
R5	200 kΩ ¼ W	1%			

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NOTE: In noisy environment, R1-R4 should be 10 kΩ or less to minimize pickup.

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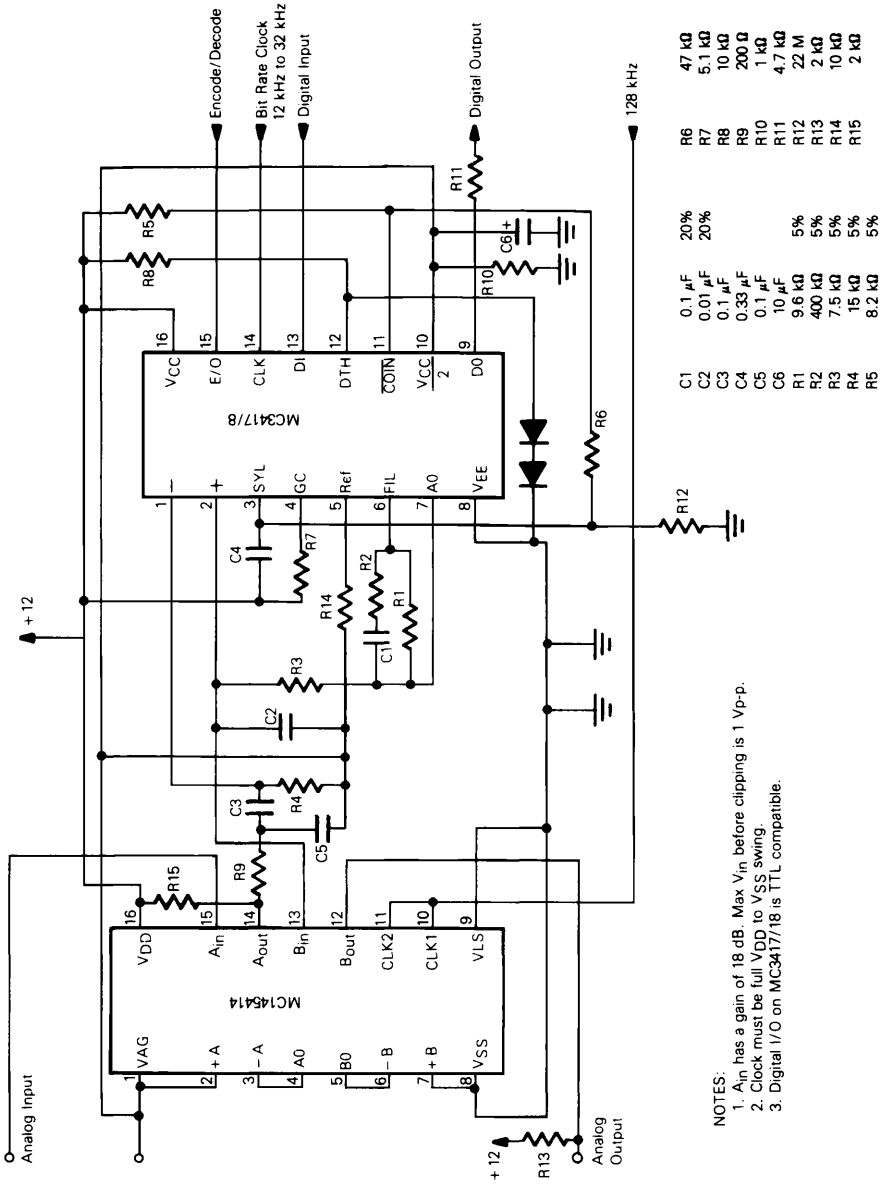

NOTES:
1. A_{in} has a gain of 18 dB. Max V_{in} before clipping is 1 Vp-p.
2. Clock must be full V_{DD} to V_{SS} swing.
3. Digital I/O on MC3417/18 is TTL compatible.

FIGURE 7 – DELTAMOD VOICE DIGITIZER USING MC3417 AND MC145414