FAIRCHILD SEMICONDUCTOR®

May 2012

FAN6863W
Highly Integrated Green-Mode PWM Controller

Features

- Low Standby Power: Under 0.1W
- Low Startup Current: 8μA
- Low Operating Current in Green Mode: 600μA
- Peak-Current Mode Operation with Cycle-by-Cycle Current Limiting
- PWM Frequency Continuously Decreasing with Burst Mode at Light Loads
- V_{DD} Over-Voltage Protection (OVP)
- Constant Output Power Limit (Full AC Input Range)
- Internal Latch Circuit (FAN6863WL) for OVP, OTP
- SENSE Pin Short-Circuit Protection (SSCP)
- Fixed PWM Frequency (65KHz) with Frequency Hopping
- Feedback Open-Loop Protection: 60ms Delay
- GATE Output Maximum Voltage Clamp: 13.5V
- Soft-Start Time: 5ms
- Soft Driving for EMI Improvement
- Full Range Frequency Hopping
- Internal OTP Sensor with Hysteresis
- Gate Driving Capability: 400mA

Applications

General-purpose switched-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-Frame SMPS
- SMPS with Surge-Current Output, such as for Printers, Scanners, Motor Drivers

Description

A highly integrated PWM controller, FAN6863W provides several features to enhance the performance of flyback converters. To minimize standby power consumption, a proprietary Green Mode provides off-time modulation to continuously decrease the switching frequency under light-load conditions. Under zero-load conditions, the power supply enters Burst Mode, which completely shuts off PWM output. Output restarts just before the supply voltage drops below the UVLO lower limit. Green Mode enables power supplies to meet international power conservation requirements.

The FAN6863W is designed for SMPS and integrates a frequency-hopping function that helps to reduce EMI emission of a power supply with minimum line filters. To compensate the power limit variation over universal input range, a current limit (V_{LIMIT}) adaptively keeps the power limit substantially constant. The gate output is clamped at 13.5V to protect the external MOSFET from over-voltage damage.

Other protection functions include SENSE pin Short-Circuit Protection (SSCP), V_{DD} Over-Voltage Protection (OVP), and Over-Temperature Protection (OTP). For OTP, an external NTC thermistor can be applied to sense the ambient temperature. When V_{DD} OVP or OTP is activated, an internal latch circuit latches off the controller. Protection types are shown in Table 1.

Table 1. Protection Type

Part Number	OVP	OLP	OTP / OTP2	SSCP
FAN6863W	Latch	A/R	Latch	A/R
FAN6863WL	Latch	Latch	Latch	A/R
FAN6863WR	A/R	A/R	A/R	A/R

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAN6863WTY	-40 to +105°C	6-Lead, SuperSOT™-6, JEDEC M0-193, 1.6mm Wide	Tape & Reel
FAN6863WLTY			
FAN6863WRTY			

Typical Application

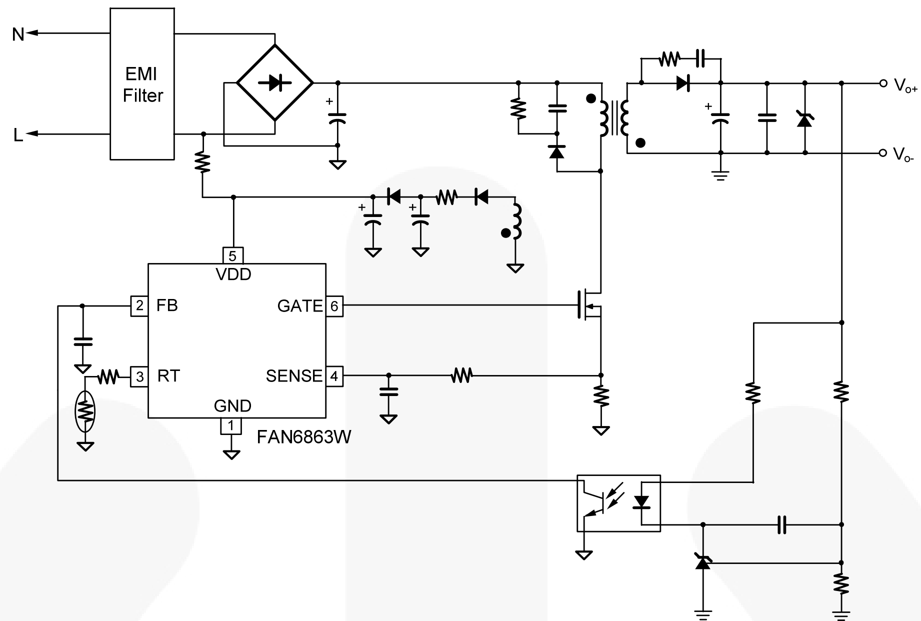


Figure 1. Typical Application

Block Diagram

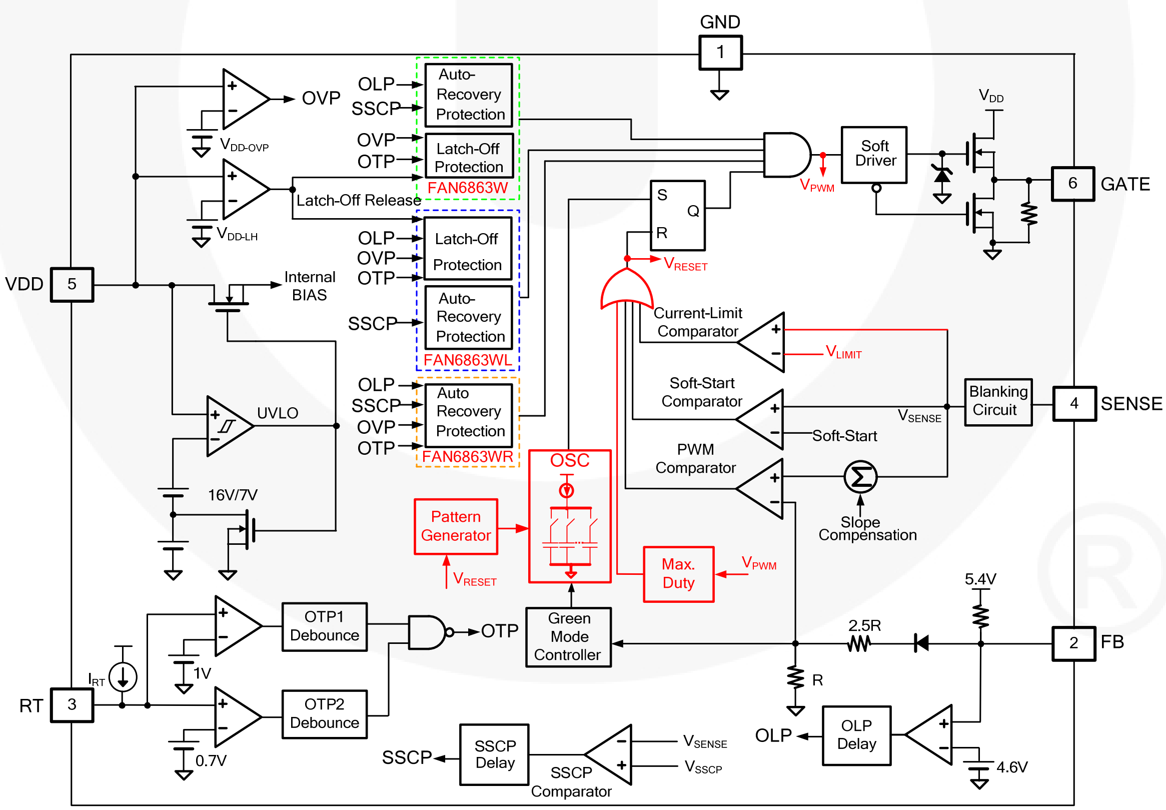
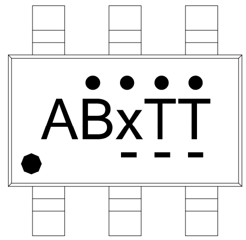


Figure 2. Block Diagram

Marking Information



ABx:	ABU: FAN6863WTY
	ABV: FAN6863WRTY
	ABW: FAN6863WLTY
TT:	Wafer Lot Code
●●●●:	Year Code
_ _ _:	Week Code

Figure 3. Top Mark

Pin Configuration

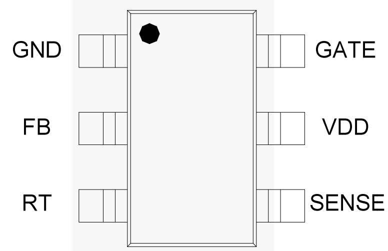


Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Function	Description
1	GND	Ground	Ground
2	FB	Feedback	The FB pin provides the output voltage regulation signal. It provides feedback to the internal PWM comparator, so the PWM comparator can control the duty cycle. This pin also provides over-current protection. IF V_{FB} is higher than the trigger level and persists at that level, the controller stops and restarts.
3	RT	Temperature Detection	An external NTC thermistor is connected from this pin to the GND pin. The impedance of the NTC decreases at high temperatures. If the voltage of the RT pin drops below the threshold, PWM output is disabled.
4	SENSE	Current Sense	This pin senses the voltage across a resistor. When the voltage reaches the internal threshold, PWM output is disabled and this activates over-current protection. This pin also provides current amplitude information for Current Mode control.
5	VDD	Power Supply	Power supply
6	GATE	Driver Output	The totem-pole output driver for driving the power MOSFET

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. All voltage values, except differential voltages, are given with respect to GND pin.

Symbol	Parameter	Min.	Max.	Unit
V_{DD}	Supply Voltage		30	V
V_L	Input Voltage to FB, SENSE, and RT Pins	-0.3	7.0	V
Θ_{JA}	Thermal Resistance (Junction-to-Ambient)		244	°C/W
T_J	Operating Junction Temperature	-40	+125	°C
T_{STG}	Storage Temperature Range	-55	+150	°C
T_L	Lead Temperature, Wave Soldering, 10 Seconds		+260	°C
ESD	Human Body Model, JESD22-A114		5.5	kV
	Charge Device Model, JESD22-C101		2.0	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-40	+105	°C

Electrical Characteristics

V_{DD} = 15V and T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DD} Section						
$V_{DD\text{-}OP}$	Continuously Operating Voltage				20	V
$V_{DD\text{-}ON}$	Turn-On Threshold Voltage		15	16	17	V
$V_{DD\text{-}OFF}$	Turn-Off Voltage		6.5	7.0	7.5	V
$V_{DD\text{-}LH}$	Threshold Voltage for Latch-Off Release			4		V
$I_{DD\text{-}ST}$	Startup Current	$V_{DD\text{-}ON}$ – 0.16V		8	15	µA
$I_{DD\text{-}OP1}$	Operating Supply Current in PWM Operation	V_{DD} = 20V, V_{FB} = 3V Gate Open			2	mA
$I_{DD\text{-}OP2}$	Operating Supply Current when $V_{FB} < V_{FB\text{-}ZDC}$	V_{DD} = 15V, $V_{FB} < V_{FB\text{-}ZDC}$		600		µA
$V_{DD\text{-}OVP}$	V_{DD} Over-Voltage Protection	FAN6863WL-Latch, FAN6863WR-Auto Restart	21.2	22.2	23.2	V
$t_{D\text{-}VDDOVP}$	V_{DD} OVP Debounce Time			50		µs
$I_{DD\text{-}LH}$	Latch-Off Holding Current	V_{DD} = 5V; FAN6863W, FAN6863WL Only		70	80	µA
Feedback Input Section						
A_V	Input-Voltage to Current-Sense Attenuation		1/4.0	1/3.5	1/3.0	V/V
Z_{FB}	Input Impedance			17		kΩ
$V_{FB\text{-}OPEN}$	FB Pin Open Voltage		5.2	5.4	5.6	V
$V_{FB\text{-}OLP}$	Threshold Voltage for Open-Loop Protection		4.3	4.6	4.9	V
$t_{D\text{-}OLP}$	Open-Loop Protection Delay	$V_{FB} > V_{FB\text{-}OLP}$, t_{ON} > 2.5µs, T_A = -40 to +105°C	54	60	66	ms
$t_{D\text{-}SCP}$	Secondary Short-Circuit Protection Delay	FB > $V_{FB\text{-}OLP}$, t_{ON} < 2.5µs, T_A = -40 to +105°C	6	7	8	ms
$t_{ON\text{-}SCP}$	Short-Circuit Protection On-Time Detection	V_{FB}>$V_{FB\text{-}OLP}$, T_A = -40 to +105°C		2.5		µs
Current Sense Section						
t_{PD}	Delay to Output			100	250	ns
t_{LEB}	Leading-Edge Blanking Time		200	250		ns
$V_{LIMIT\text{-}H}$	HIGH Threshold Voltage for Current Limit	Duty>55%	0.57	0.60	0.63	V
$V_{LIMIT\text{-}L}$	LOW Threshold Voltage for Current Limit	Duty = 0%	0.36	0.39	0.42	V
$t_{SOFT\text{-}START}$	Period During Startup Time	Startup Time	4.75	5.00	10.00	ms
V_{SSCP}	Threshold Voltage for SENSE Short-Circuit Protection	t_{ON} > 4.5µs, FB < $V_{FB\text{-}OLP}$, T_A = -40 to +105°C		110		mV
$t_{ON\text{-}SSCP}$	Detect SENSE On Time for SENSE Short-Circuit Protection			4.4		µs
t_{SSCP}	Debounce Time for SENSE Short-Circuit Protection	t_{ON} > 4.5µs, $V_{FB} < V_{FB\text{-}OLP}$, T_A = -40 to +105°C		100		µs

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Electrical Characteristics (Continued)

V_{DD} = 15 and T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Oscillator Section						
f_{OSC}	Normal PWM Frequency – Center Frequency	$V_{FB} > V_{FB-N}$	60	65	68	kHz
f_{OSC}	Normal PWM Frequency – Hopping Range	$V_{FB} \geq V_{FB-N}$		±4.0		kHz
f_{OSC}	Normal PWM Frequency – Hopping Range	$V_{FB} = V_{FB-G}$		±2.9		kHz
t_{hop-1}	Hopping Period 1	$V_{FB} \geq V_{FB-N}$		4.4		ms
t_{hop-3}	Hopping Period 3	$V_{FB} = V_{FB-G}$		11.5		ms
f_{OSC-G}	Green Mode Minimum Frequency		18	22	26	kHz
V_{FB-N}	FB Threshold Voltage for Frequency Reduction		2.4	2.5	2.6	V
V_{FB-G}	FB Voltage at f_{OSC-G}		2.1	2.2	2.3	V
V_{FB-ZDC}	FB Threshold Voltage for Zero-Duty			1.6		V
$V_{FB-ZDCR}$ - V_{FB-ZDC}	ZDC Hysteresis			0.15		V
f_{DV}	Frequency Variation vs. V_{DD} Deviation	V_{DD} = 7.5V to 21V		0.5	2.0	%
f_{DT}	Frequency Variation vs. Temperature Deviation	T_A = -40 to +105°C			2	%

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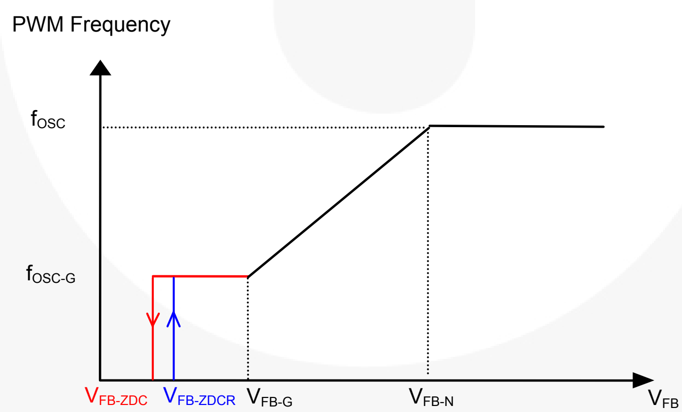

Figure 5. PWM Frequency

Electrical Characteristics (Continued)

V_{DD} = 15V and T_A = 25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
PWM Output Section						
DCY_{MAX}	Maximum Duty Cycle		68	75	85	%
V_{OL}	Output Voltage LOW	V_{DD} = 15V, I_O = 50mA			1.5	V
V_{OH}	Output Voltage HIGH	V_{DD} = 8V, I_O = 50mA	6			V
t_R	Rising Time (with Soft Driving)	GATE = 1nF		150		ns
t_F	Falling Time	GATE = 1nF		35		ns
V_{CLAMP}	Gate Output Clamping Voltage	V_{DD} = 20V	12.0	13.5	15.0	V
$I_{O-SOURCE}$	Gate Source Driving Capability	V_{DD} = 15V		400		mA
I_{O-SINK}	Gate Sink Driving Capability	V_{DD} = 15V		400		mA
Over-Temperature Protection (OTP) Section						
R_{RT}	Maximum External Resistance of RT Pin to Trigger Protection		9.2	10	11	kΩ
V_{OTP}	Threshold Voltage for Over-Temperature Protection	FAN6863W, FAN6863WL-Latch, FAN6863WR-Auto Restart, at 25°C	0.95	1.00	1.05	V
I_{RT}	Output Current of RT Pin		92	100	108	µA
t_{DOTP}	Over-Temperature Debounce Time	V_{FB}=V_{FB-N}	15	17	19	ms
V_{OTP2}	Second Threshold Voltage for Over-Temperature Protection	FAN6863W, FAN6863WL-Latch, FAN6863WR-Auto Restart, at 25°C	0.65	0.70	0.75	V
t_{DOTP2}	Second Over-Temperature Debounce Time		80	135	200	µs
T_{OTP}	Protection Junction Temperature(1)			+135		°C
$T_{Restart}$	Restart Junction Temperature(2)			T_{OTP}-25		°C

Notes:
1. When activated, the output is disabled and the latch is turned off.
2. The threshold temperature for enabling the output again and resetting the latch after OTP has been activated.

Typical Performance Characteristics

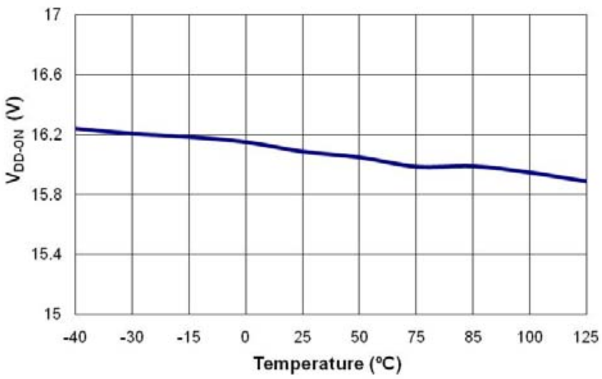

Figure 6. Turn-On Threshold Voltage (V_{DD-ON}) vs. Temperature

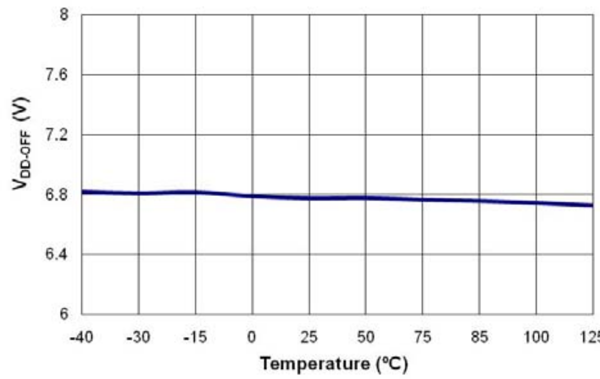

Figure 7. Turn-Off Threshold Voltage (V_{DD-OFF}) vs. Temperature

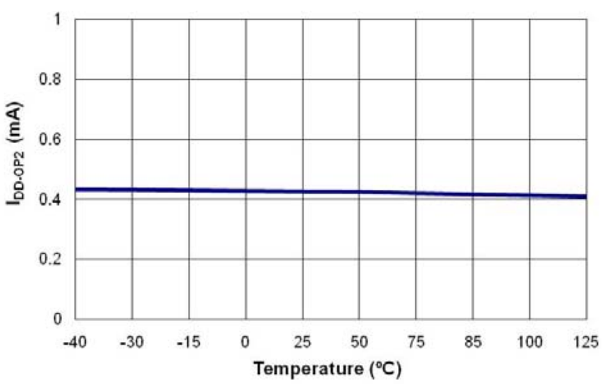

Figure 8. Operating Current (I_{DD-OP2}) vs. Temperature

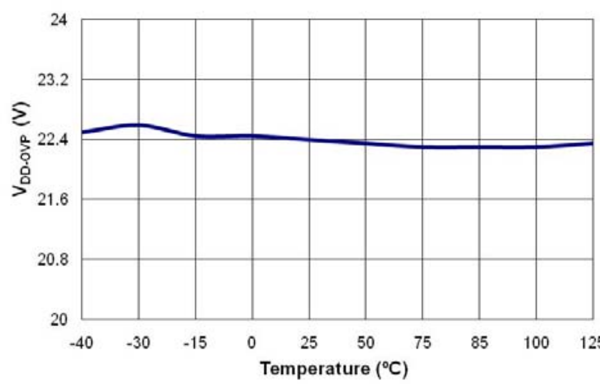

Figure 9. V_{DD} Over-Voltage Protection (V_{DD-OVP}) vs. Temperature

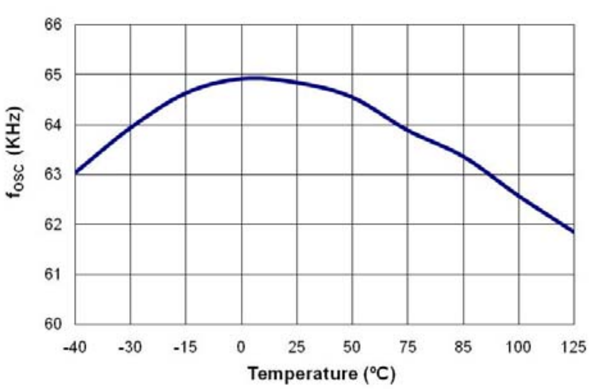

Figure 10. Center Frequency (f_{OSC}) vs. Temperature

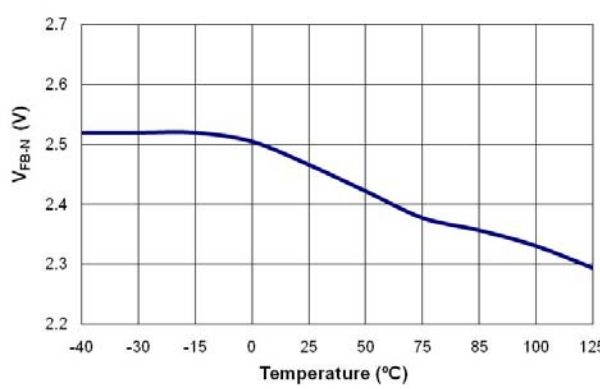

Figure 11. FB Threshold Voltage for Frequency Reduction (V_{FB-N}) vs. Temperature

Typical Performance Characteristics (Continued)

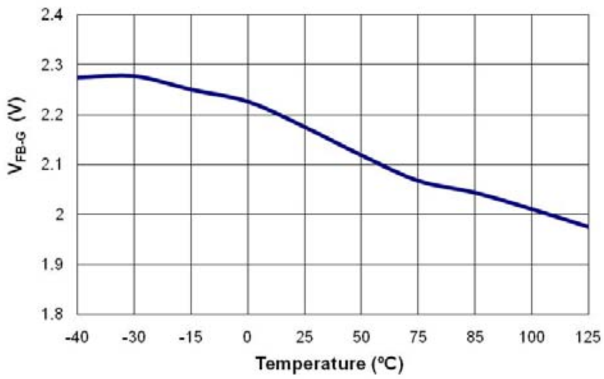

Figure 12. FB Voltage at f_{OSC-G} (V_{FB-G}) vs. Temperature

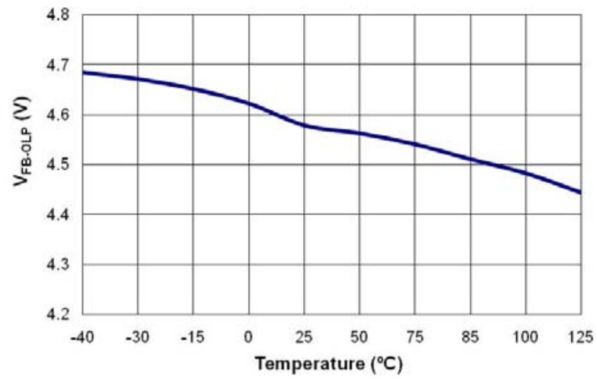

Figure 13. Threshold Voltage for Open-Loop Protection (V_{FB-OLP}) vs. Temperature

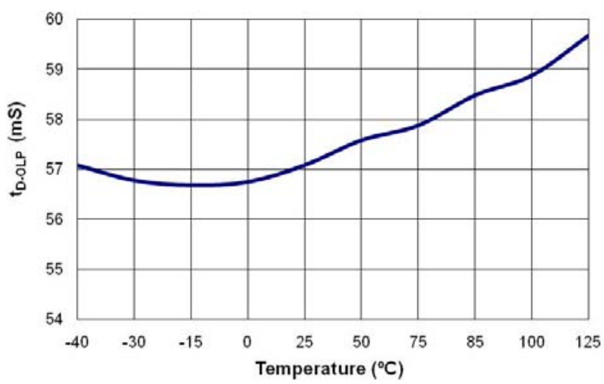

Figure 14. Open-Loop Protection Delay (t_{D-OLP}) vs. Temperature

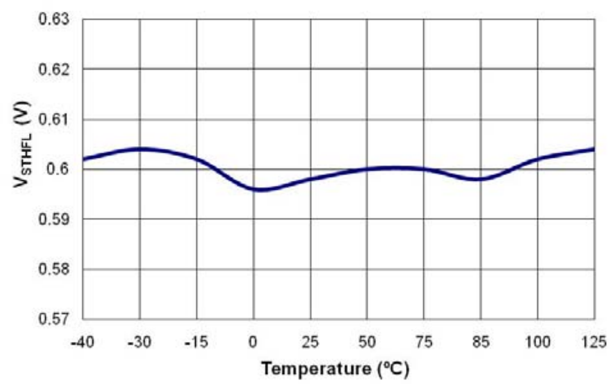

Figure 15. Flat Threshold Voltage for Current Limit (V_{STHFL}) vs. Temperature

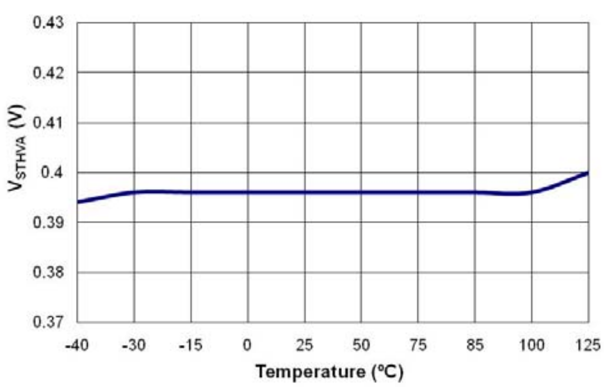

Figure 16. Valley Threshold Voltage for Current Limit (V_{STHVA}) vs. Temperature

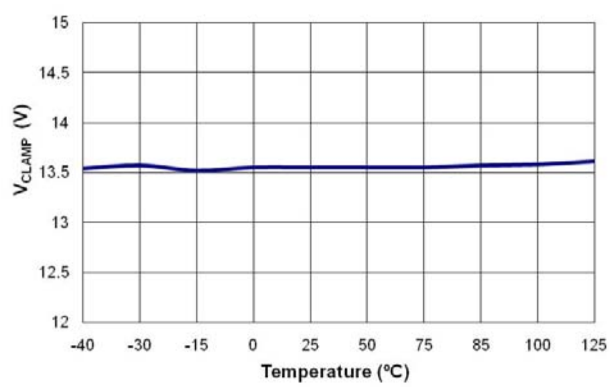

Figure 17. GATE Output Clamping Voltage (V_{CLAMP}) vs. Temperature

Typical Performance Characteristics (Continued)

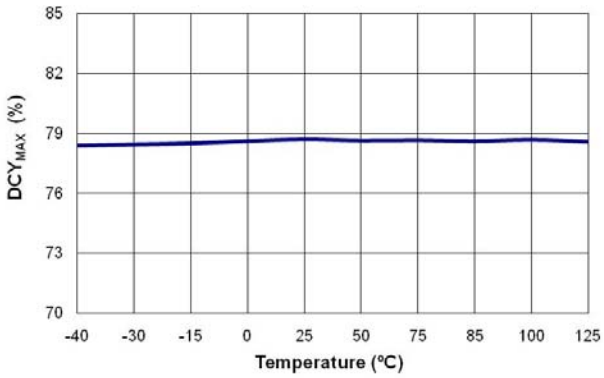

Figure 18. Maximum Duty Cycle (DCY_{MAX}) vs. Temperature

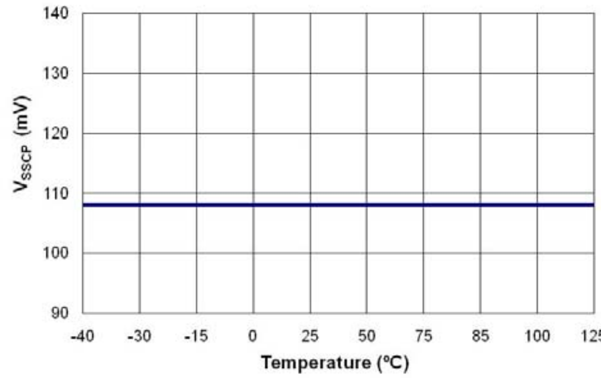

Figure 19. Threshold Voltage for SENSE Short-Circuit Protection (V_{SSCP}) vs. Temperature

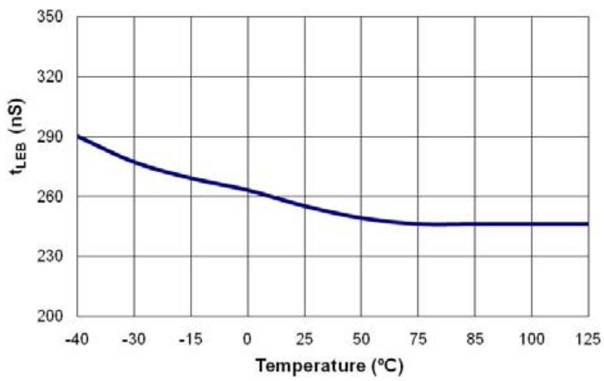

Figure 20. Leading-Edge Blanking Time (t_{LEB}) vs. Temperature

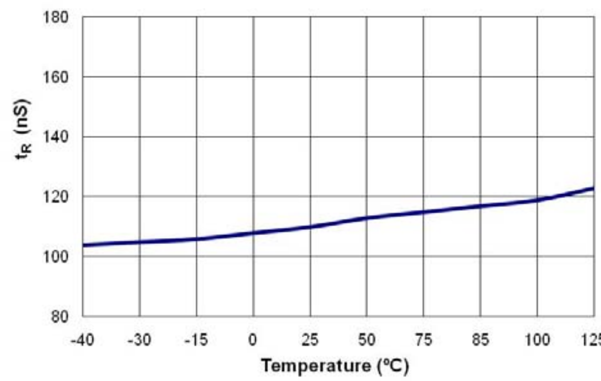

Figure 21. Rising Time (t_R) vs. Temperature

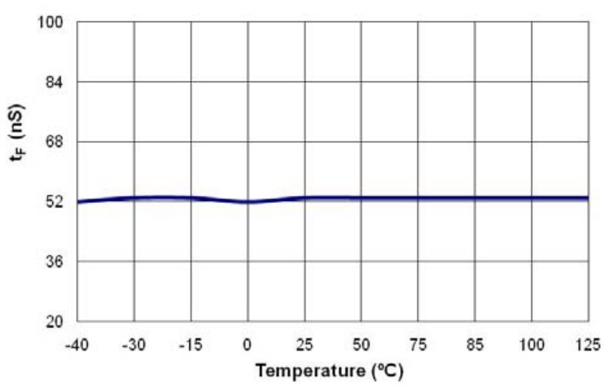

Figure 22. Falling Time (t_F) vs. Temperature

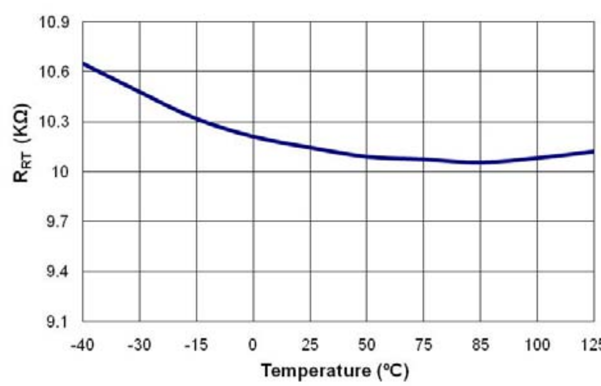

Figure 23. Internal Resistor from RT Pin (R_{RT}) vs. Temperature

Operation Description

Startup Operation

Figure 24 shows a typical startup circuit and transformer auxiliary winding for a typical application. Before switching operation begins, FAN6863W consumes only startup current (typically 8μA) and the current supplied through the startup resistor charges the V_{DD} capacitor (C_{DD}). When V_{DD} reaches turn-on voltage of 16V ($V_{DD\text{-}ON}$), switching begins and the current consumed increases to 2mA. Power is then supplied from the transformer auxiliary winding. The large hysteresis of V_{DD} (7V) provides more holdup time, which allows using a small capacitor for V_{DD}. The startup resistor is typically connected to AC line for a fast reset of latch protection.

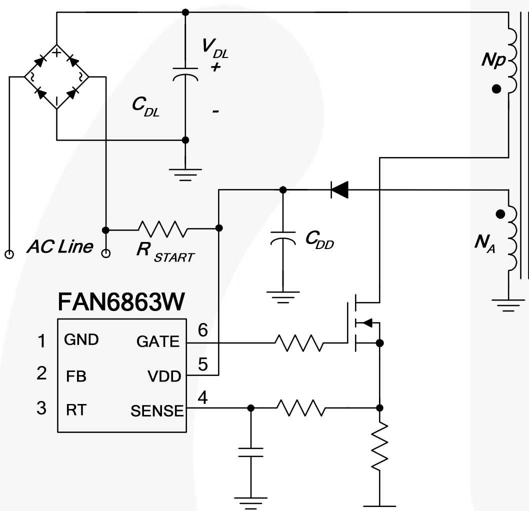

Figure 24. Startup Circuit

Green-Mode Operation

The FAN6863W uses feedback voltage (V_{FB}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 25, such that the switching frequency decreases as load decreases. In heavy-load conditions, the switching frequency is 65kHz. Once V_{FB} decreases below $V_{FB\text{-}N}$ (2.5V), the PWM frequency starts to linearly decrease from 65kHz to 22.5kHz to reduce the switching losses. As V_{FB} decreases below $V_{FB\text{-}G}$ (2.2V), the switching frequency is fixed at 22.5kHz and FAN6863W enters "deep" Green Mode, where the operating current decreases to 600μA (maximum), further reducing the standby power consumption. As V_{FB} decreases below $V_{FB\text{-}ZDC}$ (1.6V), FAN6863W enters Burst-Mode operation. When V_{FB} drops below $V_{FB\text{-}ZDC}$, switching stops and the output voltage starts to drop, which causes the feedback voltage to rise. Once V_{FB} rises above $V_{FB\text{-}ZDC}$, switching resumes. Burst Mode alternately enables and disables switching, thereby reducing switching loss in Standby Mode, as shown in Figure 26.

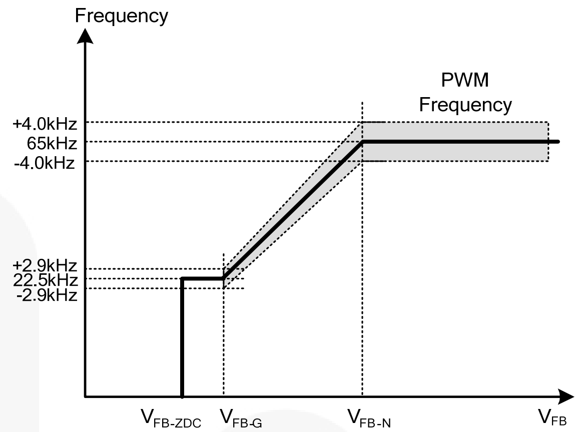

Figure 25. PWM Frequency

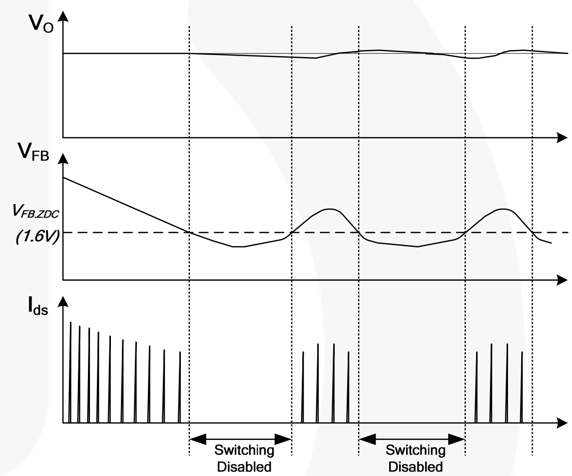

Figure 26. Burst-Mode Operation

Frequency Hopping

EMI reduction is accomplished by frequency hopping, which spreads the energy over a wider frequency range than the bandwidth measured by the EMI test equipment. An internal frequency hopping circuit changes the switching frequency between 61.0kHz and 69.0kHz with a period of 4.4ms, as shown in Figure 27. It covers the whole frequency range in hopping function and shrinks the period with operation frequency proportionally.

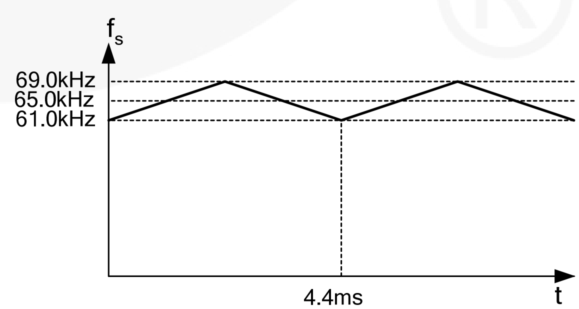

Figure 27. Frequency Hopping

Protections

Self-protective functions include V_{DD} Over-Voltage Protection (OVP), Open-Loop / Overload Protection (OLP), Over-Current Protection (OCP), Short-Circuit Protection (SCP), SENSE pin Short-Circuit Protection (SSCP), and Over-Temperature Protection (OTP). OLP, OCP, SCP, and SSCP are Auto-Restart Mode protections; OVP and OTP are Latch-Mode protections.

Auto-Restart Mode Protection

Once a fault condition is detected, switching is terminated and the MOSFET remains off. This causes V_{DD} to fall because no more power is delivered from auxiliary winding. When V_{DD} falls to V_{DD-OFF} (7V), the protection is reset and the operating current reduces to startup current, which causes V_{DD} to rise. FAN6863W resumes normal operation when V_{DD} reaches V_{DD-ON} (16V). In this manner, the auto-restart can alternately enable and disable the switching of the MOSFET until the fault condition is eliminated (*see Figure 28*).

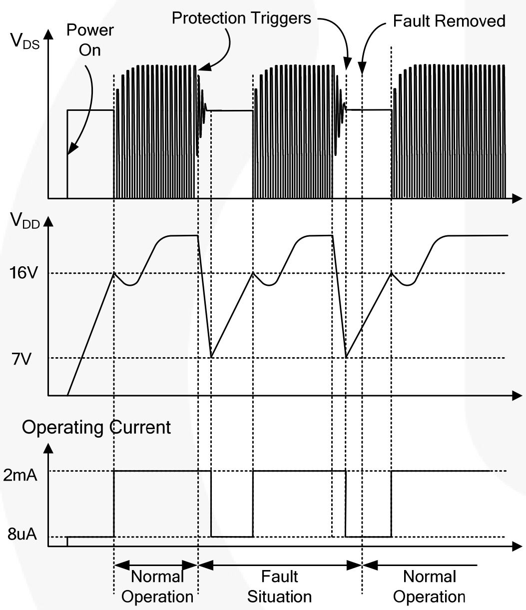

Figure 28. Auto Restart Operation

Latch-Mode Protection

Once this protection is triggered, switching is terminated and the MOSFET remains off. The latch is reset only when V_{DD} is discharged below 4V by unplugging the AC power line.

Over-Current Protection (OCP)

The FAN6863W over-current protection threshold is a pulse-by-pulse current limit (V_{LIMIT}), which turns off MOSFET for the remainder of the switching cycle when the sensing voltage of MOSFET drain current reaches the threshold. The V_{LIMIT} compensates the power limit variation over universal input range and adaptively keeps the power limit substantially constant.

Open-Loop / Overload Protection (OLP)

When the upper branch of the voltage divider for the shunt regulator (KA431 shown in Figure 29) is broken, no current flows through the photo-coupler transistor, which pulls up the feedback voltage to 5.4V.

When feedback voltage is above 4.6V for longer than 60ms, OLP is triggered. This protection is also triggered when the SMPS output drops below the nominal value for longer than 60ms due to the overload condition.

If the secondary output-short situation occurs when the feedback voltage is above 4.6V, protection time is 7ms for shorter debounce time.

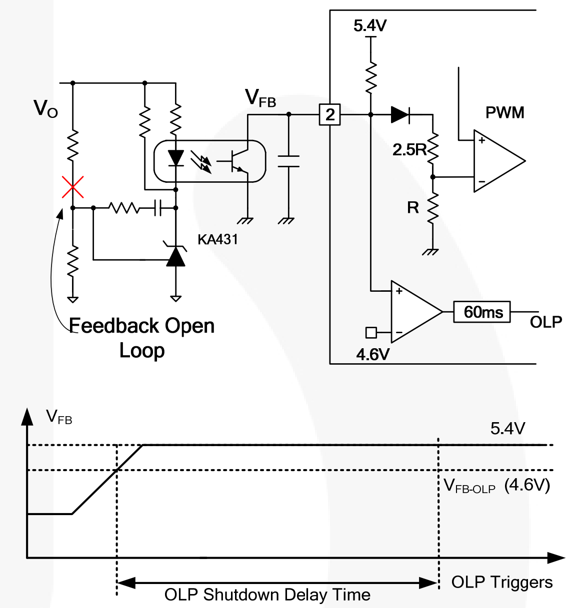

Figure 29. OLP Operation

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents IC damage caused by over voltage on the V_{DD} pin. The OVP is triggered when V_{DD} reaches 22.2V. A debounce time (typically 50µs) prevents false triggering by switching noise.

Over-Temperature Protection (OTP)

The OTP circuit is composed of current source and voltage comparators. Typically, an NTC thermistor is connected between the RT and GND pins. If the voltage of this pin drops below a threshold of 1.0V, PWM output is disabled after t_{DOTP} debounce time. If this pin voltage drops below 0.7V, it triggers the latch-off protection immediately after t_{DOTP2} debounce time.

Typical Application Circuit (Netbook Adapter by Flyback)

Application	Fairchild Devices	Input Voltage Range	Output
Netbook Adapter	FAN6863W	90~265V_{AC}	19V/2.1A (40W)

Features

- High efficiency (>85.3% at full-load condition) meeting EPS regulation with enough margin
- Low standby (pin<0.1W at no-load condition)
- Soft-start time: 5ms

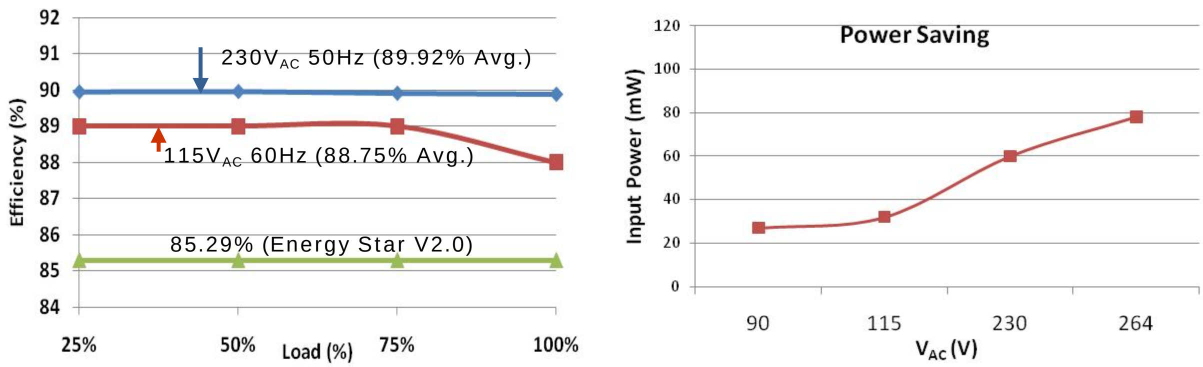

Figure 30. Measured Efficiency and Power Saving

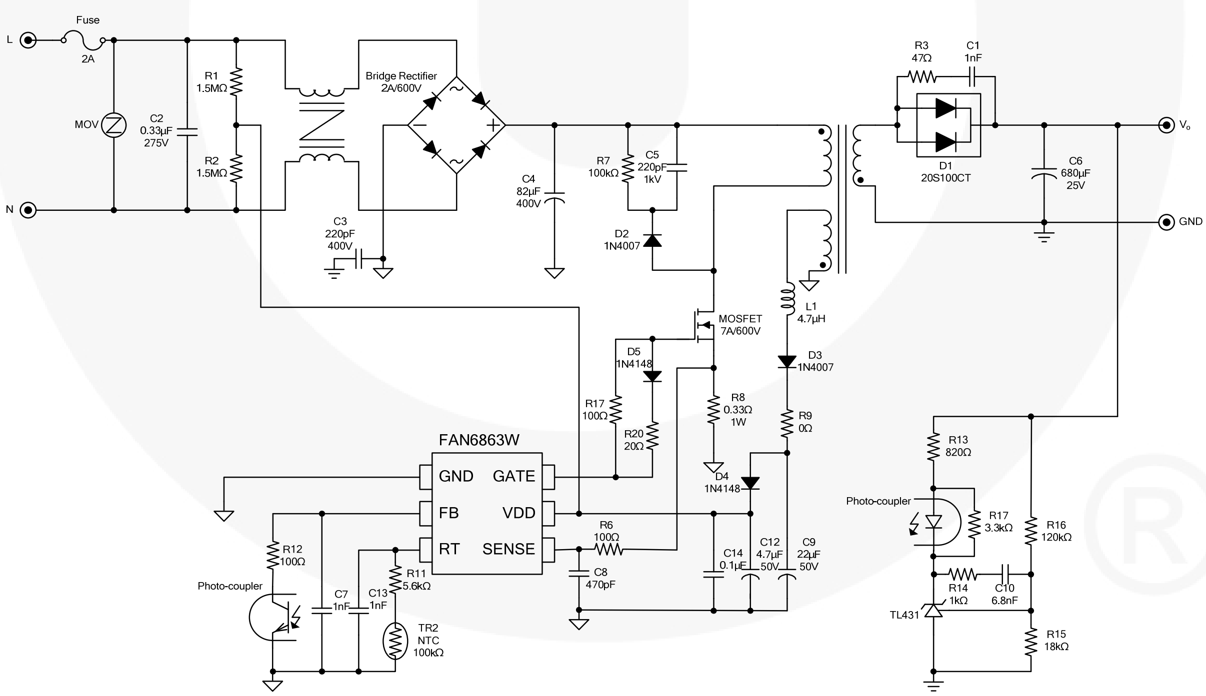

Figure 31. Schematic of Typical Application Circuit

Transformer Specification

- Core: RM 8
- Bobbin: RM 8

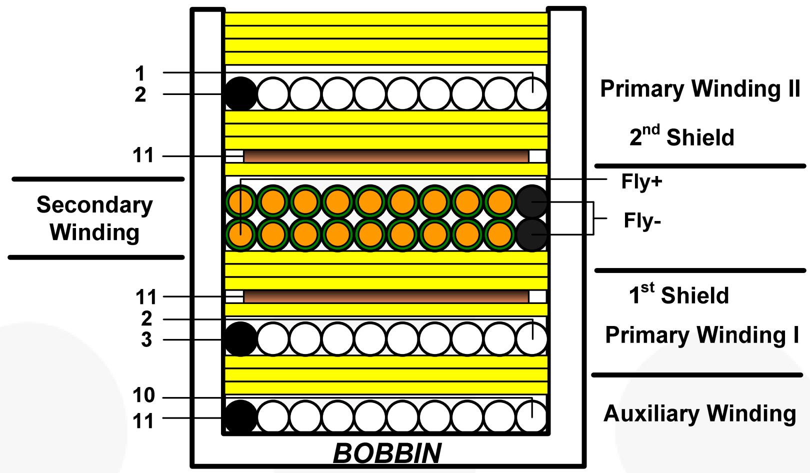

Figure 32. Transformer

NO	Terminal		Wire	Ts	Insulation	Barrier	
	S	F			Ts	Primary	Secondary
N1	11	10	0.25 • 1	9	3		
N2	3	2	0.25 • 1	33	1		
	11		COPPER SHIELD	1.2	3		
N3	Fly-	Fly+	0.5 • 2	12	1		
	11		COPPER SHIELD	1.2	3		
N4	2	1	0.25 • 1	33	4		
			CORE ROUNDING TAPE		3		

	Pin	Specification	Remark
Primary-Side Inductance	3 – 1	920μH ±5%	100kHz, 1V
Primary-Side Effective Leakage	3 – 1	15μH Maximum	Short One of the Secondary Windings

Physical Dimensions

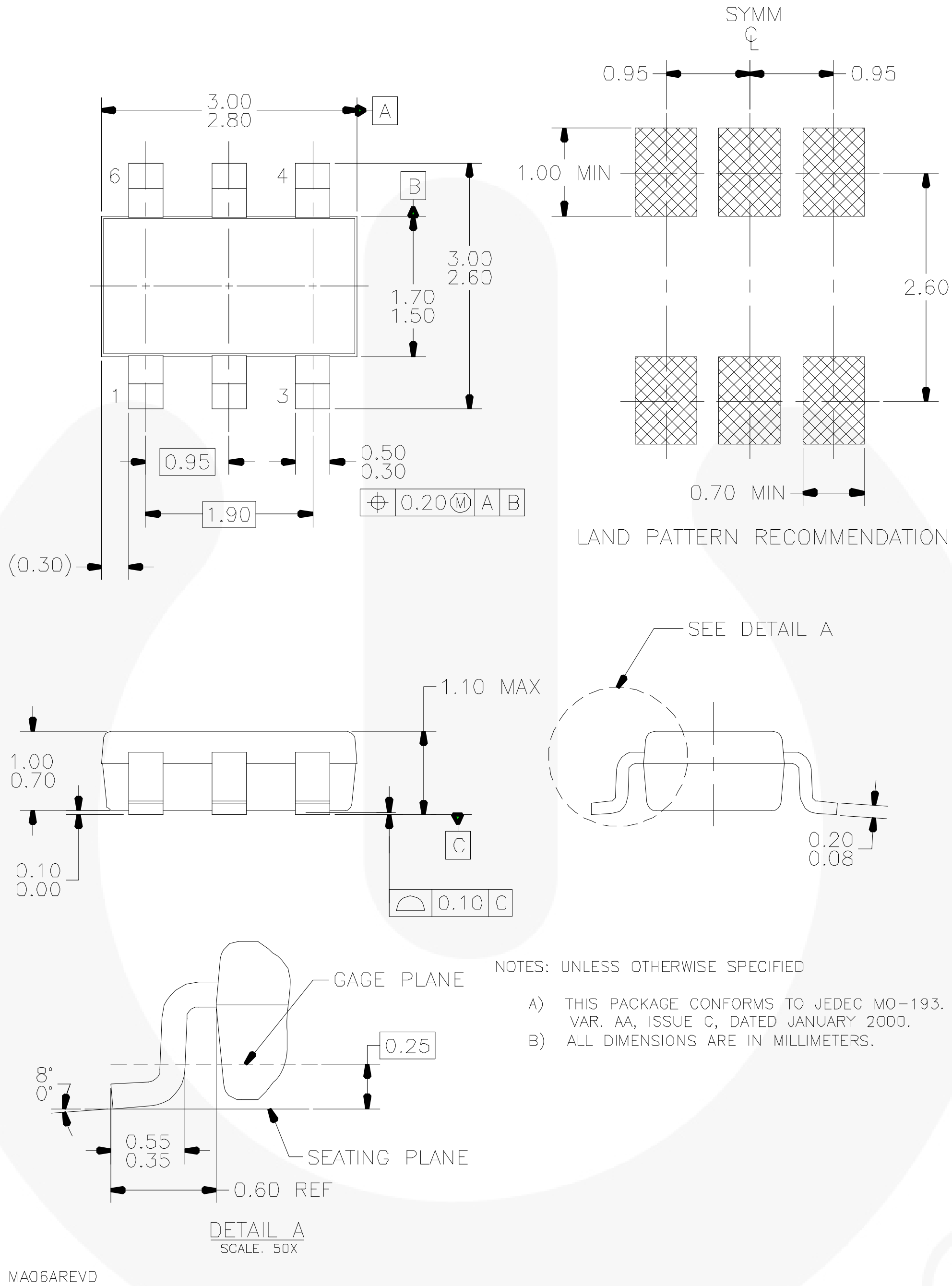

Figure 33. 6-Lead, SuperSOT™-6 JEDEC, M0-193 1.6mm Wide

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