

Single 8/Differential 4 Channel CMOS Analog Multiplexers With Active Overvoltage Protection

January 1989

Features

- This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- No Channel Interaction During Overvoltage
- Guaranteed R_{ON} Matching
- 44V Maximum Power Supply
- Break-Before-Make Switch
- Analog Signal Range $\pm 15V$
- Access Time (Max.) $1.0\mu s$
- Power Dissipation (Max.) $45mW$

Applications

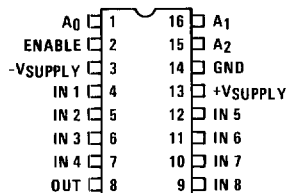
- Data Acquisition Systems
- Control Systems
- Telemetry

Description

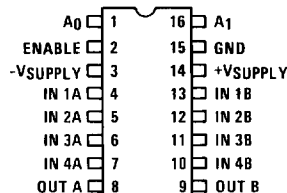
The HI-548/883 and HI-549/883 are analog multiplexers with Active Overvoltage Protection and guaranteed R_{ON} matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70 volt peak-to-peak levels with $\pm 15V$ supplies and digital inputs will sustain continuous faults up to 4 volts greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur; each input presents $1k\Omega$ of resistance under this condition. These features make the HI-548/883 and HI-549/883 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. Both devices are fabricated with 44 volt dielectrically isolated CMOS technology. The HI-548/883 is a 8 channel device and the HI-549/883 is a 4 channel differential version. If input overvoltage protection is not needed, the HI-508/883 and HI-509/883 multiplexers are recommended. For further information see Application Notes 520 and 521.

Pinouts

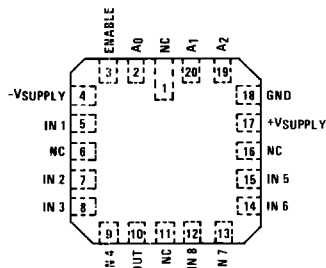
HI1-548/883 (CERAMIC DIP)
TOP VIEW



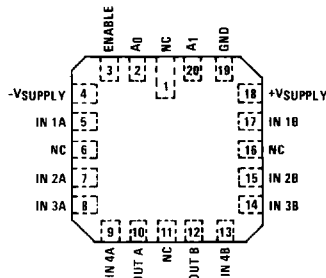
HI1-549/883 (CERAMIC DIP)
TOP VIEW



HI4-548/883 (CERAMIC LCC)
TOP VIEW

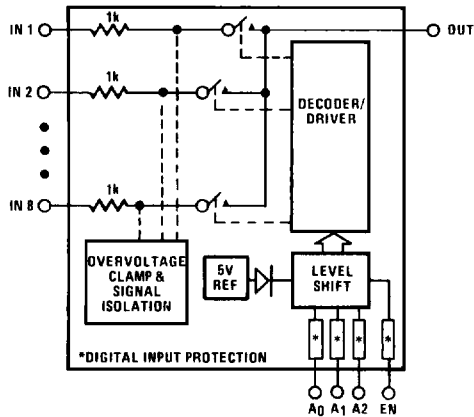


HI4-549/883 (CERAMIC LCC)
TOP VIEW



Functional Diagrams

HI-548/883

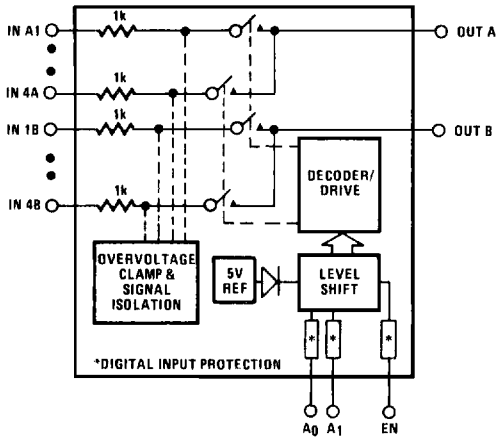


TRUTH TABLES

HI-548/883

A ₂	A ₁	A ₀	EN	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-549/883



HI-549/883

A ₁	A ₀	EN	"ON" CHANNEL PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Specifications HI-548/883 HI-549/883

Absolute Maximum Ratings

Voltage Between Supply Pins	44V
+V _{SUPPLY} to Ground	22V
-V _{SUPPLY} to Ground	25V
Analog Input Voltage	
+V _S	+V _{SUPPLY} +20V
-V _S	-V _{SUPPLY} -20V
Digital Input Voltage	
+V _{EN} , +V _A	+V _{SUPPLY} +4V
-V _{EN} , -V _A	-V _{SUPPLY} -4V
	or 20mA, whichever occurs first.
Continuous Current, S or D	20mA
Peak Current, S or D	
(Pulsed at 1ms, 10% Duty Cycle Max.)	40mA
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 Seconds)	275°C

Junction Temperature	+175°C
Thermal Resistance, Junction-to-Case (θ_{JC})	
Ceramic DIP Package	26°C/W
Ceramic LCC Package	19°C/W
Thermal Resistance, Junction-to-Ambient (θ_{JA})	
Ceramic DIP Package	80°C/W
Ceramic LCC Package	76°C/W
Power Dissipation (at 75°C)	
Ceramic DIP Package	1.25W
Ceramic LCC Package	1.32W
Power Dissipation Derating Factor (Above +75°C)	
Ceramic DIP Package	12.5mW/°C
Ceramic LCC Package	13.2mW/°C
ESD Classification	≤2000V

Recommended Operating Conditions

Operating Temperature Range	-55°C to +125°C
Operating Supply Voltage ($\pm V_{SUPPLY}$)	$\pm 15V$
Analog Input Voltage (V_S)	$\pm V_{SUPPLY}$

Logic Low Level (V_{AL})	0V to 0.8V
Logic High Level (V_{AH})	+4V to +V _{SUPPLY}
Max RMS Current, S or D	8mA

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at +V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V, V_{EN} = 4.0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Leakage Current	I _{IH}	Measure Inputs Sequentially, Connect All Unused Inputs to GND	1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	μA
	I _{IL}		1, 2, 3	+25°C, +125°C, -55°C	-1.0	1.0	μA
Leakage Current Into the Source Terminal of an "OFF" Switch	+I _{S(OFF)}	V _S = +10V, V _D = -10V, V _{EN} = 0.8V All Unused Inputs = -10V	1	+25°C	-10	+10	nA
			2, 3	+125°C, -55°C	-50	+50	nA
	-I _{S(OFF)}	V _S = -10V, V _D = +10V, V _{EN} = 0.8V All Unused Inputs = +10V	1	+25°C	-10	+10	nA
			2, 3	+125°C, -55°C	-50	+50	nA
Leakage Current Into the Drain Terminal of an "OFF" Switch	+I _{D(OFF)}	V _D = +10V, V _{EN} = 0.8V All Unused Inputs = -10V HI-548/883 HI-549/883	1	+25°C	-10	+10	nA
			2, 3	+125°C, -55°C	-200	+200	nA
	-I _{D(OFF)}	V _D = -10V, V _{EN} = 0.8V All Unused Inputs = +10V HI-548/883 HI-549/883	1	+25°C	-10	+10	nA
			2, 3	+125°C, -55°C	-200	+200	nA
Leakage Current From an "ON" Driver Into the Switch (Drain)	+I _{D(ON)}	V _S = V _D = +10V All Unused Inputs = -10V HI-548/883 HI-549/883	1	+25°C	-10	+10	nA
			2, 3	+125°C, -55°C	-200	+200	nA
	-I _{D(ON)}	V _S = V _D = -10V All Unused Inputs = +10V HI-548/883 HI-549/883	1	+25°C	-10	+10	nA
			2, 3	+125°C, -55°C	-200	+200	nA
Overvoltage Protected, Leakage Current Into the Drain Terminal of an "OFF" Switch	I _{D(OFF)}	V _S = 33V, V _D = 0V, V _{EN} = 0.8V V _S applied at ≤25% duty cycle	1, 2, 3	+25°C, +125°C, -55°C	-2.0	+2.0	μA
		V _S = -33V, V _D = 0V, V _{EN} = 0.8V V _S applied at ≤25% duty cycle	1, 2, 3	+25°C, +125°C, -55°C	-2.0	+2.0	μA
Positive Supply Current	I(+)	V _A = 0V, V _{EN} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C		2.0	mA
Negative Supply Current	I(-)	V _A = 0V, V _{EN} = 4.0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Standby Positive Supply Current	+I _{SBY}	V _A = 0V, V _{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C		2.0	mA
Standby Negative Supply Current	-I _{SBY}	V _A = 0V, V _{EN} = 0V	1, 2, 3	+25°C, +125°C, -55°C	-1.0		mA
Switch "ON" Resistance	+R _{DS1}	V _S = 10V I _D = 100μA	1	+25°C		1500	Ω
			2, 3	+125°C, -55°C		1800	Ω
	-R _{DS1}	V _S = -10V I _D = -100μA	1	+25°C		1500	Ω
			2, 3	+125°C, -55°C		1800	Ω
Logic Level Voltage	V _{AL}	Note 1, 2	1, 2, 3	+25°C, +125°C, -55°C		0.8	V
	V _{AH}	Note 1, 2	1, 2, 3	+25°C, +125°C, -55°C	4.0		V
Difference in switch "ON" Resistance Between Channels	+ΔR _{DS1}	$\frac{(+R_{DS1MAX}) - (+R_{DS1MIN}) \times 100}{+R_{DS1AVE}}$	1	+25°C		7	%
	-ΔR _{DS1}	$\frac{(-R_{DS1MAX}) - (-R_{DS1MIN}) \times 100}{-R_{DS1AVE}}$	1	+25°C		7	%

NOTES: 1. Used for forcing conditions for all DC tests unless otherwise specified.
2. To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.

CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at +V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V, V_{EN} = 4.0V, Unless Otherwise Specified.

A.C. PARAMETERS	SYMBOL	CONDITIONS	SUBGROUP	TEMP	LIMITS		UNITS
					MIN	MAX	
Break-Before-Make Time Delay	t _D	R _L = 1kΩ, C _L = 12.5pF	9	+25°C	25		ns
Propagation Delay Times: Address Inputs to I/O Channel Times	t _A	R _L = 10MΩ, C _L = 14pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
Enable to I/O	t _{ON(EN)}	R _L = 1kΩ, C _L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns
	t _{OFF(EN)}	R _L = 1kΩ, C _L = 12.5pF	9	+25°C		500	ns
			10, 11	+125°C, -55°C		1000	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at +V_{SUPPLY} = +15V, -V_{SUPPLY} = -15V, V_{EN} = 4.0V, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS		UNITS
					MIN	MAX	
Capacitance: Address Input	C _A	V ₊ = V ₋ = 0V f = 1MHz	3	+25°C		10	pF
Capacitance: Output Switch	C _{OS}	V ₊ = V ₋ = 0V f = 1MHz	HI-548/883 3	+25°C		45	pF
			HI-549/883 3	+25°C		25	pF
Capacitance Input Switch	C _{IS}	V ₊ = V ₋ = 0V f = 1MHz	3	+25°C		15	pF
Charge Transfer Error	V _{CTE}	V _S = GND V _{GEN} = 0V to 5V, f = 200kHz	3	+25°C		10	mV
Off Isolation	V _{ISO}	V _{EN} = 0.8V, R _L = 1kΩ C _L = 15pF, V _S = 7V _{RMS} f = 100kHz	3, 4	+25°C	-50		dB

NOTES: 3. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

4. Worst case isolation occurs on channel 4 due to proximity of the output pins.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

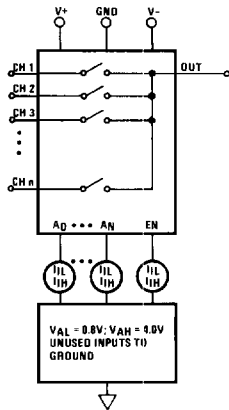
MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1, 2 & 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

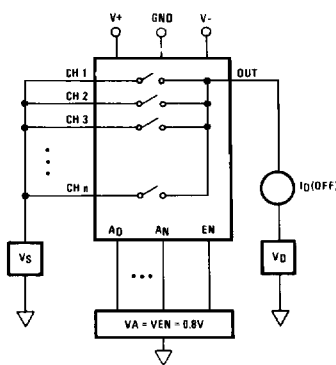
CAUTION: These devices are sensitive to electrostatic discharge. Proper IC handling procedures should be followed.

Test Circuits

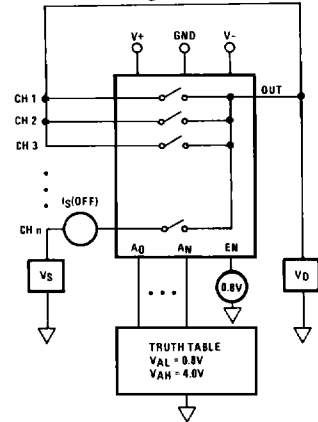
INPUT LEAKAGE CURRENT



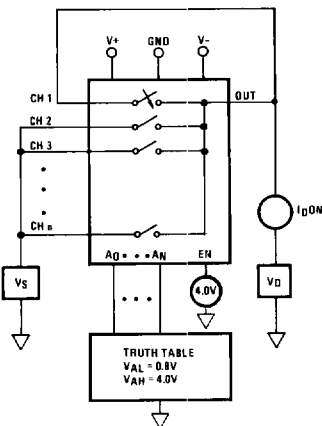
$I_D(OFF)$



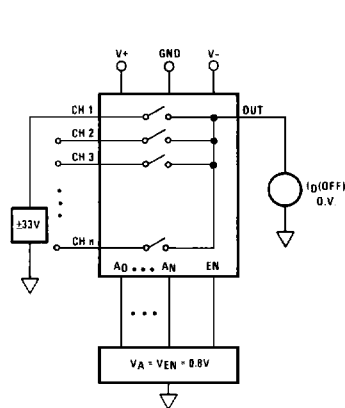
$I_S(OFF)$



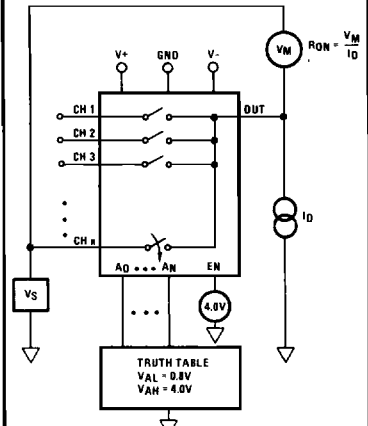
$I_D(ON)$



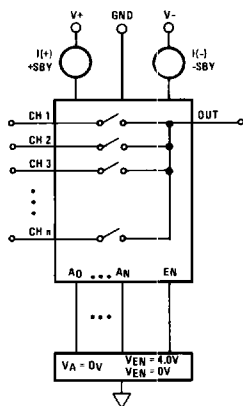
$I_D(OFF)$ OVERVOLTAGE



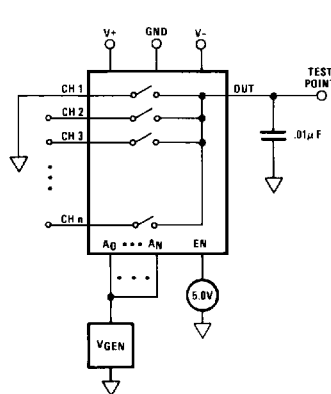
R_{DS}



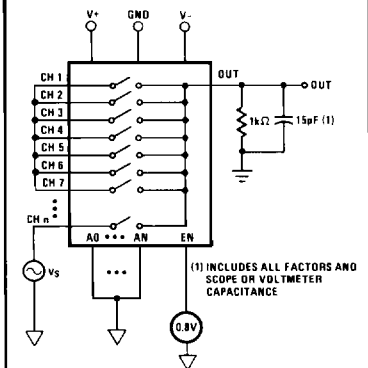
SUPPLY CURRENTS



CHARGE TRANSFER ERROR

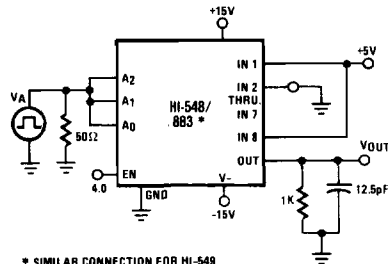
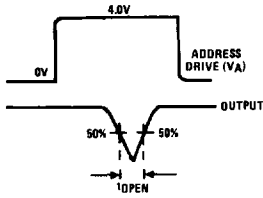


OFF CHANNEL ISOLATION



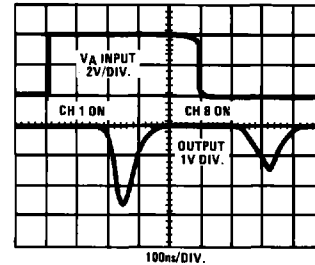
Switching Waveforms

**BREAK-BEFORE-MAKE
DELAY (t_{OPEN})**

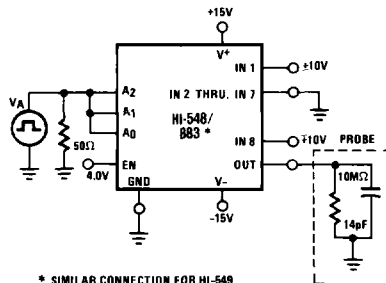
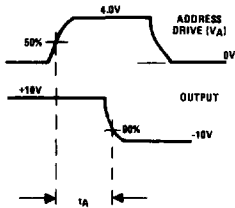


* SIMILAR CONNECTION FOR HI-549

**BREAK-BEFORE-MAKE
DELAY (t_{OPEN})**

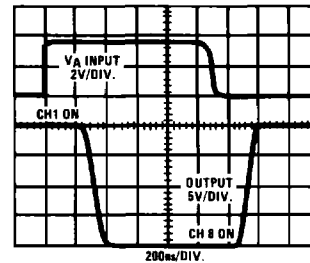


ACCESS TIME

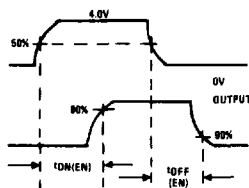


* SIMILAR CONNECTION FOR HI-549

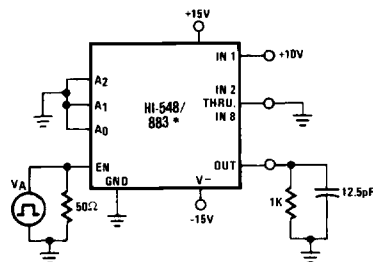
ACCESS TIME



ENABLE DRIVE

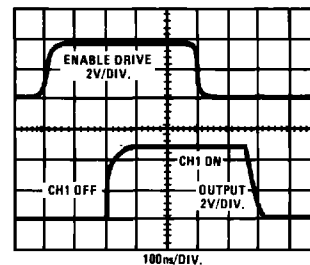


**ENABLE DELAY
 $t_{\text{ON}}(\text{EN})$, $t_{\text{OFF}}(\text{EN})$**



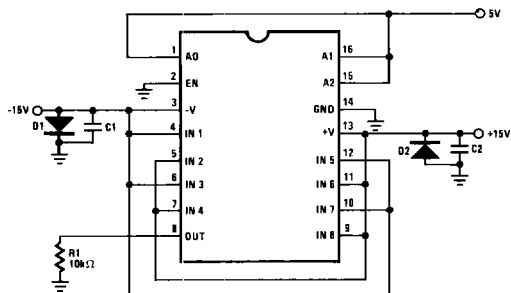
* SIMILAR CONNECTION FOR HI-549

**ENABLE DELAY
 $t_{\text{ON}}(\text{EN})$, $t_{\text{OFF}}(\text{EN})$**



Burn-In Circuits

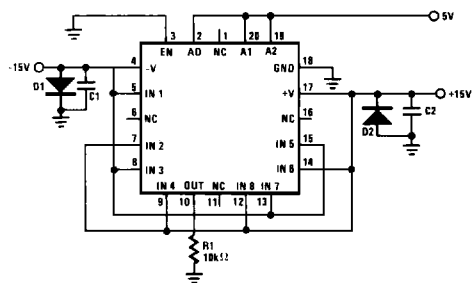
HI-548/883 CERAMIC DIP



NOTES:

R1 = $10k\Omega \pm 5\%$ 1/2 or 1/4W (per socket)
 C1, C2 = $0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
 D1, D2 = IN4002 (or equivalent) (per board)

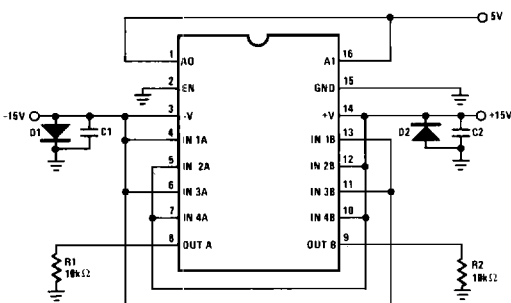
HI-548/883 CERAMIC LCC



NOTES:

R1 = $10k\Omega \pm 5\%$ 1/2 or 1/4W (per socket)
 C1, C2 = $0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
 D1, D2 = IN4002 (or equivalent) (per board)

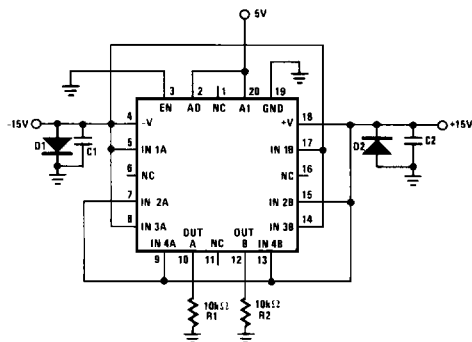
HI-549/883 CERAMIC DIP



NOTES:

R1, R2 = $10k\Omega \pm 5\%$ 1/2 or 1/4W (per socket)
 C1, C2 = $0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
 D1, D2 = IN4002 (or equivalent) (per board)

HI-549/883 CERAMIC LCC

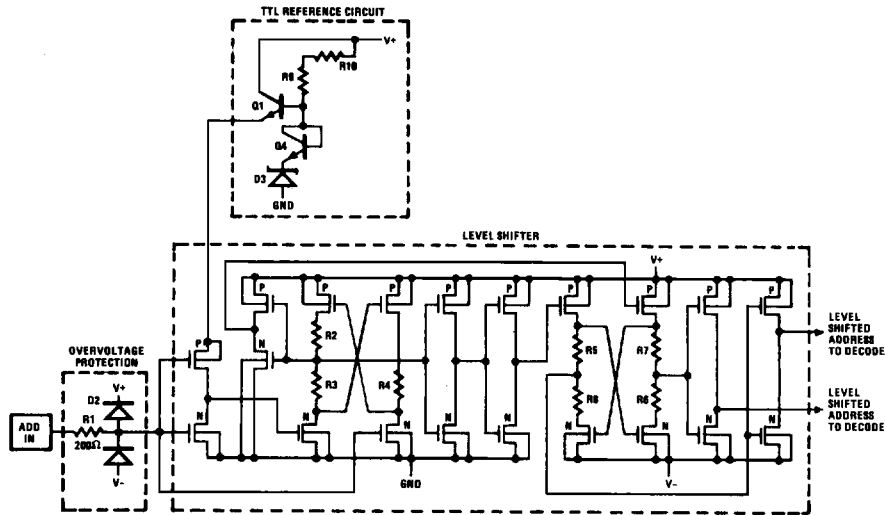


NOTES:

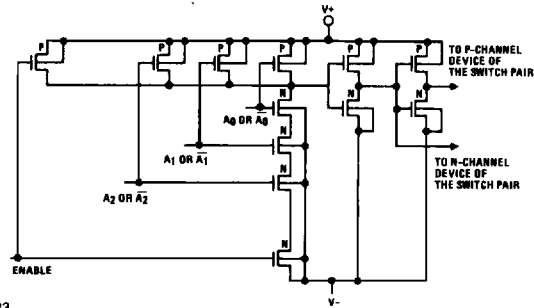
R1, R2 = $10k\Omega \pm 5\%$ 1/2 or 1/4W (per socket)
 C1, C2 = $0.01\mu F$ (per socket) or $0.1\mu F$ (per row)
 D1, D2 = IN4002 (or equivalent) (per board)

Schematic Diagrams

ADDRESS INPUT BUFFER AND LEVEL SHIFTER

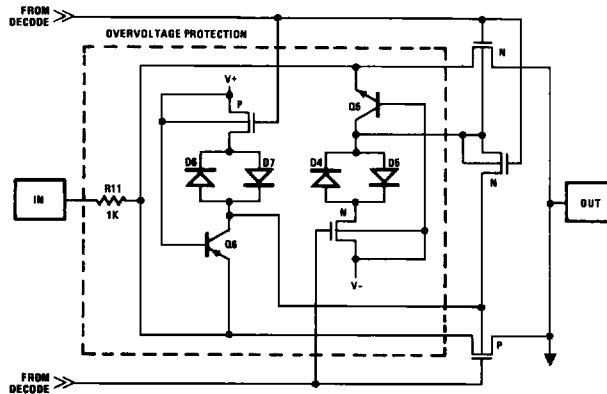


ADDRESS DECODER



Delete A₂ or $\bar{A}_2$ input for HI-549/883

MULTIPLEX SWITCH



Die Characteristics

DIE DIMENSIONS: 83 x 108 x 19 mils

METALLIZATION

Type: Al

Thickness: $16\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

GLASSIVATION

Type: Nitride

Thickness: $7\text{k}\text{\AA} \pm 0.7\text{k}\text{\AA}$

WORST CASE CURRENT DENSITY: $1.4 \times 10^5 \text{ A/cm}^2$

TRANSISTOR COUNT:

HI-548/883 253

HI-549/883 253

PROCESS: CMOS-DI

DIE ATTACH

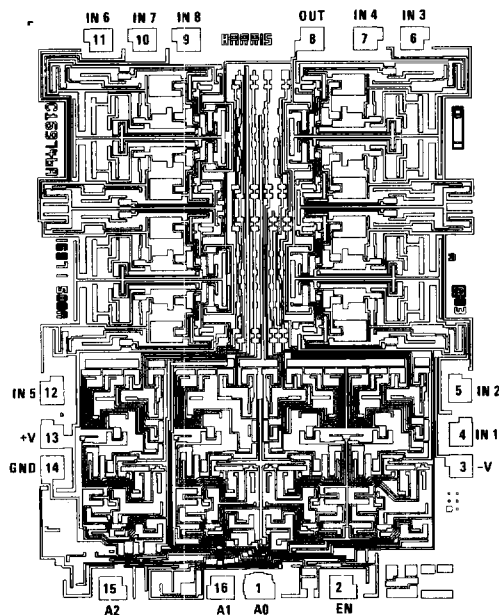
Material: Gold Silicon Eutectic Alloy

Temperature: Ceramic DIP — 460°C (Max)

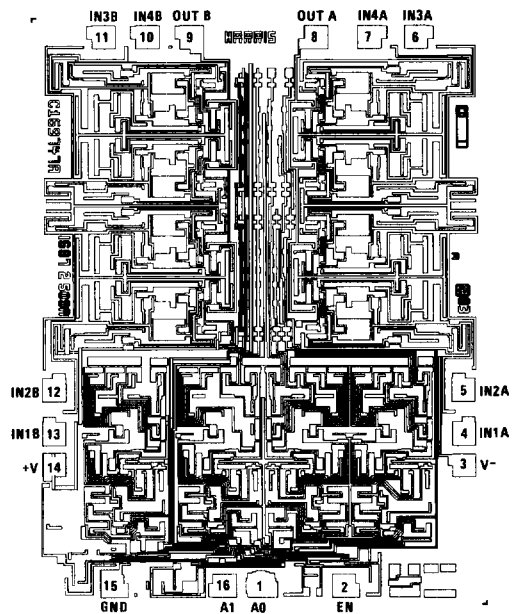
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

HI-548/883



HI-549/883



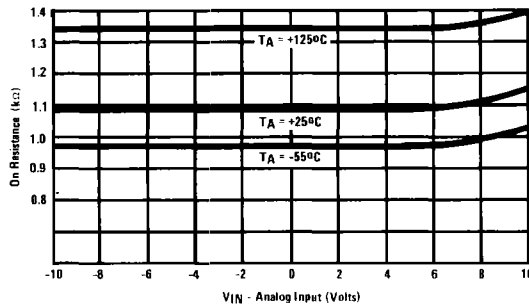
NOTE: Pad Numbers Correspond to DIP Pin Numbers Only

Single 8/Differential 4 Channel CMOS Analog Multiplexers With Active Overvoltage Protection

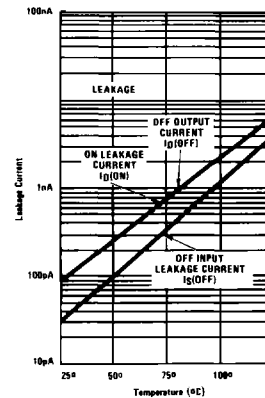
The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design data only. No guarantee is implied.

Typical Performance Characteristics Unless Otherwise Specified: $T_A = 25^\circ\text{C}$, $V_{\text{SUPPLY}} = \pm 15\text{V}$, $V_{\text{AH}} = +4\text{V}$, $V_{\text{AL}} = 0.8\text{V}$

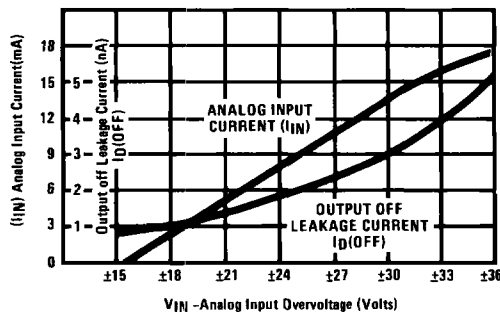
ON RESISTANCE vs. ANALOG INPUT VOLTAGE



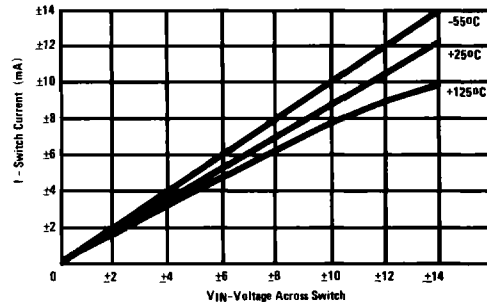
LEAKAGE CURRENT vs. TEMPERATURE



ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



ON CHANNEL CURRENT vs. VOLTAGE



SUPPLY CURRENT vs. TOGGLE FREQUENCY

