32-bit Microcontroller

CMOS

FR60 MB91460D Series

MB91F465DA, MB91F467DA/F467DB

PRELIMINARY

■ DESCRIPTION

MB91460D series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family* of CPUs.

This series contains the LIN-USART and CAN controllers.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Limited.

■ FEATURES

1. FR60 CPU core

- 32-bit RISC, load/store architecture, five-stage pipeline
- 16-bit fixed-length instructions (basic instructions)
- Instruction execution speed: 1 instruction per cycle
- Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
- Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
- Register interlock function: Facilitating assembly-language coding
- Built-in multiplier with instruction-level support
  Signed 32-bit multiplication : 5 cycles
  Signed 16-bit multiplication : 3 cycles
- Interrupts (save PC/PS) : 6 cycles (16 priority levels)

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Be sure to refer to the “Check Sheet” for the latest cautions on development.

“Check Sheet” is seen at the following support page
URL : http://www.fujitsu.com/global/services/microelectronics/product/micom/support/index.html

“Check Sheet” lists the minimal requirement items to be checked to prevent problems beforehand in system development.

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- Harvard architecture enabling program access and data access to be performed simultaneously
- Instructions compatible with the FR family

2. Internal peripheral resources

- General-purpose ports : Maximum 170 ports
- DMAC (DMA Controller)
  Maximum of 5 channels able to operate simultaneously. (External to external : 1 channel)
  3 transfer sources (external pin/internal peripheral/software)
  Activation source can be selected using software.
  Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
  Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
  Fly-by transfer support (between external I/O and memory)
  Transfer data size selectable from 8/16/32-bit
  Multi-byte transfer enabled (by software)
  DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)
- A/D converter (successive approximation type)
  10-bit resolution: 24 channels
  Conversion time: minimum 1 µs
- External interrupt inputs : 14 channels
  8 channels shared with CAN RX or I2C pins
- Bit search module (for REALOS)
  Function to search from the MSB (most significant bit) for the position of the first “0”, “1”, or changed bit in a word
- LIN-USART (full duplex double buffer): 5 channels
  Clock synchronous/asynchronous selectable
  Sync-break detection
  Internal dedicated baud rate generator
- I^2C* bus interface (supports 400 kbps): 3 channels
  Master/slave transmission and reception
  Arbitration function, clock synchronization function
- CAN controller (C-CAN): 3 channels
  Maximum transfer speed: 1 Mbps
  32 transmission/reception message buffers
- ? Stepper motor controller : 6 channels
  4 high current output to each channel
  2 synchronized PWMs per channel (8/10-bit)
- ? Sound generator : 1 channel
  Tone frequency : PWM frequency divide-by-two (reload value + 1)
- ? Alarm comparator : 1 channel
  Monitor external voltage
  Generate an interrupt in case of voltage lower/higher than the defined thresholds (reference voltage)
- 16-bit PPG timer : 12 channels
- ? 16-bit PFM timer : 1 channel
- 16-bit reload timer: 8 channels
- 16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)
- Input capture: 8 channels (operates in conjunction with the free-run timer)
- Output compare: 4 channels (operates in conjunction with the free-run timer)
- Up/Down counter: 3 channels (3*8-bit or 1*16-bit + 1*8-bit)
- Watchdog timer

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PRELIMINARY

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- Real-time clock
- Low-power consumption modes : Sleep/stop mode function

? Low voltage detection circuit

? Clock supervisor

Monitors the sub-clock (32 kHz) and the main clock (4 MHz) , and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.

? Clock modulator

? Clock monitor

? Sub-clock calibration

Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator

? Main oscillator stabilization timer

Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter

? Sub-oscillator stabilization timer

Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

3. Package and technology

- Package : QFP-208
- CMOS 0.18 μm technology
- Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
- Operating temperature range: between − 40˚C and + 105˚C

Note * Purchase of Fujitsu I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system provided that the system conforms to the I²C Standard Specification as defined by Philips.

PRELIMINARY

■ PRODUCT LINEUP

Feature	MB91V460A	MB91F465DA	MB91F467DA MB91F467DB
Max. core frequency (CLKB)	80MHz	100MHz	96MHz
Max. resource frequency (CLKP)	40MHz	50MHz	48MHz
Max. external bus freq. (CLKT)	40MHz	50MHz	48MHz
Max. CAN frequency (CLKCAN)	20MHz	50MHz	48MHz
Max. FlexRay frequency (SCLK)	-	-	-
Technology	0.35um	0.18um	0.18um
Watchdog	yes	yes	yes
Watchdog (RC osc. based)	yes (disengageable)	yes	yes
Bit Search	yes	yes	yes
Reset input (INITX)	yes	yes	yes
Hardware Standby input (HSTX)	yes	no	no
Clock Modulator	yes	yes	yes
Clock Monitor	yes	yes	yes
Low Power Mode	yes	yes	yes
DMA	5 ch	5 ch	5 ch
MAC (uDSP)	no	no	no
MMU/MPU	MPU (16 ch) [1)]	MPU (8 ch) [1)]	MPU (8 ch) [1)]
Flash	Emulation SRAM 32bit read data	544 KByte	1088 KByte
Satellite Flash	-	no	no
Flash Protection	-	yes	yes
D-RAM	64 KByte	32 KByte	32 KByte
ID-RAM	64 KByte	16 KByte	32 KByte
Flash-Cache (Instruction cache)	16 KByte	8 KByte	8 KByte
Boot-ROM / BI-ROM	4 KByte fixed	4 KByte	4 KByte
RTC	1 ch	1 ch	1 ch
Free Running Timer	8 ch	8 ch	8 ch
ICU	8 ch	8 ch	8 ch
OCU	8 ch	4 ch	4 ch
Reload Timer	8 ch	8 ch	8 ch
PPG 16-bit	16 ch	12 ch	12 ch
PFM 16-bit	1 ch	1 ch	1 ch
Sound Generator	1 ch	1 ch	1 ch
Up/Down Counter (8/16-bit)	4 ch (8-bit) / 2 ch (16-bit)	3 ch (8-bit) / 1 ch (16-bit)	3 ch (8-bit) / 1 ch (16-bit)
C_CAN	6 ch (128msg)	3 ch (32msg)	3 ch (32msg)
LIN-USART	4 ch + 4 ch FIFO + 8 ch	1 ch + 4 ch FIFO	1 ch + 4 ch FIFO
I2C (400k)	4 ch	3 ch	3 ch
FR external bus	yes (32bit addr, 32bit data)	yes (26bit addr, 32bit data)	yes (26bit addr, 32bit data)

PRELIMINARY

Feature	MB91V460A	MB91F465DA	MB91F467DA MB91F467DB
External Interrupts	16 ch	14 ch	14 ch
NMI Interrupts	1 ch	-	-
SMC	6 ch	6 ch	6 ch
LCD controller (40x4)	1 ch	-	-
ADC (10 bit)	32 ch	24 ch	24 ch
Alarm Comparator	2 ch	1 ch	1 ch
Supply Supervisor	yes	yes	yes
Clock Supervisor	yes	yes	yes
Main clock oscillator	4MHz	4MHz	4MHz
Sub clock oscillator	32kHz	32kHz	32kHz
RC Oscillator	100kHz	100kHz / 2MHz	100kHz / 2MHz
PLL	x 20	x 25	x 24
DSU4	yes	-	-
EDSU	yes (32 BP) *1	yes (16 BP) *1	yes (16 BP) *1
Supply Voltage	3V / 5V	3V / 5V	3V / 5V
Regulator	yes	yes	yes
Power Consumption	n.a.	< 1 W	< 1 W
Temperatur Range (Ta)	0..70 C	-40..105 C	-40..105 C
Package	BGA660	QFP208	QFP208
Power on to PLL run	< 20 ms	< 20 ms	< 20 ms
Flash Download Time	n.a.	< 5 sec. typical	< 6 sec typical

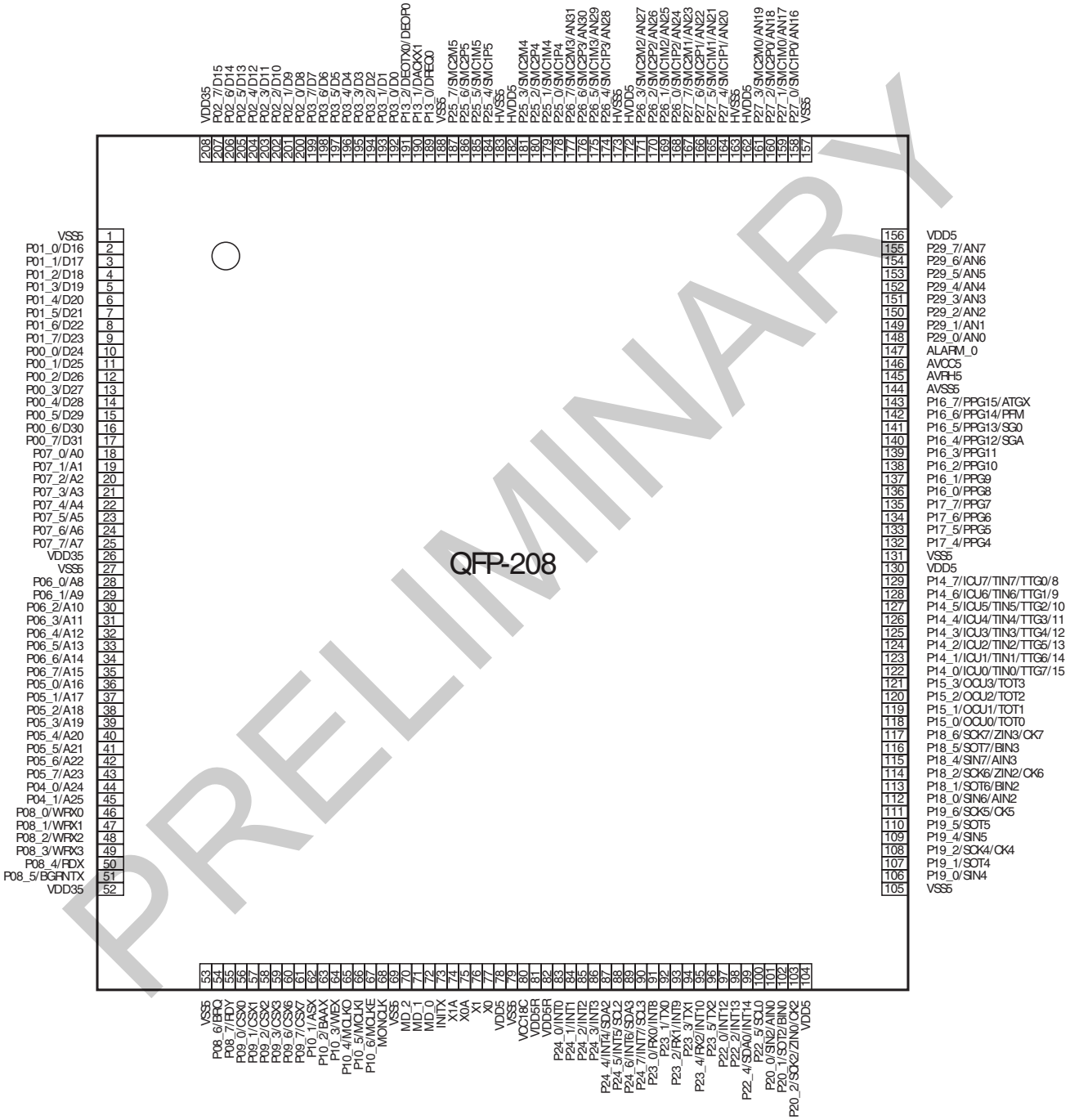
*1 : MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

PRELIMINARY

■ PIN ASSIGNMENT

1. MB91F465DA, MB91F467Dx

(TOP VIEW)



FPT-208P-M04

PRELIMINARY

■ PIN DESCRIPTION

1. MB91F465DA, MB91F467Dx

Pin no.	Pin name	I/O	I/O circuit type*	Function
2 to 9	P01_0 to P01_7	I/O	A	General-purpose input/output ports
	D16 to D23			Signal pins of external data bus (bit16 to bit23)
10 to 17	P00_0 to P00_7	I/O	A	General-purpose input/output ports
	D24 to D31			Signal pins of external data bus (bit24 to bit31)
18 to 25	P07_0 to P07_7	I/O	A	General-purpose input/output ports
	A0 to A7			Signal pins of external address bus (bit0 to bit7)
28 to 35	P06_0 to P06_7	I/O	A	General-purpose input/output ports
	A8 to A15			Signal pins of external address bus (bit8 to bit15)
36 to 43	P05_0 to P05_7	I/O	A	General-purpose input/output ports
	A16 to A23			Signal pins of external address bus (bit16 to bit23)
44, 45	P04_0, P04_1	I/O	A	General-purpose input/output ports
	A24, A25			Signal pins of external address bus (bit24, bit25)
46 to 49	P08_0 to P08_3	I/O	A	General-purpose input/output ports
	WRX0 to WRX3			External write strobe output pins
50	P08_4	I/O	A	General-purpose input/output port
	RDX			External read strobe output pin
51	P08_5	I/O	A	General-purpose input/output port
	BGRNTX			External bus release reception output pin
54	P08_6	I/O	A	General-purpose input/output port
	BRQ			External bus release request input pin
55	P08_7	I/O	A	General-purpose input/output port
	RDY			External ready input pin
56 to 59	P09_0 to P09_3	I/O	A	General-purpose input/output ports
	CSX0 to CSX3			Chip select output pins
60, 61	P09_6, P09_7	I/O	A	General-purpose input/output ports
	CSX6, CSX7			Chip select output pins
62	P10_1	I/O	A	General-purpose input/output port
	ASX			Address strobe output pin
63	P10_2	I/O	A	General-purpose input/output port
	BAAX			Burst address advance output pin
64	P10_3 WEX	I/O	A	General-purpose input/output port Write enable output pin
65	P10_4	I/O	A	General-purpose input/output port
	MCLKO			Clock output pin for memory

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PRELIMINARY

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Pin no.	Pin name	I/O	I/O circuit type*	Function
66	P10_5	I/O	A	General-purpose input/output port
	MCLKI			Clock input pin for memory
67	P10_6	I/O	A	General-purpose input/output port
	MCLKE			Clock enable signal pin for memory
68	MONCLK	O	M	Clock monitor pin
70	MD_2	I	G	Mode setting pins
71	MD_1	I	G	
72	MD_0	I	G	
73	INITX	I	H	External reset input pin
74	X1A	—	J2	Sub clock (oscillation) output
75	X0A	—	J2	Sub clock (oscillation) input
76	X1	—	J1	Clock (oscillation) output
77	X0	—	J1	Clock (oscillation) input
83 to 86	P24_0 to P24_3	I/O	A	General-purpose input/output ports
	INT0 to INT3			External interrupt input pins
87	P24_4	I/O	C	General-purpose input/output port
	INT4			External interrupt input pin
	SDA2			I^2C bus DATA input/output pin
88	P24_5	I/O	C	General-purpose input/output port
	INT5			External interrupt input pin
	SCL2			I^2C bus clock input/output pin
89	P24_6	I/O	C	General-purpose input/output port
	INT6			External interrupt input pin
	SDA3			I^2C bus DATA input/output pin
90	P24_7	I/O	C	General-purpose input/output port
	INT7			External interrupt input pin
	SCL3			I^2C bus clock input/output pin
91	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input/output pin of CAN0
	INT8			External interrupt input pin
92	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0
93	P23_2	I/O	A	General-purpose input/output port
	RX1			RX input/output pin of CAN1
	INT9			External interrupt input pin

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PRELIMINARY

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Pin no.	Pin name	I/O	I/O circuit type*	Function
94	P23_3	I/O	A	General-purpose input/output port
	TX1			TX output pin of CAN1
95	P23_4	I/O	A	General-purpose input/output port
	RX2			RX input/output pin of CAN2
	INT10			External interrupt input pin
96	P23_5	I/O	A	General-purpose input/output port
	TX2			TX output pin of CAN2
97	P22_0	I/O	A	General-purpose input/output port
	INT12			External interrupt input pin
98	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
99	P22_4	I/O	C	General-purpose input/output port
	SDA0			I^2C bus data input/output pin
	INT14			External interrupt input pin
100	P22_5	I/O	C	General-purpose input/output port
	SCL0			I^2C bus clock input/output pin
101	P20_0	I/O	A	General-purpose input/output port
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
102	P20_1	I/O	A	General-purpose input/output port
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
103	P20_2	I/O	A	General-purpose input/output port
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2
106	P19_0	I/O	A	General-purpose input/output port
	SIN4			Data input pin of USART4
107	P19_1	I/O	A	General-purpose input/output port
	SOT4			Data output pin of USART4
108	P19_2	I/O	A	General-purpose input/output port
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4

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PRELIMINARY

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Pin no.	Pin name	I/O	I/O circuit type*	Function
109	P19_4	I/O	A	General-purpose input/output port
	SIN5			Data input pin of USART5
110	P19_5	I/O	A	General-purpose input/output port
	SOT5			Data output pin of USART5
111	P19_6	I/O	A	General-purpose input/output port
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
112	P18_0	I/O	A	General-purpose input/output port
	SIN6			Data input pin of USART6
	AIN2			Up/down counter input pin
113	P18_1	I/O	A	General-purpose input/output port
	SOT6			Data output pin of USART6
	BIN2			Up/down counter input pin
114	P18_2	I/O	A	General-purpose input/output port
	SCK6			Clock input/output pin of USART6
	ZIN2			Up/down counter input pin
	CK6			External clock input pin of free-run timer 6
115	P18_4	I/O	A	General-purpose input/output port
	SIN7			Data input pin of USART7
	AIN3			Up/down counter input pin
116	P18_5	I/O	A	General-purpose input/output port
	SOT7			Data output pin of USART7
	BIN3			Up/down counter input pin
117	P18_6	I/O	A	General-purpose input/output port
	SCK7			Clock input/output pin of USART7
	ZIN3			Up/down counter input pin
	CK7			External clock input pin of free-run timer 7
118 to 121	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
122 to 129	P14_0 to P14_7	I/O	A	General-purpose input/output ports
	ICU0 to ICU7			Input capture input pins
	TIN0 to TIN7			External trigger input pins of reload timer
	TTG4/12 to TTG7/15, TTG8 to TTG11			External trigger input pins of PPG timer

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PRELIMINARY

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Pin no.	Pin name	I/O	I/O circuit type*	Function
132 to 135	P17_4 to P17_7	I/O	A	General-purpose input/output ports
	PPG4 to PPG7			Output pins of PPG timer
136 to 139	P16_0 to P16_3	I/O	A	General-purpose input/output ports
	PPG8 to PPG11			PPG timer output pins
140	P16_4	I/O	A	General-purpose input/output port
	PPG12			Output pin of PPG timer
	SGA			SGA output pin of sound generator
141	P16_5	I/O	A	General-purpose input/output port
	PPG13			Output pin of PPG timer
	SG0			SG0 output pin of sound generator
142	P16_6	I/O	A	General-purpose input/output port
	PPG14			Output pin of PPG timer
	PFM			Pulse frequency modulator output pin
143	P16_7	I/O	A	General-purpose input/output port
	PPG15			PPG timer output pin
	ATGX			A/D converter external trigger input pin
147	ALARM_0	I	N	Alarm comparator input pin
148 to 155	P29_0 to P29_7	I/O	B	General-purpose input/output ports
	AN0 to AN7			Analog input pins of A/D converter
158	P27_0	I/O	F	General-purpose input/output port
	SMC1P0			Controller output pin of Stepper motor
	AN16			Analog input pin of A/D converter
159	P27_1	I/O	F	General-purpose input/output port
	SMC1M0			Controller output pin of Stepper motor
	AN17			Analog input pin of A/D converter
160	P27_2	I/O	F	General-purpose input/output port
	SMC2P0			Controller output pin of Stepper motor
	AN18			Analog input pin of A/D converter
161	P27_3	I/O	F	General-purpose input/output port
	SMC2M0			Controller output pin of Stepper motor
	AN19			Analog input pin of A/D converter
164	P27_4	I/O	F	General-purpose input/output port
	SMC1P1			Controller output pin of Stepper motor
	AN20			Analog input pin of A/D converter

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PRELIMINARY

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Pin no.	Pin name	I/O	I/O circuit type*	Function
165	P27_5	I/O	F	General-purpose input/output port
	SMC1M1			Controller output pin of Stepper motor
	AN21			Analog input pin of A/D converter
166	P27_6	I/O	F	General-purpose input/output port
	SMC2P1			Controller output pin of Stepper motor
	AN22			Analog input pin of A/D converter
167	P27_7	I/O	F	General-purpose input/output port
	SMC2M1			Controller output pin of Stepper motor
	AN23			Analog input pin of A/D converter
168	P26_0	I/O	F	General-purpose input/output port
	SMC1P2			Controller output pin of Stepper motor
	AN24			Analog input pin of A/D converter
169	P26_1	I/O	F	General-purpose input/output port
	SMC1M2			Controller output pin of Stepper motor
	AN25			Analog input pin of A/D converter
170	P26_2	I/O	F	General-purpose input/output port
	SMC2P2			Controller output pin of Stepper motor
	AN26			Analog input pin of A/D converter
171	P26_3	I/O	F	General-purpose input/output port
	SMC2M2			Controller output pin of Stepper motor
	AN27			Analog input pin of A/D converter
174	P26_4	I/O	F	General-purpose input/output port
	SMC1P3			Controller output pin of Stepper motor
	AN28			Analog input pin of A/D converter
175	P26_5	I/O	F	General-purpose input/output port
	SMC1M3			Controller output pin of Stepper motor
	AN29			Analog input pin of A/D converter
176	P26_6	I/O	F	General-purpose input/output port
	SMC2P3			Controller output pin of Stepper motor
	AN30			Analog input pin of A/D converter
177	P26_7	I/O	F	General-purpose input/output port
	SMC2M3			Controller output pin of Stepper motor
	AN31			Analog input pin of A/D converter

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PRELIMINARY

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Pin no.	Pin name	I/O	I/O circuit type*	Function
178	P25_0	I/O	E	General-purpose input/output port
	SMC1P4			Controller output pin of Stepper motor
179	P25_1	I/O	E	General-purpose input/output port
	SMC1M4			Controller output pin of Stepper motor
180	P25_2	I/O	E	General-purpose input/output port
	SMC2P4			Controller output pin of Stepper motor
181	P25_3	I/O	E	General-purpose input/output port
	SMC2M4			Controller output pin of Stepper motor
184	P25_4	I/O	E	General-purpose input/output port
	SMC1P5			Controller output pin of Stepper motor
185	P25_5	I/O	E	General-purpose input/output port
	SMC1M5			Controller output pin of Stepper motor
186	P25_6	I/O	E	General-purpose input/output port
	SMC2P5			Controller output pin of Stepper motor
187	P25_7	I/O	E	General-purpose input/output port
	SMC2M5			Controller output pin of Stepper motor
189	P13_0	I/O	A	General-purpose input/output port
	DREQ0			DMA external transfer request input
190	P13_1	I/O	A	General-purpose input/output port
	DACKX1			DMA external transfer acknowledge output pin
191	P13_2	I/O	A	General-purpose input/output port
	DEOTX0			DMA external transfer EOT (End of Track) output pin
	DEOP0			DMA external transfer EOP (End of Process) output pin
192 to 199	P03_0 to P03_7	I/O	A	General-purpose input/output ports
	D0 to D7			Signal pins of external data bus (bit0 to bit7)
200 to 207	P02_0 to P02_7	I/O	A	General-purpose input/output ports
	D8 to D15			Signal pins of external data bus (bit8 to bit15)

* : For information about the I/O circuit type, refer to “■ I/O CIRCUIT TYPES”.

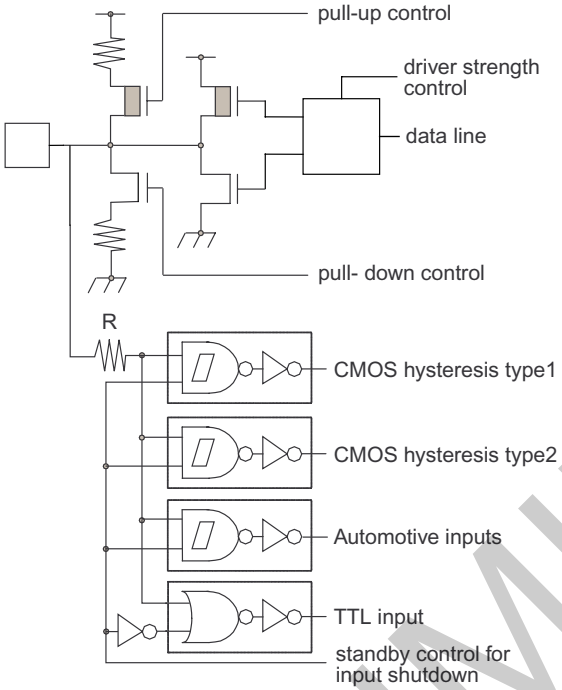
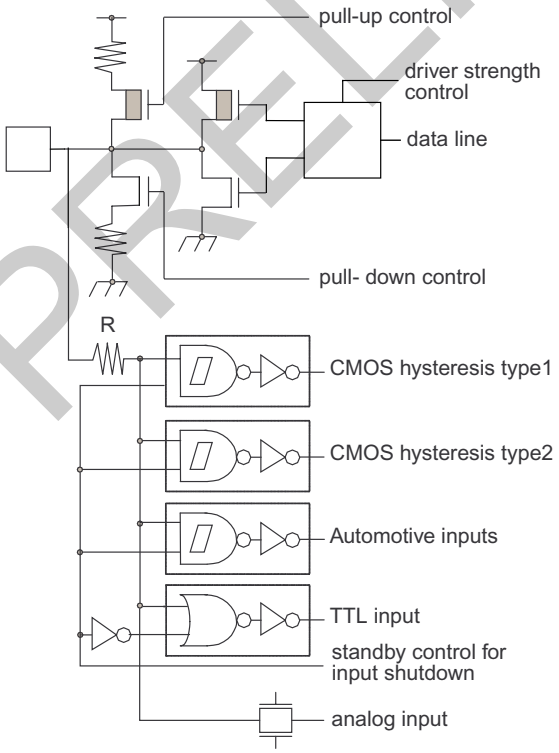
PRELIMINARY

[Power supply/Ground pins]

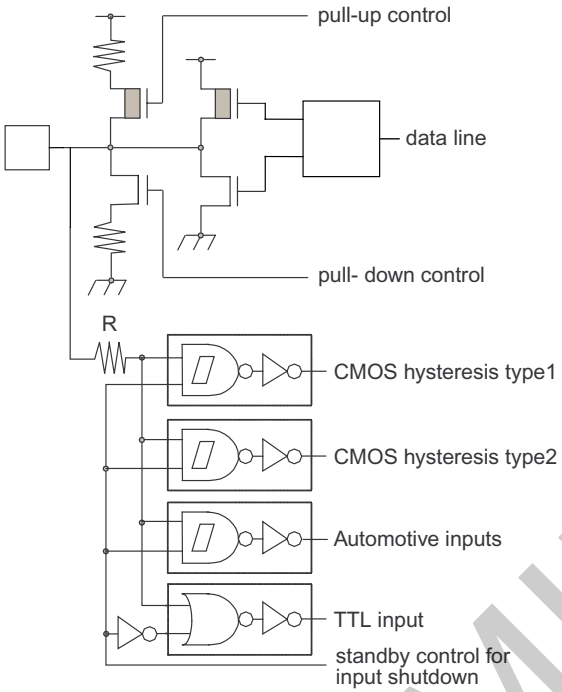
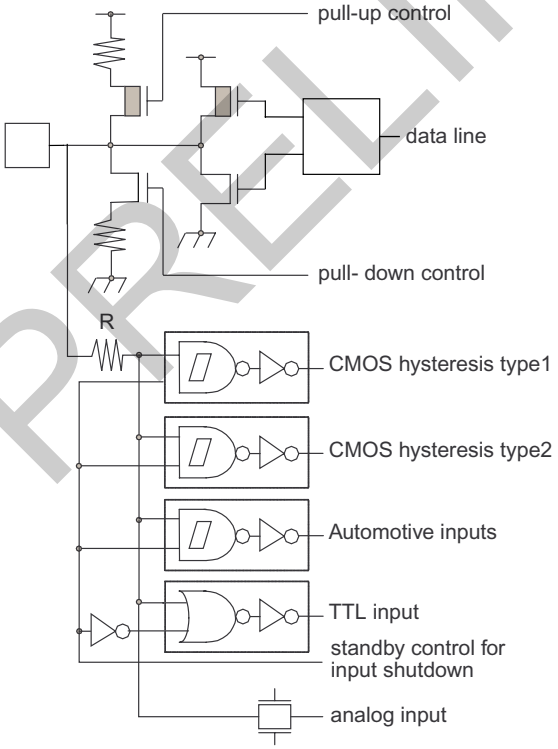
Pin no.	Pin name	I/O	Function
1, 27, 53, 69, 79, 105, 131, 157, 188	VSS5	Supply	Ground pins
163, 173, 183	HVSS5		Ground pins for Stepper motor controller
26, 52	VDD35		Power supply pins for external data bus
78, 104, 130, 156	VDD5		Power supply pins
162, 172, 182	HVDD5		Power supply pins for Stepper motor controller
81, 82	VDD5R		Power supply pins for internal regulator
144	AVSS5		Analog ground pin for A/D converter
146	AVCC5		Power supply pin for A/D converter
145	AVRH5		Reference power supply pin for A/D converter
80	VCC18C		Capacitor connection pin for internal regulator

PRELIMINARY

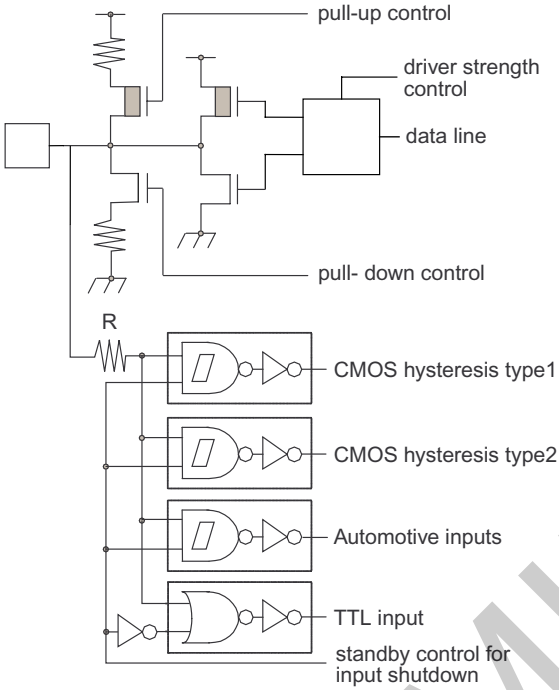
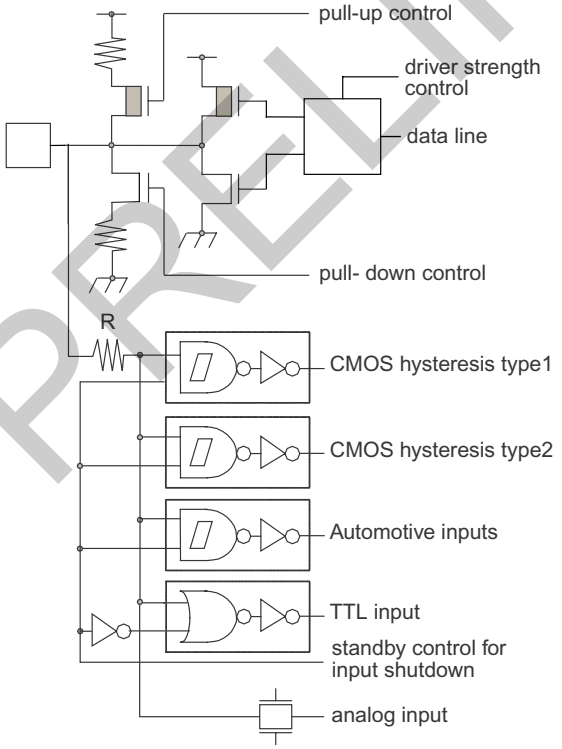
■ I/O CIRCUIT TYPES

Type	Circuit	Remarks
A		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
B		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function) TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

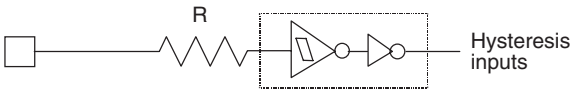
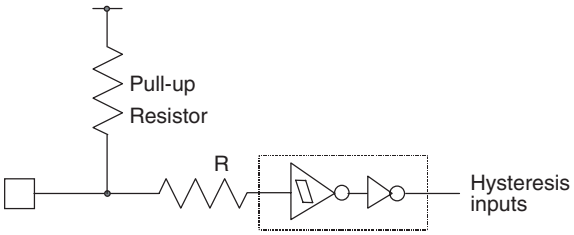
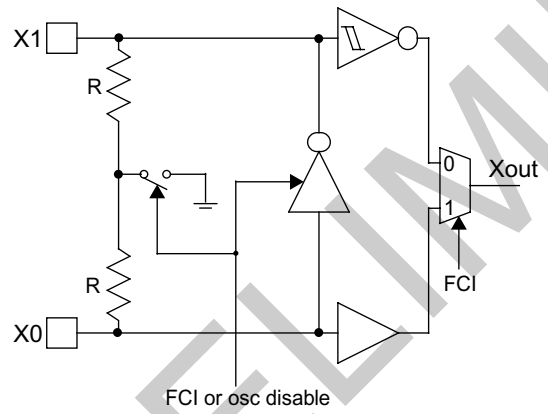
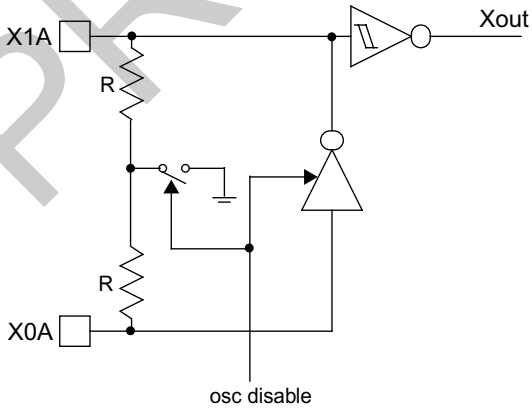
PRELIMINARY

Type	Circuit	Remarks
C		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
D		CMOS level output (I_{OL} = 3mA, I_{OH} = -3mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

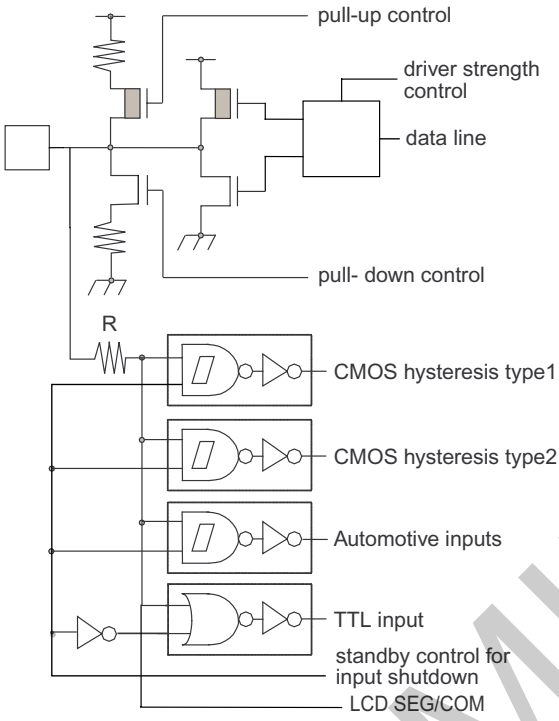
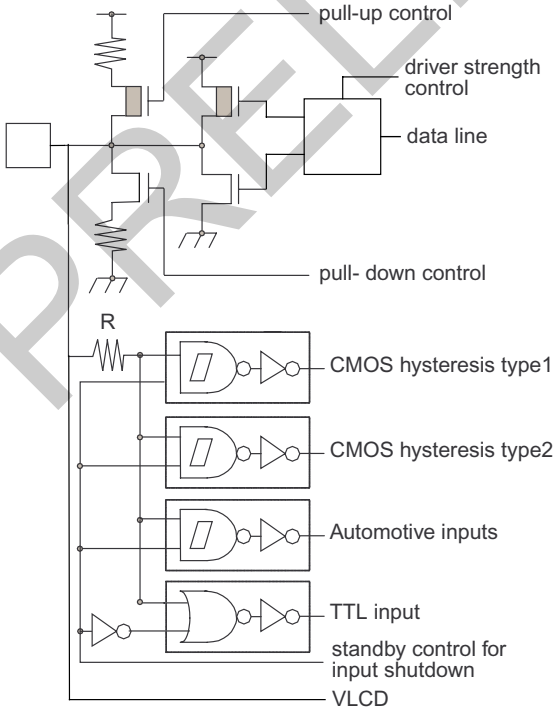
PRELIMINARY

Type	Circuit	Remarks
E		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx.
F		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input

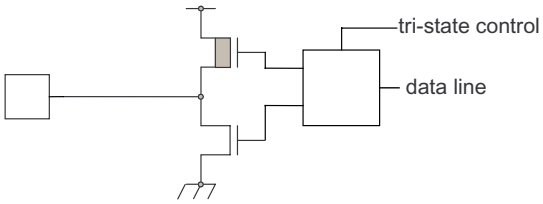
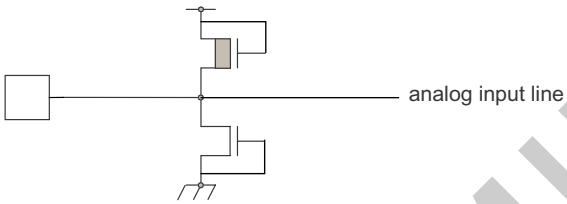
PRELIMINARY

Type	Circuit	Remarks
G		Mask ROM and EVA device: CMOS Hysteresis input pin Flash device: CMOS input pin 12 V withstand (for MD [2:0])
H		CMOS Hysteresis input pin Pull-up resistor value: 50 kΩ approx.
J1		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 2 * 0.5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled or in FCI mode.
J2		Low-speed oscillation circuit: • Feedback resistor = approx. 2 * 5 MΩ. Feedback resistor is grounded in the center when the oscillator is disabled.

PRELIMINARY

Type	Circuit	Remarks
K		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. LCD SEG/COM output
L		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function) TTL input with input shutdown function Programmable pull-up resistor: 50kΩ approx. Analog input LCD Voltage input

PRELIMINARY

Type	Circuit	Remarks
M		CMOS level tri-state output (I_{OL} = 5mA, I_{OH} = -5mA)
N		Analog input pin with protection

PRELIMINARY

■ HANDLING DEVICES

1. Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ($V_{DD}5$, $V_{DD}35$ or $HV_{DD}5$) or less than ($V_{SS}5$ or $HV_{SS}5$) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

2. Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2KΩ to 10KΩ) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to $V_{SS}5$ or $V_{DD}5$ directly. Unused ALARM input pins can be connected to $AV_{SS}5$ directly.

3. Power supply pins

In MB91460D series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460D series must be connected to the current supply source via a low impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 μF as a bypass capacitor between power supply pin and ground pin near this device.
This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 μF (use a X7R ceramic capacitator) to VCC18C pin for the regulator.

4. Crystal oscillator circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

5. Notes on using external clock

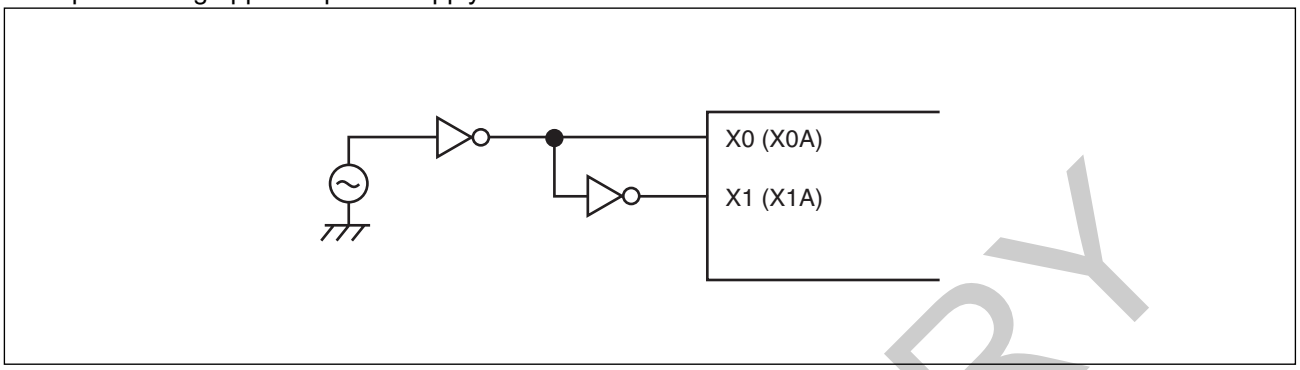
When using the external clock, it is necessary to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination, X1 (X1A) should be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. At X0 and X1, a frequency up to 16 MHz is possible.

(Continued)

PRELIMINARY

(Continued)

Example of using opposite phase supply



PRELIMINARY

6. Mode pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

7. Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

8. Pull-up control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

9. Notes on PS register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.
As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

1) The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:
   (a) a user interrupt or NMI is accepted; (b) single-step execution is performed; or (c) execution breaks due to a data event or from the emulator menu.
   -D0 and D1 flags are updated in advance.
   -An EIT handling routine (user interrupt/NMI or emulator) is executed.
   -Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1).
2) The following behavior occurs when an ORCCR, STILM, MOV Ri or PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.
   -The PS register is updated in advance.
   -An EIT handling routine (user interrupt/NMI or emulator) is executed.
   - Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1).

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■ NOTES ON DEBUGGER

1. Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

2. Break function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

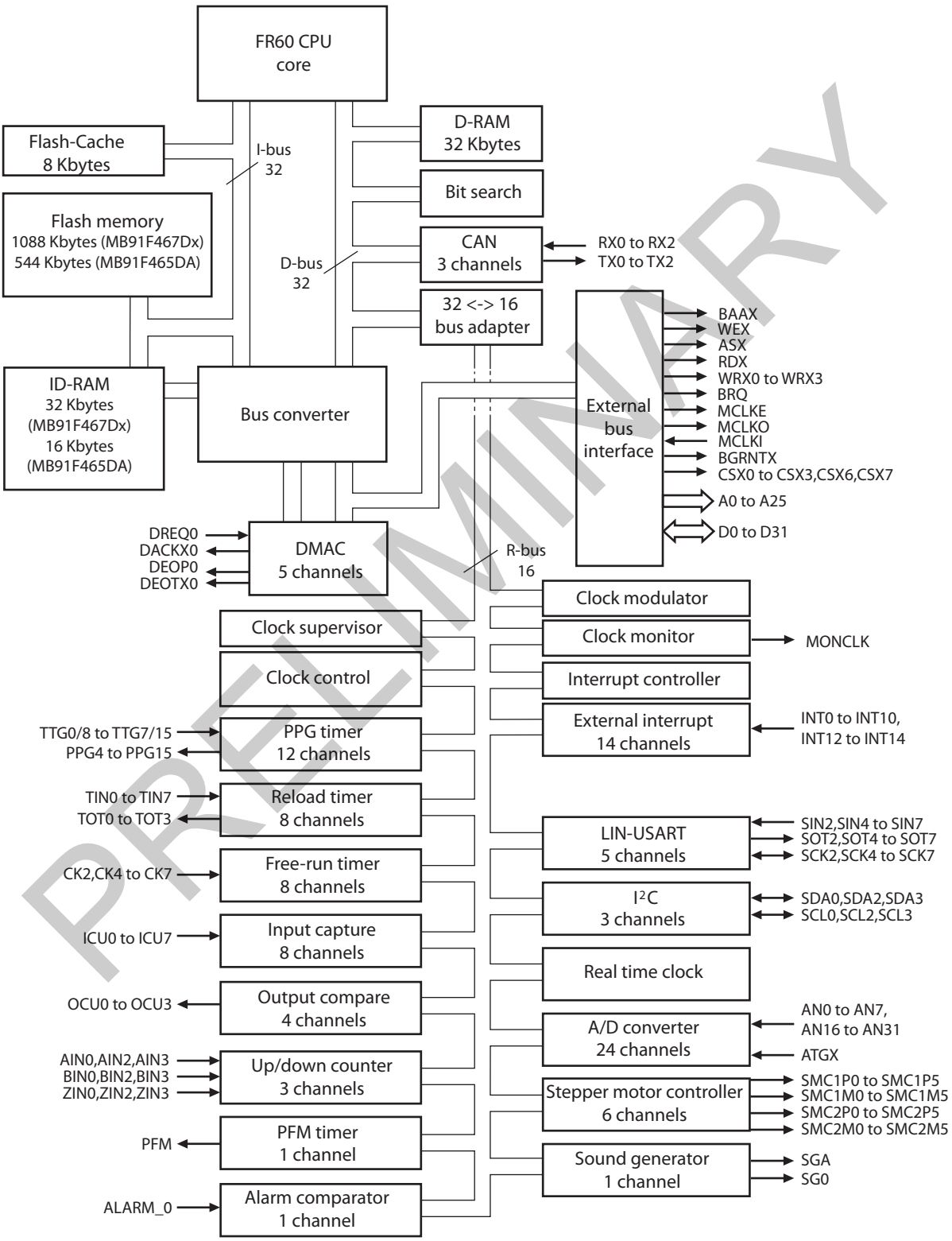
3. Operand break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

PRELIMINARY

■ BLOCK DIAGRAM

1. MB91F465DA, MB91F467Dx



PRELIMINARY

■ CPU AND CONTROL UNIT

The FR family CPU is a high performance core that is designed based on the RISC architecture with advanced instructions for embedded applications.

1. Features

- Adoption of RISC architecture
  Basic instruction: 1 instruction per cycle
- General-purpose registers: 32-bit 16 registers
- 4 Gbytes linear memory space
- Multiplier installed
  32-bit 32-bit multiplication: 5 cycles
  16-bit 16-bit multiplication: 3 cycles
- Enhanced interrupt processing function
  Quick response speed (6 cycles)
  Multiple-interrupt support
  Level mask function (16 levels)
- Enhanced instructions for I/O operation
  Memory-to-memory transfer instruction
  Bit processing instruction
  Basic instruction word length: 16 bits
- Low-power consumption
  Sleep mode/stop mode

2. Internal architecture

- The FR family CPU uses the Harvard architecture in which the instruction bus and data bus are independent of each other.
- A 32-bit ↔ 16-bit buffer is connected to the 32-bit bus (D-bus) to provide an interface between the CPU and peripheral resources.
- A Harvard ↔ Princeton bus converter is connected to both the I-bus and D-bus to provide an interface between the CPU and the bus controller.

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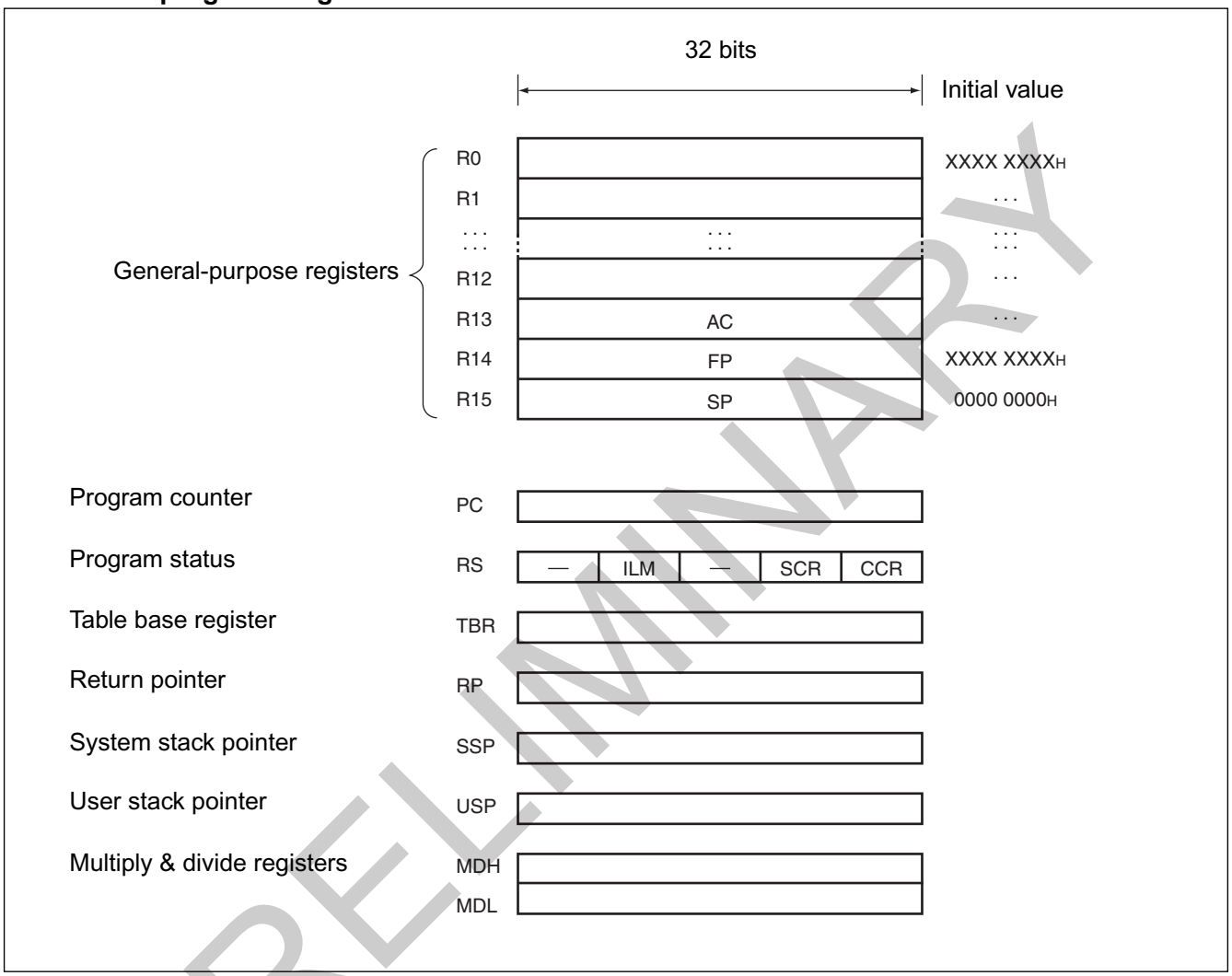
3. Programming model

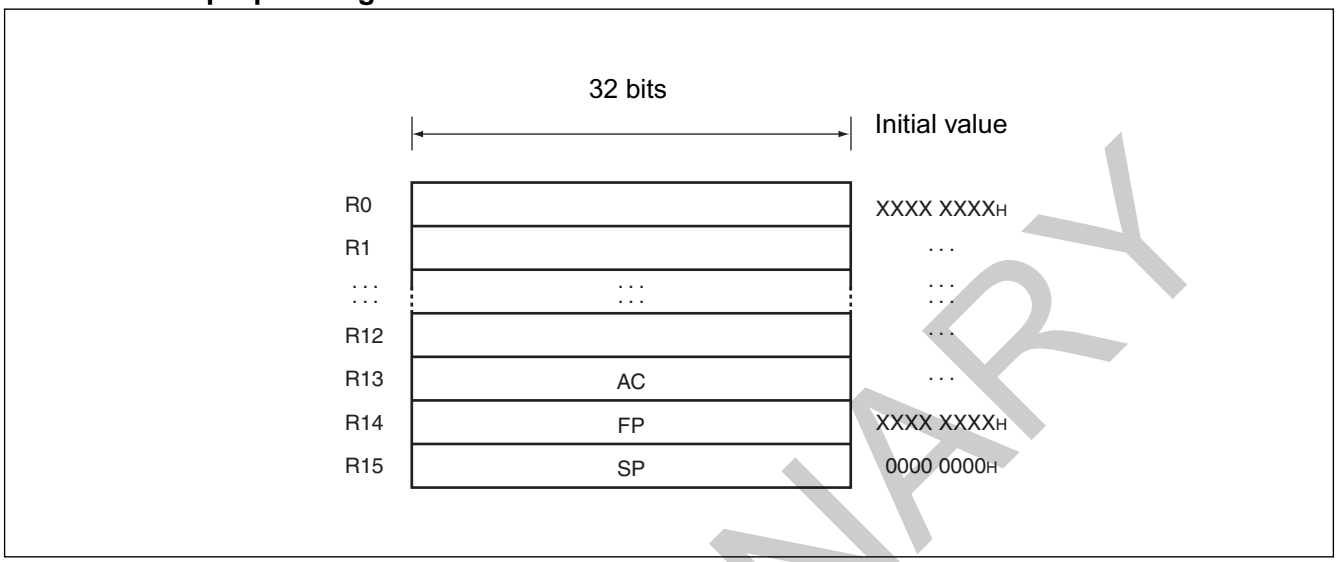
3.1. Basic programming model



PRELIMINARY

4. Registers

4.1. General-purpose register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

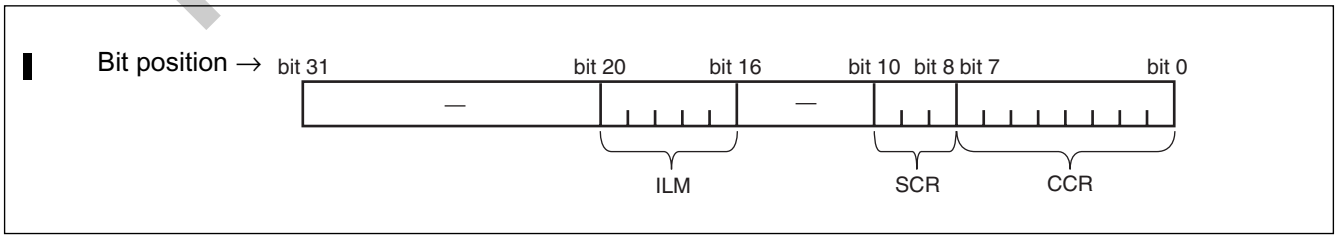
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000H (SSP value).

4.2. PS (Program Status)

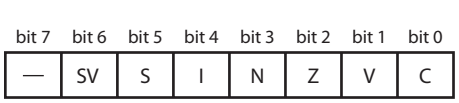
This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always “0”. Write access to these bits is invalid.



PRELIMINARY

4.3. CCR (Condition Code Register)

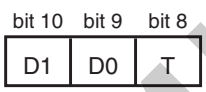


Initial value

- 000XXXX$_B$

SV : Supervisor flag
S : Stack flag
I : Interrupt enable flag
N : Negative enable flag
Z : Zero flag
V : Overflow flag
C : Carry flag

4.4. SCR (System Condition Register)



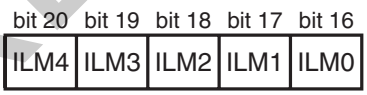
Initial value

XX0$_B$

Flag for step division (D1, D0)
This flag stores interim data during execution of step division.

Step trace trap flag (T)
This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

4.5. ILM (Interrupt Level Mask register)



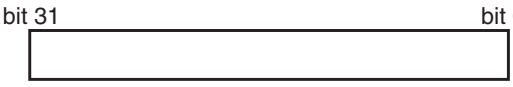
Initial value

01111$_B$

This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value “01111$_B$” at reset.

4.6. PC (Program Counter)



Initial value

XXXXXXXX$_H$

The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

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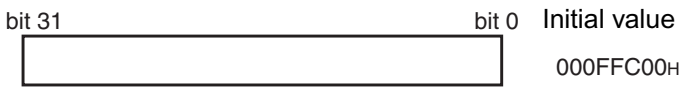
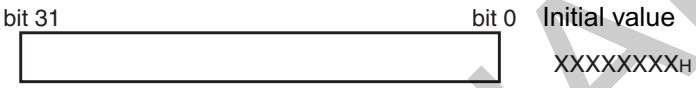
4.7. TBR (Table Base Register)



The table base register stores the starting address of the vector table used in EIT processing.

The initial value at reset is 000FFC00H.

4.8. RP (Return Pointer)



The return pointer stores the address for return from subroutines.

During execution of a CALL instruction, the PC value is transferred to this RP register.

During execution of a RET instruction, the contents of the RP register are transferred to PC.

The initial value at reset is undefined.

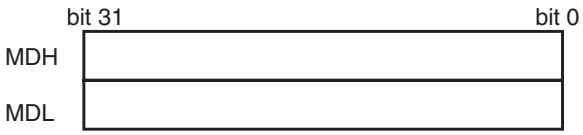
4.9. USP (User Stack Pointer)

The user stack pointer, when the S flag is “1”, this register functions as the R15 register.

- The USP register can also be explicitly specified.

  The initial value at reset is undefined.
- This register cannot be used with RETI instructions.

4.10. Multiply & divide registers



These registers are for multiplication and division, and are each 32 bits in length.

The initial value at reset is undefined.

PRELIMINARY

■ EMBEDDED PROGRAM/DATA MEMORY (FLASH)

1. Flash features

- MB91F467Dx: 1088 Kbytes (16 × 64 Kbytes + 8 × 8 Kbytes = 8.5 Mbits)
- MB91F465DA: 544 Kbytes (8 × 64 Kbytes + 4 × 8 Kbytes = 4.25 Mbits)
- Programmable wait state for read/write access
- Flash and Boot security with security vector at 0x0014:8000 - 0x0014:800F
- Boot security
- Basic specification: Same as MBM29LV400TC (except size and part of sector configuration)

2. Operation modes

(1) 64-bit CPU mode (available on MB91F467Dx only) :

- CPU reads and executes programs in word (32-bit) length units.
- Flash writing is not possible.
- Actual Flash Memory access is performed in d-word (64-bit) length units.

(2) 32-bit CPU mode :

- MB91F465DA: CPU reads and executes programs in word (32-bit) length units.
  MB91F467Dx: CPU reads, writes and executes programs in word (32-bit) length units.
- Actual Flash Memory access is performed in word (32-bit) length units.

(3) 16-bit CPU mode :

- CPU reads and writes in half-word (16-bit) length units.
- Program execution from the Flash is not possible.
- Actual Flash Memory access is performed in half-word (16-bit) length units.

PRELIMINARY

3. Flash access in CPU mode

3.1. Flash configuration

3.1.1. Flash memory map MB91F467Dx

Address									
0014:FFFFh 0014:C000h	SA6 (8kB)				SA7 (8kB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8kB)				SA5 (8kB)				
0014:7FFFh 0014:4000h	SA2 (8kB)				SA3 (8kB)				
0014:3FFFh 0014:0000h	SA0 (8kB)				SA1 (8kB)				
0013:FFFFh 0012:0000h	SA22 (64kB)				SA23 (64kB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64kB)				SA21 (64kB)				
000F:FFFFh 000E:0000h	SA18 (64kB)				SA19 (64kB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64kB)				SA17 (64kB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64kB)				SA15 (64kB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64kB)				SA13 (64kB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64kB)				SA11 (64kB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64kB)				SA9 (64kB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read/write	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

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3.1.2. Flash memory map MB91F465DA

Addr									
0014:FFFFh 0014:C000h	SA6 (8kB)				SA7 (8kB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8kB)				SA5 (8kB)				
0014:7FFFh 0014:4000h	SA2 (8kB)				SA3 (8kB)				
0014:3FFFh 0014:0000h	SA0 (8kB)				SA1 (8kB)				
0013:FFFFh 0012:0000h	SA22 (64kB)				SA23 (64kB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64kB)				SA21 (64kB)				
000F:FFFFh 000E:0000h	SA18 (64kB)				SA19 (64kB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64kB)				SA17 (64kB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64kB)				SA15 (64kB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64kB)				SA13 (64kB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64kB)				SA11 (64kB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64kB)				SA9 (64kB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read	dat[31:0]				dat[31:0]				

Legend	Memory not available in this area	Memory available in this area

PRELIMINARY

3.2. Flash access timing settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

3.2.1. Flash read timing settings (synchronous read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	-	1	
to 48 MHz	0	0	1	-	2	
to 96 MHz	1	1	3	-	4	
to 100 MHz	1	1	3	-	4	not available on MB91F467Dx

3.2.2. Flash write timing settings (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 32 MHz	1	-	-	0	4	
to 48 MHz	1	-	-	0	5	
to 64 MHz	1	-	-	0	6	
to 96 MHz	1	-	-	0	7	
to 100 MHz	1	-	-	0	7	not available on MB91F467Dx

PRELIMINARY

3.3. Address mapping from CPU to parallel programming mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

3.3.1. Address mapping MB91F467Dx

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:0000h to 14:FFFFh	addr[2]==0	SA0, SA2, SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h
14:0000h to 14:FFFFh	addr[2]==1	SA1, SA3, SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h + 00:2000h
04:0000h to 13:FFFFh	addr[2]==0	SA8, SA10, SA12, SA14, SA16, SA18, SA20, SA22 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h
04:0000h to 13:FFFFh	addr[2]==1	SA9, SA11, SA13, SA15, SA17, SA19, SA21, SA23 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h + 01:0000h

Note: FA result is without 20:0000h offset for parallel Flash programming .
Set offset by keeping FA[21] = 1 as described in section “Parallel Flash programming mode”.

3.3.2. Address mapping MB91F465DA

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:8000h to 14:FFFFh	addr[2]==0	SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h
14:8000h to 14:FFFFh	addr[2]==1	SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 0D:0000h + 00:2000h
08:0000h to 0F:FFFFh	addr[2]==0	SA12, SA14, SA16, SA18 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 00:0000h
08:0000h to 0F:FFFFh	addr[2]==1	SA13, SA15, SA17, SA19 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 - 00:0000h + 01:0000h

Note: FA result is without 10:0000h offset for parallel Flash programming .
Set offset by keeping FA[20] = 1 as described in section “Parallel Flash programming mode”.

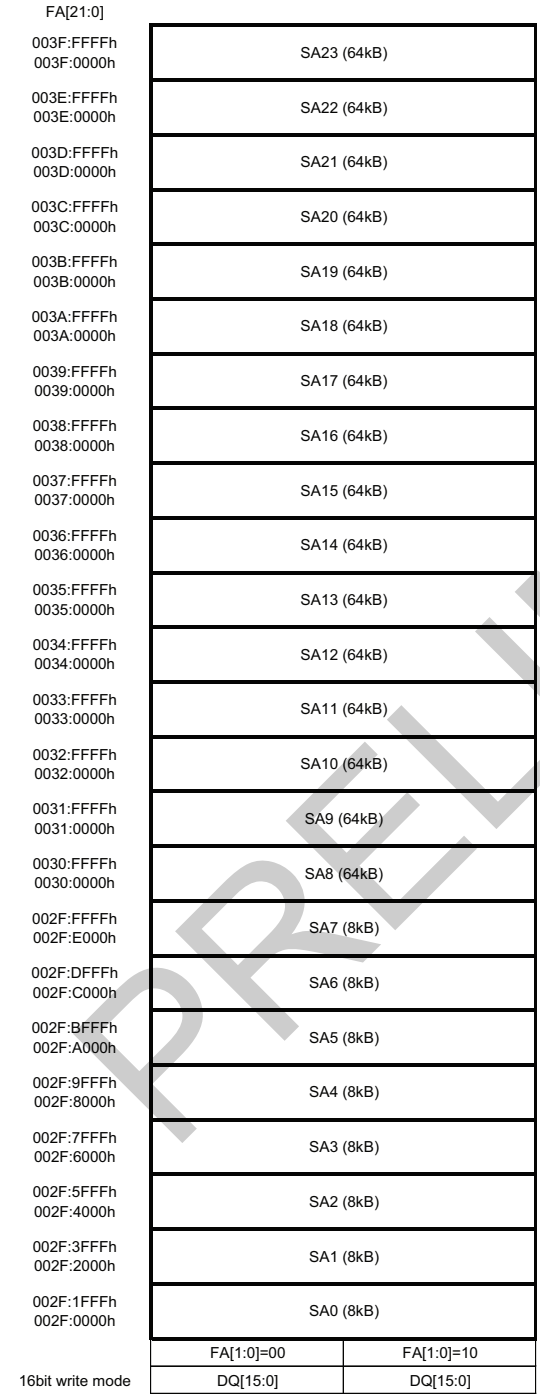
PRELIMINARY

4. Parallel Flash programming mode

4.1. Flash configuration in parallel Flash programming mode

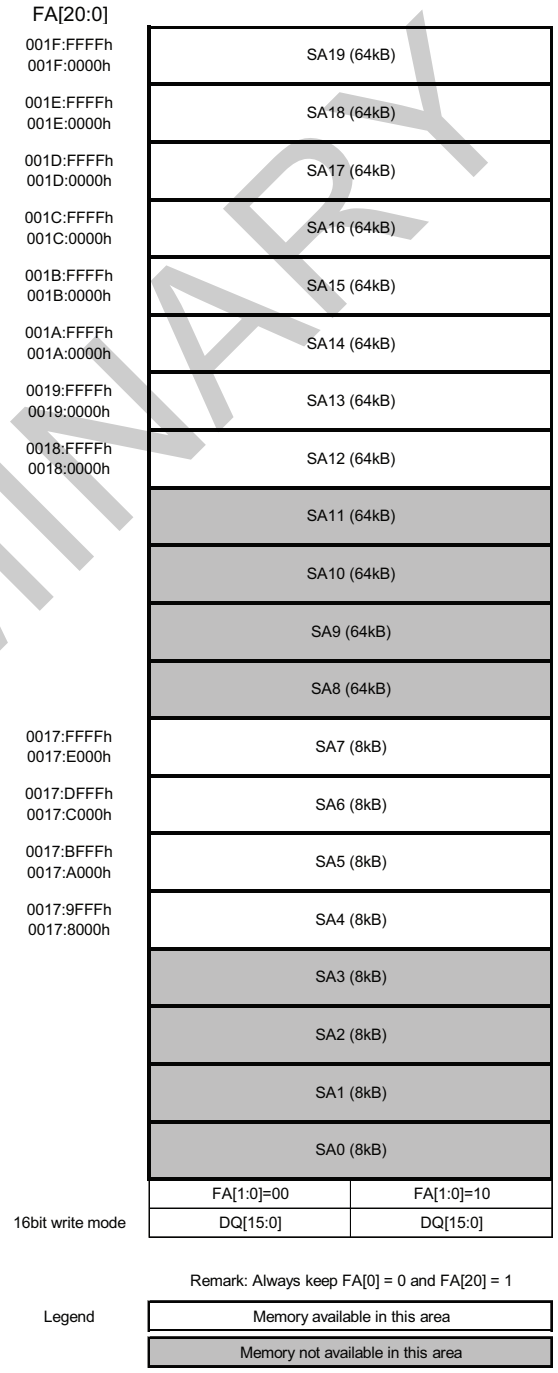
Parallel Flash programming mode (MD[2:0] = 111):

MB91F467Dx



Remark: Always keep FA[0] = 0 and FA[21] = 1

MB91F465DA



PRELIMINARY

4.2. Pin connections in parallel programming mode

Resetting after setting the MD[2:0] pins to [111] will halt CPU functioning. At this time, the Flash memory's interface circuit enables direct control of the Flash memory unit from external pins by directly linking some of the signals to General Purpose Ports. Please see table below for signal mapping.

In this mode, the Flash memory appears to the external pins as a stand-alone unit. This mode is generally set when writing/erasing using the parallel Flash programmer. In this mode, all operations of the 8.5 Mbits Flash memory's Auto Algorithms are available.

Correspondence between MBM29LV400TC and Flash Memory Control Signals

MBM29LV400TC External pins	FR-CPU mode	**MB91F465DA, MB91F467Dx** external pins			Comment
		Flash memory mode	Normal function	Pin number	
—	INITX	—	INITX	73	
RESET	—	FRSTX	P09_6	60	
—	—	MD_2	MD_2	70	
—	—	MD_1	MD_1	71	
—	—	MD_0	MD_0	72	
RY/BY	FMCS:RDY bit	RY/BYX	P09_0	56	
BYTE	Internally fixed to 'H'	BYTEX	P09_2	58	
WE	Internal control signal + control via interface circuit	WEX	P13_2	191	
OE		OEX	P13_1	190	
CE		CEX	P13_0	189	
—		ATDIN	P25_7	187	
—		EQIN	P25_6	186	
—		TESTX	P09_3	59	
—		RDYI	P09_1	57	
A-1	Internal address bus	FA0	P25_5	185	
A0 to A3		FA1 to FA4	P27_0 to P27_3	158 to 161	
A4 to A7		FA5 to FA8	P27_4 to P27_7	164 to 167	
A8 to A11		FA9 to FA12	P26_0 to P26_3	168 to 171	
A12 to A15		FA13 to FA16	P26_4 to P26_7	174 to 177	
A16 to A19		FA17 to FA20	P25_0 to P25_3	178 to 181	
—		FA21	P25_4	184	Not needed on MB91F465DA
DQ0 to DQ7	Internal data bus	DQ0 to DQ7	P03_0 to P03_7	192 to 199	
DQ8 to DQ15		DQ8 to DQ15	P02_0 to P02_7	200 to 207	

PRELIMINARY

5. Flash Security

5.1. Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004
FSV2: 0x14:8008 BSV2: 0x14:800C

5.2. Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 Kbytes sectors.

5.2.1. FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1 [31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to “0”	set to “0”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “0”	set to “1”	set to “0”	Write Protection (all device modes, without exception)
set all to “0”	set to “0”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”) and Write Protection (all device modes)
set all to “0”	set to “1”	set to “0”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “1”	set to “1”	set to “0”	Write Protection (all device modes, except INTVEC mode MD[2:0] = “000”)
set all to “0”	set to “1”	set to “1”	set to “1”	Read Protection (all device modes, except INTVEC mode MD[2:0] = “000”) and Write Protection (all device modes except INTVEC mode MD[2:0] = “000”)

PRELIMINARY

5.2.2. FSV1 (bit15 to bit0)

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 Kbytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1 [15:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	SA0 (MB91F467Dx) SA4 (MB91F465DA)	set to “0”	set to “1” —	On MB91F465DA, write protection is mandatory!
FSV1[1]	SA1 (MB91F467Dx) SA5 (MB91F465DA)	set to “0”	set to “1”	
FSV1[2]	SA2 (MB91F467Dx) SA6 (MB91F465DA)	set to “0”	set to “1”	
FSV1[3]	SA3 (MB91F467Dx) SA7 (MB91F465DA)	set to “0”	set to “1”	
FSV1[4]	SA4 (MB91F467Dx)	set to “0”	—	Write protection is mandatory!
FSV1[5]	SA5 (MB91F467Dx)	set to “0”	set to “1”	
FSV1[6]	SA6 (MB91F467Dx)	set to “0”	set to “1”	
FSV1[7]	SA7 (MB91F467Dx)	set to “0”	set to “1”	
FSV1[8]	—	set to “0”	set to “1”	not available
FSV1[9]	—	set to “0”	set to “1”	not available
FSV1[10]	—	set to “0”	set to “1”	not available
FSV1[11]	—	set to “0”	set to “1”	not available
FSV1[12]	—	set to “0”	set to “1”	not available
FSV1[13]	—	set to “0”	set to “1”	not available
FSV1[14]	—	set to “0”	set to “1”	not available
FSV1[15]	—	set to “0”	set to “1”	not available

Note : It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.
See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

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5.3. Security Vector FSV2

The setting of the Flash Security Vector FSV2 bits [31:0] is responsible for the individual write protection of the 64 Kbytes sectors. It is only evaluated if write protection bit FSV1 [17] is set.

Explanation of the bits in the Flash Security Vector FSV2[31:0]

FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV2[0]	SA8 (MB91F467Dx) SA12 (MB91F465DA)	set to “0”	set to “1”	
FSV2[1]	SA9 (MB91F467Dx) SA13 (MB91F465DA)	set to “0”	set to “1”	
FSV2[2]	SA10 (MB91F467Dx) SA14 (MB91F465DA)	set to “0”	set to “1”	
FSV2[3]	SA11 (MB91F467Dx) SA15 (MB91F465DA)	set to “0”	set to “1”	
FSV2[4]	SA12 (MB91F467Dx) SA16 (MB91F465DA)	set to “0”	set to “1”	
FSV2[5]	SA13 (MB91F467Dx) SA17 (MB91F465DA)	set to “0”	set to “1”	
FSV2[6]	SA14 (MB91F467Dx) SA18 (MB91F465DA)	set to “0”	set to “1”	
FSV2[7]	SA15 (MB91F467Dx) SA19 (MB91F465DA)	set to “0”	set to “1”	
FSV2[8]	SA16 (MB91F467Dx)	set to “0”	set to “1”	
FSV2[9]	SA17 (MB91F467Dx)	set to “0”	set to “1”	
FSV2[10]	SA18 (MB91F467Dx)	set to “0”	set to “1”	
FSV2[11]	SA19 (MB91F467Dx)	set to “0”	set to “1”	
FSV2[12]	SA20 (MB91F467Dx)	set to “0”	set to “1”	
FSV2[13]	SA21 (MB91F467Dx)	set to “0”	set to “1”	
FSV2[14]	SA22 (MB91F467Dx)	set to “0”	set to “1”	
FSV2[15]	SA23 (MB91F467Dx)	set to “0”	set to “1”	
FSV2[31:16]	—	set to “0”	set to “1”	not available

Note : See section “Flash access in CPU mode” for an overview about the sector organisation of the Flash Memory.

PRELIMINARY

■ MEMORY SPACE

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

- Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access : 000_H to $0FF_H$

Half word access : 000_H to $1FF_H$

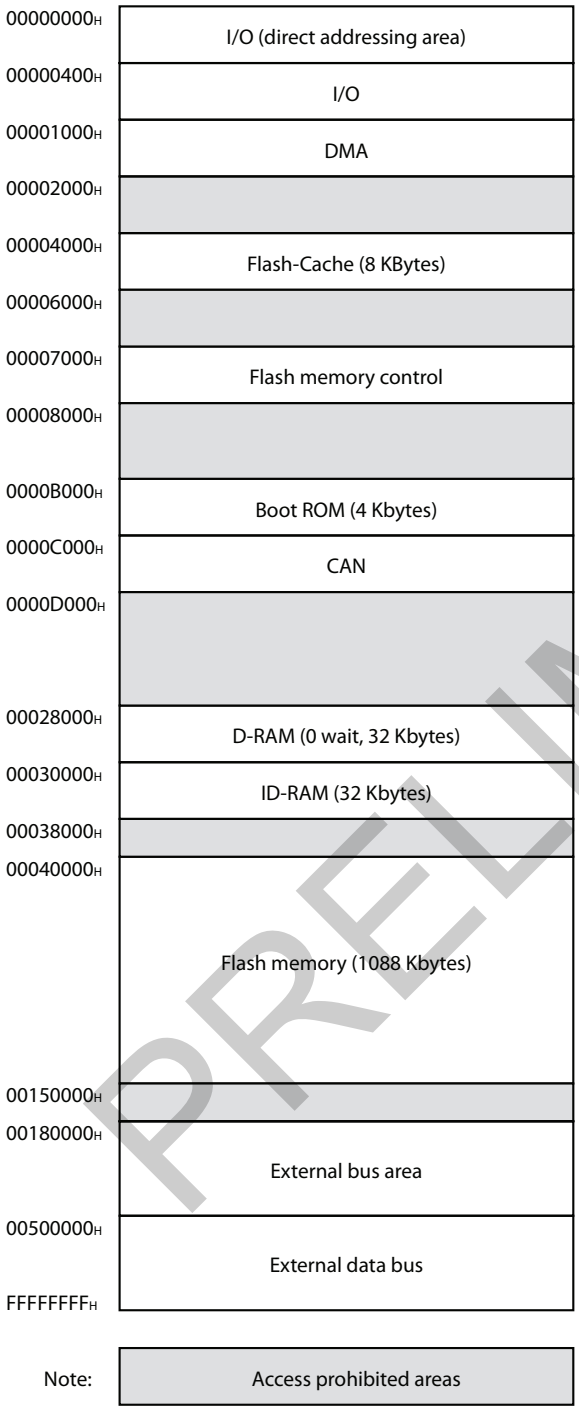
Word data access : 000_H to $3FF_H$

PRELIMINARY

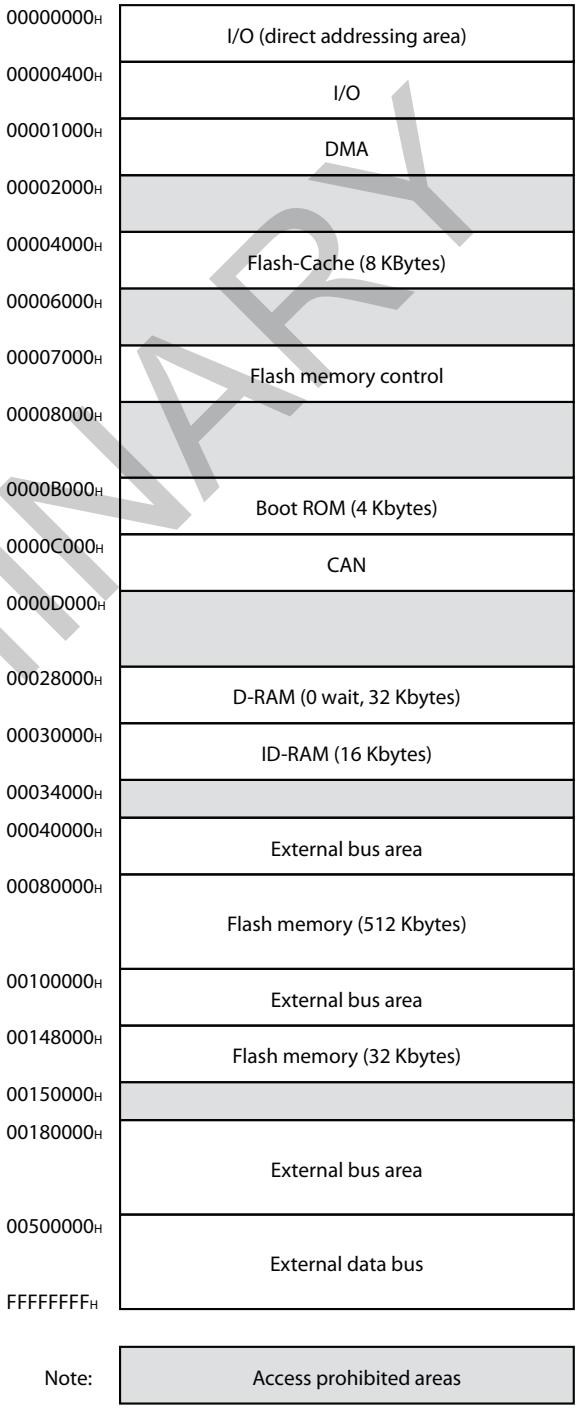
■ MEMORY MAPS

1. MB91F465DA, MB91F467Dx

MB91F467Dx



MB91F465DA

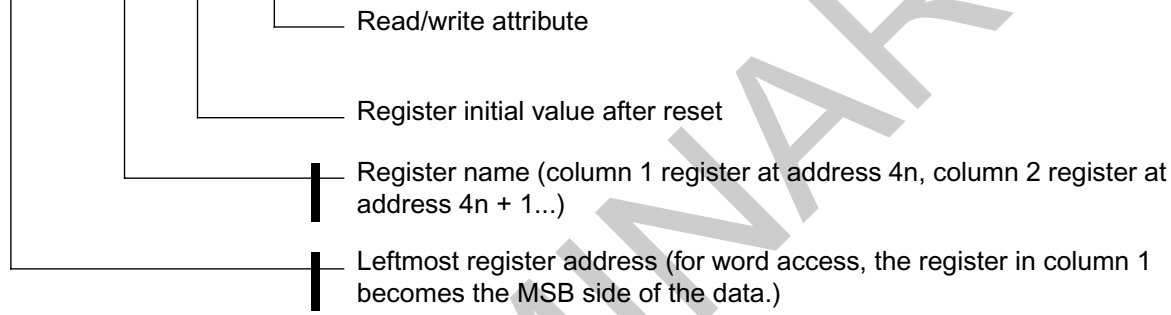


PRELIMINARY

■ I/O MAP

1. MB91F465DA, MB91F467Dx

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note : Initial values of register bits are represented as follows:
- " 1 " : Initial value " 1 "
- " 0 " : Initial value " 0 "
- " X " : Initial value " undefined "
- " - " : No physical register at this location

Access is barred with an undefined data access attribute.

PRELIMINARY

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	PDR02 [R/W] XXXXXXXX	PDR03 [R/W] XXXXXXXX	R-bus Port Data Register
000004H	PDR04 [R/W] - - - - - - XX	PDR05 [R/W] XXXXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008H	PDR08 [R/W] XXXXXXXX	PDR09 [R/W] XX - - XXXX	PDR10 [R/W] - XXXXXX -	Reserved	
00000CH	Reserved	PDR13 [R/W] - - - - - XXX	PDR14 [R/W] XXXXXXXX	PDR15 [R/W] - - - - XXXX	
000010H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXX - - - -	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014H	PDR20 [R/W] - - - - - XXX	Reserved	PDR22 [R/W] - - XX - X - X	PDR23 [R/W] - - XXXXXX	
000018H	PDR24 [R/W] XXXXXXXX	PDR25 [R/W] XXXXXXXX	PDR26 [R/W] XXXXXXXX	PDR27 [R/W] XXXXXXXX	
00001CH	Reserved	PDR29 [R/W] XXXXXXXX	Reserved		
000020H to 00002CH	Reserved				Reserved
000030H	EIRR0 [R/W] XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt (INT 0 to INT 7)
000034H	EIRR1 [R/W] XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt (INT 8 to INT 10, INT 12 to INT 14)
000038H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	Reserved		Delay Interrupt
00003CH to 00004CH	Reserved				Reserved
000050H	SCR02 [R/W, W] 00000000	SMR02 [R/W, W] 00000000	SSR02 [R/W, R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054H	ESCR02 [R/W] 00000X00	ECCR02 [R/W, R, W] -00000XX	Reserved		
000058H, 00005CH	Reserved				Reserved

(Continued)

PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000060H	SCR04 [R/W, W] 00000000	SMR04 [R/W, W] 00000000	SSR04 [R/W, R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064H	ESCR04 [R/W] 00000X00	ECCR04 [R/W, R, W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068H	SCR05 [R/W, W] 00000000	SMR05 [R/W, W] 00000000	SSR05 [R/W, R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
00006CH	ESCR05 [R/W] 00000X00	ECCR05 [R/W, R, W] -00000XX	FSR05 [R] - - - 00000	FCR05 [R/W] 0001 - 000	
000070H	SCR06 [R/W, W] 00000000	SMR06 [R/W, W] 00000000	SSR06 [R/W, R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074H	ESCR06 [R/W] 00000X00	ECCR06 [R/W, R, W] -00000XX	FSR06 [R] - - - 00000	FCR06 [R/W] 0001 - 000	
000078H	SCR07 [R/W, W] 00000000	SMR07 [R/W, W] 00000000	SSR07 [R/W, R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
00007CH	ESCR07 [R/W] 00000X00	ECCR07 [R/W, R, W] -00000XX	FSR07 [R] - - - 00000	FCR07 [R/W] 0001 - 000	
000080H	Reserved				Reserved
000084H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	Reserved		Baud rate Generator LIN-USART 2,4 to 7
000088H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
00008CH	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090H	PWC20 [R/W] - - - - - - XX XXXXXXXX		PWC10 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 0
000094H	Reserved		PWS20 [R/W] -0000000	PWS10 [R/W] - -000000	
000098H	PWC21 [R/W] - - - - - - XX XXXXXXXX		PWC11 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 1
00009CH	Reserved		PWS21 [R/W] -0000000	PWS11 [R/W] - -000000	

(Continued)

PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000A0H	PWC22 [R/W] - - - - - - XX XXXXXXXX		PWC12 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 2
0000A4H	Reserved		PWS22 [R/W] -0000000	PWS12 [R/W] - -000000	
0000A8H	PWC23 [R/W] - - - - - - XX XXXXXXXX		PWC13 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 3
0000ACH	Reserved		PWS23 [R/W] -0000000	PWS13 [R/W] - -000000	
0000B0H	PWC24 [R/W] - - - - - - XX XXXXXXXX		PWC14 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 4
0000B4H	Reserved		PWS24 [R/W] -0000000	PWS14 [R/W] - -000000	
0000B8H	PWC25 [R/W] - - - - - - XX XXXXXXXX		PWC15 [R/W] - - - - - - XX XXXXXXXX		Stepper Motor 5
0000BCH	Reserved		PWS25 [R/W] -0000000	PWS15 [R/W] - -000000	
0000C0H	Reserved	PWC0 [R/W] -00000--	Reserved	PWC1 [R/W] -00000--	Stepper Motor Control 0 to 5
0000C4H	Reserved	PWC2 [R/W] -00000--	Reserved	PWC3 [R/W] -00000--	
0000C8H	Reserved	PWC4 [R/W] -00000--	Reserved	PWC5 [R/W] -00000--	
0000CCH	Reserved				Reserved
0000D0H	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - - 00	ITBAL0 [R/W] 00000000	I²C 0
0000D4H	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
0000D8H	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] 00011111	Reserved	
0000DCH to 000100H	Reserved				Reserved
000104H	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7
000108H	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8 to 11
000110H to 00012CH	Reserved				Reserved

(Continued)

PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000130H	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134H	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138H	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
00013CH	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	
000140H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
00014CH	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
00015CH	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
00016CH	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170H	P0TMCSRH [R/W] - 0 - 000 - 0	P0TMCSRL [R/W] - - - 00000	P1TMCSRH [R/W] - 0 - 000 - 0	P1TMCSRL [R/W] - - - 00000	PFM
000174H	P0TMRLR [W] XXXXXXXX XXXXXXXX		P0TMR [R] XXXXXXXX XXXXXXXX		
000178H	P1TMRLR [W] XXXXXXXX XXXXXXXX		P1TMR [R] XXXXXXXX XXXXXXXX		
00017CH	Reserved				Reserved

(Continued)

PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000180H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		
00018CH	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
00019CH	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
0001A0H	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
0001A8H	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
0001ACH	Reserved	ACSR0 [R/W] - 11XXX00	Reserved		Alarm Comparator 0
0001B0H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0
0001B4H	Reserved		TMCSRH0 [R/W] - - - 00000	TMCSRL0 [R/W] 0 - 000000	
0001B8H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1
0001BCH	Reserved		TMCSRH1 [R/W] - - - 00000	TMCSRL1 [R/W] 0 - 000000	
0001C0H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4, PPG 5)
0001C4H	Reserved		TMCSRH2 [R/W] - - - 00000	TMCSRL2 [R/W] 0 - 000000	

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PRELIMINARY

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0001C8H	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6, PPG 7)
0001CCH	Reserved		TMCSRH3 [R/W] - - - 00000	TMCSRL3 [R/W] 0 - 000000	
0001D0H	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8, PPG 9)
0001D4H	Reserved		TMCSRH4 [R/W] - - - 00000	TMCSRL4 [R/W] 0 - 000000	
0001D8H	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10, PPG 11)
0001DCH	Reserved		TMCSRH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
0001E0H	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12, PPG 13)
0001E4H	Reserved		TMCSRH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	
0001E8H	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14, PPG 15) (A/D Converter)
0001ECH	Reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
0001F0H	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
0001F4H	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
0001F8H	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU 1)
0001FCH	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU 3)

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PRELIMINARY

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000200H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228H to 00023CH	Reserved				
000240H	DMACR [R/W] 00 - - 0000	Reserved			
000244H to 0002CCH	Reserved				Reserved
0002D0H	Reserved	ICS045 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4 to 7
0002D4H	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
0002D8H	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
0002DCH to 0002ECH	Reserved				Reserved
0002F0H	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4, ICU 5)

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PRELIMINARY

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0002F4H	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6, ICU 7)
0002F8H	TCDT6 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS6 [R/W] 00000000	Free Running Timer 6
0002FCH	TCDT7 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS7 [R/W] 00000000	Free Running Timer 7
000300H	Reserved	UDRC0 [W] 00000000	Reserved	UDCR0 [R] 00000000	Up/Down Counter 0
000304H	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00001000	Reserved	UDCS0 [R/W] 00000000	
000308H, 00030CH	Reserved				Reserved
000310H	UDRC3 [W] 00000000	UDRC2 [W] 00000000	UDCR3 [R] 00000000	UDCR2 [R] 00000000	Up/Down Counter 2 to 3
000314H	UDCCH2 [R/W] 00000000	UDCCL2 [R/W] 00001000	Reserved	UDCS2 [R/W] 00000000	
000318H	UDCCH3 [R/W] 00000000	UDCCL3 [R/W] 00001000	Reserved	UDCS3 [R/W] 00000000	
00031CH	Reserved				Reserved
000320H	GCN13 [R/W] 00110010 00010000		Reserved	GCN23 [R/W] - - - - 0000	PPG Control 12 to 15
000324H to 00032CH	Reserved				Reserved
000330H	PTMR12 [R] 11111111 11111111		PCSR12 [W] XXXXXXXX XXXXXXXX		PPG 12
000334H	PDUT12 [W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338H	PTMR13 [R] 11111111 11111111		PCSR13 [W] XXXXXXXX XXXXXXXX		PPG 13
00033CH	PDUT13 [W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340H	PTMR14 [R] 11111111 11111111		PCSR14 [W] XXXXXXXX XXXXXXXX		PPG 14
000344H	PDUT14 [W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	

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PRELIMINARY

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000348H	PTMR15 [R] 11111111 11111111		PCSR15 [W] XXXXXXXX XXXXXXXX		PPG 15
00034CH	PDUT15 [W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 000000 - 0	
000350H to 000364H	Reserved				Reserved
000368H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH2 [R/W] - - - - - - 00	ITBAL2 [R/W] 00000000	I²C 2
00036CH	ITMKH2 [R/W] 00 - - - - 11	ITMKL2 [R/W] 11111111	ISMK2 [R/W] 01111111	ISBA2 [R/W] - 0000000	
000370H	Reserved	IDAR2 [R/W] 00000000	ICCR2 [R/W] 00011111	Reserved	
000374H	IBCR3 [R/W] 00000000	IBSR3 [R] 00000000	ITBAH3 [R/W] - - - - - - 00	ITBAL3 [R/W] 00000000	I²C 3
000378H	ITMKH3 [R/W] 00 - - - - 11	ITMKL3 [R/W] 11111111	ISMK3 [R/W] 01111111	ISBA3 [R/W] - 0000000	
00037CH	Reserved	IDAR3 [R/W] 00000000	ICCR3 [R/W] 00011111	Reserved	
000380H to 00038CH	Reserved				Reserved
000390H	ROMS [R] 11111111 00000000 (MB91F467Dx) 11111111 01000011 (MB91F465DA)		Reserved		ROM Select Register
000394H to 0003ECH	Reserved				Reserved
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H to 00043CH	Reserved				Reserved

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PRELIMINARY

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000440H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044CH	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045CH	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046CH	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478H	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
00047CH	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	
000480H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXX - 00	CTBR [W] XXXXXXXX	Clock Control
000484H	CLKR [R/W] ---- 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488H	Reserved				Reserved

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PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00048CH	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLMULG [W] 00000000	PLL Interface
000490H	PLLCTRL [R/W] - - - - 0000	Reserved			
000494H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control
000498H	PORTEN [R/W] - - - - - - 00	Reserved			Port Input Enable Control
00049CH	Reserved				Reserved
0004A0H	Reserved	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 - 00 - 0		Real Time Clock (Watch Timer)
0004A4H	Reserved	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
0004A8H	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	Reserved	
0004ACH	CSVTR [R/W] - - - 00010	CSVCR [R/W] 00011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock-Supervisor / Selector / Monitor
0004B0H	CUCR [R/W] - - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration of Sub Clock
0004B4H	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
0004B8H	CMPR [R/W] - - 000010 11111101		Reserved	CMCR [R/W] - 001 - - 00	Clock Modulator
0004BCH	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
0004C0H	CANPRE [R/W] 0 - - - 0000	CANCKD [R/W] - - - - - 000*1	Reserved		CAN Clock Control
0004C4H	LVSEL [R/W] 00000111	LVDET [R/W] 0000 0 - 00	HWWDE [R/W] - - - - - - 00	HWWD [R/W, W] 00011000	Low Voltage Detection/ Hardware Watchdog
0004C8H	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 00 - - - 000	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilisation Timer
0004CCH	OSCCR [R/W] - - - - - - - 0	Reserved	REGSEL [R/W] - - 000100	REGCTR [R/W] - - - 0 - - 00	Main- Oscillation Standby Control Main-/Subregulator Control
0004D0H to 00063CH	Reserved				Reserved

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PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000640H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00100000*2		External Bus
000644H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
00064CH	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
00065CH	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660H	AWR0 [R/W] 01001111 11111011		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
00066CH	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674H	Reserved				
000678H	IORW0 [R/W] XXXXXXXX	IORW1 [R/W] XXXXXXXX	IORW2 [R/W] XXXXXXXX	Reserved	
00067CH	Reserved				
000680H	CSER [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** *3	
000684H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		
000688H to 0007F8H	Reserved				
0007FCH	Reserved	MODR [W] XXXXXXXX	Reserved		Mode Register

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PRELIMINARY

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Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000800H to 000CFCH	Reserved				Reserved
000D00H	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	PDRD02 [R] XXXXXXXX	PDRD03 [R] XXXXXXXX	R-bus Port Data Direct Read Register
000D04H	PDRD04 [R] - - - - - - XX	PDRD05 [R] XXXXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
000D08H	PDRD08 [R] XXXXXXXX	PDRD09 [R] XX - - XXXX	PDRD10 [R] - XXXXXX -	Reserved	
000D0CH	Reserved	PDRD13 [R] - - - - - XXX	PDRD14 [R] XXXXXXXX	PDRD15 [R] - - - - XXXX	
000D10H	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXX - - - -	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
000D14H	PDRD20 [R] - - - - - XXX	Reserved	PDRD22 [R] - - XX - X - X	PDRD23 [R] - - XXXXXX	
000D18H	PDRD24 [R] XXXXXXXX	PDRD25 [R] XXXXXXXX	PDRD26 [R] XXXXXXXX	PDRD27 [R] XXXXXXXX	
000D1CH	Reserved	PDRD29 [R] XXXXXXXX	Reserved		
000D20H to 000D3CH	Reserved				Reserved
000D40H	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	DDR02 [R/W] 00000000	DDR03 [R/W] 00000000	R-bus Port Direction Register
000D44H	DDR04 [R/W] - - - - - - 00	DDR05 [R/W] 00000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
000D48H	DDR08 [R/W] 00000000	DDR09 [R/W] 00 - - 0000	DDR10 [R/W] - 000000 -	Reserved	
000D4CH	Reserved	DDR13 [R/W] - - - - - 000	DDR14 [R/W] 00000000	DDR15 [R/W] - - - - 0000	
000D50H	DDR16 [R/W] 00000000	DDR17 [R/W] 0000 - - - -	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
000D54H	DDR20 [R/W] - - - - - 000	Reserved	DDR22 [R/W] - - 00 - 0 - 0	DDR23 [R/W] - - 000000	
000D58H	DDR24 [R/W] 00000000	DDR25 [R/W] 00000000	DDR26 [R/W] 00000000	DDR27 [R/W] 00000000	
000D5CH	Reserved	DDR29 [R/W] 00000000	Reserved		
000D60H to 000D7CH	Reserved				Reserved

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PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000D80H	PFR00 [R/W] 11111111	PFR01 [R/W] 11111111	PFR02 [R/W] 11111111	PFR03 [R/W] 11111111	R-bus Port Function Register
000D84H	PFR04 [R/W] - - - - - - 11	PFR05 [R/W] 11111111	PFR06 [R/W] 11111111	PFR07 [R/W] 11111111	
000D88H	PFR08 [R/W] 11111111	PFR09 [R/W] 11 - - 1111	PFR10 [R/W] - 111111 -	Reserved	
000D8CH	Reserved	PFR13 [R/W] - - - - - 000	PFR14 [R/W] 00000000	PFR15 [R/W] - - - - 0000	
000D90H	PFR16 [R/W] 00000000	PFR17 [R/W] 0000 - - - -	PFR18 [R/W] - 000 - 000	PFR19 [R/W] - 000 - 000	
000D94H	PFR20 [R/W] - - - - - 000	Reserved	PFR22 [R/W] - - 00 - 0 - 0	PFR23 [R/W] - - 000000	
000D98H	PFR24 [R/W] 00000000	PFR25 [R/W] 00000000	PFR26 [R/W] 00000000	PFR27 [R/W] 00000000	
000D9CH	Reserved	PFR29 [R/W] 00000000	Reserved		
000DA0H to 000DBCH	Reserved				Reserved
000DC0H	EPFR00 [R/W] - - - - - - - -	EPFR01 [R/W] - - - - - - - -	EPFR02 [R/W] - - - - - - - -	EPFR03 [R/W] - - - - - - - -	R-bus Extra Port Function Register
000DC4H	EPFR04 [R/W] - - - - - - - -	EPFR05 [R/W] - - - - - - - -	EPFR06 [R/W] - - - - - - - -	EPFR07 [R/W] - - - - - - - -	
000DC8H	EPFR08 [R/W] - - - - - - - -	EPFR09 [R/W] - - - - - - - -	EPFR10 [R/W] - - 00 - - - -	Reserved	
000DCCH	Reserved	EPFR13 [R/W] - - - - - 0 - -	EPFR14 [R/W] 00000000	EPFR15 [R/W] - - - - 0000	
000DD0H	EPFR16 [R/W] 0000 - - - -	EPFR17 [R/W] - - - - - - - -	EPFR18 [R/W] - 00 - - 00 -	EPFR19 [R/W] - 0 - - - 0 - -	
000DD4H	EPFR20 [R/W] - - - - - 00 -	Reserved	EPFR22 [R/W] - - - - - - - -	EPFR23 [R/W] - - - - - - - -	
000DD8H	EPFR24 [R/W] - - - - - - - -	EPFR25 [R/W] - - - - - - - -	EPFR26 [R/W] 00000000	EPFR27 [R/W] 00000000	
000DDCH	Reserved	EPFR29 [R/W] - - - - - - - -	Reserved		
000DE0H to 000DFCH	Reserved				Reserved

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PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000E00H	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	PODR02 [R/W] 00000000	PODR03 [R/W] 00000000	R-bus Port Output Drive Select Register
000E04H	PODR04 [R/W] - - - - - - 00	PODR05 [R/W] 00000000	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
000E08H	PODR08 [R/W] 00000000	PODR09 [R/W] 00 - - 0000	PODR10 [R/W] - 000000 -	Reserved	
000E0CH	Reserved	PODR13 [R/W] - - - - - 000	PODR14 [R/W] 00000000	PODR15 [R/W] - - - - 0000	
000E10H	PODR16 [R/W] 00000000	PODR17 [R/W] 0000 - - - -	PODR18 [R/W] - 000 - 000	PODR19 [R/W] - 000 - 000	
000E14H	PODR20 [R/W] - - - - - 000	Reserved	PODR22 [R/W] - - 00 - 0 - 0	PODR23 [R/W] - - 000000	
000E18H	PODR24 [R/W] 00000000	PODR25 [R/W] 00000000	PODR26 [R/W] 00000000	PODR27 [R/W] 00000000	
000E1CH	Reserved	PODR29 [R/W] 00000000	Reserved		
000E20H to 000E3CH	Reserved				Reserved
000E40H	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	PILR02 [R/W] 00000000	PILR03 [R/W] 00000000	R-bus Port Input Level Select Register
000E44H	PILR04 [R/W] - - - - - - 00	PILR05 [R/W] 00000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
000E48H	PILR08 [R/W] 00000000	PILR09 [R/W] 00 - - 0000	PILR10 [R/W] - 000000 -	Reserved	
000E4CH	Reserved	PILR13 [R/W] - - - - - 000	PILR14 [R/W] 00000000	PILR15 [R/W] - - - - 0000	
000E50H	PILR16 [R/W] 00000000	PILR17 [R/W] 0000 - - - -	PILR18 [R/W] - 000 - 000	PILR19 [R/W] - 000 - 000	
000E54H	PILR20 [R/W] - - - - - 000	Reserved	PILR22 [R/W] - - 00 - 0 - 0	PILR23 [R/W] - - 000000	
000E58H	PILR24 [R/W] 00000000	PILR25 [R/W] 00000000	PILR26 [R/W] 00000000	PILR27 [R/W] 00000000	
000E5CH	Reserved	PILR29 [R/W] 00000000	Reserved		
000E60H to 000E7CH	Reserved				Reserved

(Continued)

PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000E80H	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	EPILR02 [R/W] 00000000	EPILR03 [R/W] 00000000	R-bus Extra Port Input Level Select Register
000E84H	EPILR04 [R/W] - - - - - - 00	EPILR05 [R/W] 00000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
000E88H	EPILR08 [R/W] 00000000	EPILR09 [R/W] 00 - - 0000	EPILR10 [R/W] - 000000 -	Reserved	
000E8CH	Reserved	EPILR13 [R/W] - - - - - 000	EPILR14 [R/W] 00000000	EPILR15 [R/W] - - - - 0000	
000E90H	EPILR16 [R/W] 00000000	EPILR17 [R/W] 0000 - - - -	EPILR18 [R/W] - 000 - 000	EPILR19 [R/W] - 000 - 000	
000E94H	EPILR20 [R/W] - - - - - 000	Reserved	EPILR22 [R/W] - - 00 - 0 - 0	EPILR23 [R/W] - - 000000	
000E98H	EPILR24 [R/W] 00000000	EPILR25 [R/W] 00000000	EPILR26 [R/W] 00000000	EPILR27 [R/W] 00000000	
000E9CH	Reserved	EPILR29 [R/W] 00000000	Reserved		
000EA0H to 000EBCH	Reserved				Reserved
000EC0H	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	PPER02 [R/W] 00000000	PPER03 [R/W] 00000000	R-bus Port Pull-Up/Down Enable Register
000EC4H	PPER04 [R/W] - - - - - - 00	PPER05 [R/W] 00000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
000EC8H	PPER08 [R/W] 00000000	PPER09 [R/W] 00 - - 0000	PPER10 [R/W] - 000000 -	Reserved	
000ECCH	Reserved	PPER13 [R/W] - - - - - 000	PPER14 [R/W] 00000000	PPER15 [R/W] - - - - 0000	
000ED0H	PPER16 [R/W] 00000000	PPER17 [R/W] 0000 - - - -	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
000ED4H	PPER20 [R/W] - - - - - 000	Reserved	PPER22 [R/W] - - 00 - 0 - 0	PPER23 [R/W] - - 000000	
000ED8H	PPER24 [R/W] 00000000	PPER25 [R/W] 00000000	PPER26 [R/W] 00000000	PPER27 [R/W] 00000000	
000EDCH	Reserved	PPER29 [R/W] 00000000	Reserved		
000EE0H to 000EFCH	Reserved				Reserved

(Continued)

PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000F00H	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	PPCR02 [R/W] 11111111	PPCR03 [R/W] 11111111	R-bus Port Pull-Up/Down Control Register
000F04H	PPCR04 [R/W] - - - - - - 11	PPCR05 [R/W] 11111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
000F08H	PPCR08 [R/W] 11111111	PPCR09 [R/W] 11 - - 1111	PPCR10 [R/W] - 111111 -	Reserved	
000F0CH	Reserved	PPCR13 [R/W] - - - - - 111	PPCR14 [R/W] 11111111	PPCR15 [R/W] - - - - 1111	
000F10H	PPCR16 [R/W] 11111111	PPCR17 [R/W] 1111 - - - -	PPCR18 [R/W] - 111 - 111	PPCR19 [R/W] - 111 - 111	
000F14H	PPCR20 [R/W] - - - - - 111	Reserved	PPCR22 [R/W] - - 11 - 1 - 1	PPCR23 [R/W] - - 111111	
000F18H	PPCR24 [R/W] 11111111	PPCR25 [R/W] 11111111	PPCR26 [R/W] 11111111	PPCR27 [R/W] 11111111	
000F1CH	Reserved	PPCR29 [R/W] 11111111	Reserved		
000F20H to 000F3CH	Reserved				Reserved
001000H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001028H to 001FFCH	Reserved				Reserved

(Continued)

PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
002000H to 006FFCH	MB91F467Dx Flash-cache size is 8 Kbytes : 004000H to 005FFCH MB91F465DA Flash-cache size is 8 Kbytes : 004000H to 005FFCH				Flash-cache / I-RAM area
007000H	FMCS [R/W] 01101000	FMCR [R] - - - 00000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ Flash-cache/ I-RAM Control Register
007004H	FMWT [R/W] 11111111 11111111		FMWT2 [R] - 001 - - - -	FMPS [R/W] - - - - - 000	
007008H	FMAC [R] 00000000 00000000 00000000 00000000				
00700CH	FCHA0 [R/W] - - - - - - - - - - - 00000 00000000 00000000				Flash-cache Non-cacheable area setting Register
007010H	FCHA1 [R/W] - - - - - - - - - - - 00000 00000000 00000000				
007014H to 007FFCH	Reserved				Reserved
008000H to 00BFFCH	MB91F467Dx Boot-ROM size is 4 Kbytes : 00B000H to 00BFFCH MB91F465DA Boot-ROM size is 4 Kbytes : 00B000H to 00BFFCH (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area
00C000H	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
00C004H	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
00C008H	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
00C00CH	BRPE0 [R/W] 00000000 00000000		Reserved		
00C010H	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
00C014H	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
00C018H	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
00C01CH	IF1MCTR0 [R/W] 00000000 00000000		Reserved		

(Continued)

PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C020H	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		CAN 0 IF 1 Register
00C024H	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
00C028H, 00C02CH	Reserved				
00C030H	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
00C034H	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
00C038H, 00C03CH	Reserved				
00C040H	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
00C044H	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
00C048H	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
00C04CH	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
00C050H	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
00C054H	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
00C058H, 00C05CH	Reserved				
00C060H	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
00C064H	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
00C068H to 00C07CH	Reserved				

(Continued)

PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C080H	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
00C084H to 00C08CH	Reserved				
00C090H	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
00C094H to 00C09CH	Reserved				
00C0A0H	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
00C0A4H to 00C0ACH	Reserved				
00C0B0H	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
00C0B4H to 00C0FCH	Reserved				Reserved
00C100H	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN 1 Control Register
00C104H	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
00C108H	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
00C10CH	BRPE1 [R/W] 00000000 00000000		Reserved		
00C110H	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN 1 IF 1 Register
00C114H	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		
00C118H	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
00C11CH	IF1MCTR1 [R/W] 00000000 00000000		Reserved		
00C120H	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
00C124H	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		

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PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C128H, 00C12CH	Reserved				CAN 1 IF 1 Register
00C130H	IF1DTA21 [R/W] 00000000 00000000		IF1DTA11 [R/W] 00000000 00000000		
00C134H	IF1DTB21 [R/W] 00000000 00000000		IF1DTB11 [R/W] 00000000 00000000		
00C138H, 00C13CH	Reserved				
00C140H	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN 1 IF 2 Register
00C144H	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
00C148H	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		
00C14CH	IF2MCTR1 [R/W] 00000000 00000000		Reserved		
00C150H	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
00C154H	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
00C158H, 00C15CH	Reserved				
00C160H	IF2DTA21 [R/W] 00000000 00000000		IF2DTA11 [R/W] 00000000 00000000		
00C164H	IF2DTB21 [R/W] 00000000 00000000		IF2DTB11 [R/W] 00000000 00000000		
00C168H to 00C17CH	Reserved				
00C180H	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN 1 Status Flags
00C184H to 00C18CH	Reserved				
00C190H	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
00C194H to 00C19CH	Reserved				

(Continued)

PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C1A0H	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		CAN 1 Status Flags
00C1A4H to 00C1ACH	Reserved				
00C1B0H	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
00C1B4H to 00C1FCH	Reserved				
00C200H	CTRLR2 [R/W] 00000000 00000001		STATR2 [R/W] 00000000 00000000		CAN 2 Control Register
00C204H	ERRCNT2 [R] 00000000 00000000		BTR2 [R/W] 00100011 00000001		
00C208H	INTR2 [R] 00000000 00000000		TESTR2 [R/W] 00000000 X0000000		
00C20CH	BRPE2 [R/W] 00000000 00000000		Reserved		
00C210H	IF1CREQ2 [R/W] 00000000 00000001		IF1CMSK2 [R/W] 00000000 00000000		CAN 2 IF 1 Register
00C214H	IF1MSK22 [R/W] 11111111 11111111		IF1MSK12 [R/W] 11111111 11111111		
00C218H	IF1ARB22 [R/W] 00000000 00000000		IF1ARB12 [R/W] 00000000 00000000		
00C21CH	IF1MCTR2 [R/W] 00000000 00000000		Reserved		
00C220H	IF1DTA12 [R/W] 00000000 00000000		IF1DTA22 [R/W] 00000000 00000000		
00C224H	IF1DTB12 [R/W] 00000000 00000000		IF1DTB22 [R/W] 00000000 00000000		
00C228H, 00C22CH	Reserved				
00C230H	IF1DTA22 [R/W] 00000000 00000000		IF1DTA12 [R/W] 00000000 00000000		
00C234H	IF1DTB22 [R/W] 00000000 00000000		IF1DTB12 [R/W] 00000000 00000000		
00C238H, 00C23CH	Reserved				

(Continued)

PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C240H	IF2CREQ2 [R/W] 00000000 00000001		IF2CMSK2 [R/W] 00000000 00000000		CAN 2 IF 2 Register
00C244H	IF2MSK22 [R/W] 11111111 11111111		IF2MSK12 [R/W] 11111111 11111111		
00C248H	IF2ARB22 [R/W] 00000000 00000000		IF2ARB12 [R/W] 00000000 00000000		
00C24CH	IF2MCTR2 [R/W] 00000000 00000000		Reserved		
00C250H	IF2DTA12 [R/W] 00000000 00000000		IF2DTA22 [R/W] 00000000 00000000		
00C254H	IF2DTB12 [R/W] 00000000 00000000		IF2DTB22 [R/W] 00000000 00000000		
00C258H, 00C25CH	Reserved				
00C260H	IF2DTA22 [R/W] 00000000 00000000		IF2DTA12 [R/W] 00000000 00000000		
00C264H	IF2DTB22 [R/W] 00000000 00000000		IF2DTB12 [R/W] 00000000 00000000		
00C268H to 00C27CH	Reserved				
00C280H	TREQR22 [R] 00000000 00000000		TREQR12 [R] 00000000 00000000		CAN 2 Status Flags
00C284H to 00C28CH	Reserved				
00C290H	NEWDT22 [R] 00000000 00000000		NEWDT12 [R] 00000000 00000000		
00C294H to 00C29CH	Reserved				
00C2A0H	INTPND22 [R] 00000000 00000000		INTPND12 [R] 00000000 00000000		
00C2A4H to 00C2ACH	Reserved				
00C2B0H	MSGVAL22 [R] 00000000 00000000		MSGVAL12 [R] 00000000 00000000		

(Continued)

PRELIMINARY

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C2B4H to 00EFFCH	Reserved				Reserved
00F000H	BCTRL [R/W] -------- -------- 11111100 00000000				EDSU / MPU
00F004H	BSTAT [R/W] -------- -----000 00000000 10--0000				
00F008H	BIAC [R] -------- -------- 00000000 00000000				
00F00CH	BOAC [R] -------- -------- 00000000 00000000				
00F010H	BIRQ [R/W] -------- -------- 00000000 00000000				
00F014H to 00F01CH	Reserved				
00F020H	BCR0 [R/W] -------- 00000000 00000000 00000000				
00F024H	BCR1 [R/W] -------- 00000000 00000000 00000000				
00F028H	BCR2 [R/W] -------- 00000000 00000000 00000000				
00F02CH	BCR3 [R/W] -------- 00000000 00000000 00000000				
00F030H to 00F07CH	Reserved				Reserved
00F080H	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
00F084H	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F088H	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F08CH	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F090H	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F094H	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F098H	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

PRELIMINARY

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00F09C$_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
00F0A0$_H$	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A4$_H$	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A8$_H$	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0AC$_H$	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B0$_H$	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B4$_H$	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B8$_H$	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0BC$_H$	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0C0$_H$ to 01FFFC$_H$	Reserved				Reserved
020000$_H$ to 02FFFC$_H$	MB91F467Dx D-RAM size is 32 Kbytes : 028000$_H$ to 02FFFC$_H$ MB91F465DA D-RAM size is 32 Kbytes : 028000$_H$ to 02FFFC$_H$ (data access is 0 wait cycles)				D-RAM area
030000$_H$ to 03FFFC$_H$	MB91F467Dx ID-RAM size is 32 Kbytes : 030000$_H$ to 037FFC$_H$ MB91F465DA ID-RAM size is 16 Kbytes : 030000$_H$ to 033FFC$_H$ (instruction access is 0 wait cycles, data access is 1 wait cycle)				ID-RAM area

*1 : depends on the number of available CAN channels

*2 : ACR0 [11 : 10] depends on bus width setting in Mode vector fetch information

*3 : TCR [3 : 0] INIT value = 0000, keeps value after RST

PRELIMINARY

2. Flash memory and external bus area

32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000H to 05FFF8H	SA8 (64kB, MB91F467Dx) External bus (MB91F465DA)				SA9 (64kB, MB91F467Dx) External bus (MB91F465DA)				ROMS0
060000H to 07FFF8H	SA10 (64kB, MB91F467Dx) External bus (MB91F465DA)				SA11 (64kB, MB91F467Dx) External bus (MB91F465DA)				ROMS1
080000H to 09FFF8H	SA12 (64kB)				SA13 (64kB)				ROMS2
0A0000H to 0BFFF8H	SA14 (64kB)				SA15 (64kB)				ROMS3
0C0000H to 0DFFF8H	SA16 (64kB)				SA17 (64kB)				ROMS4
0E0000H to 0FFFF0H	SA18 (64kB)				SA19 (64kB)				ROMS5
0FFFF8H	FMV [R] 06 00 00 00H				FRV [R] 00 00 BF F8H				
100000H to 11FFF8H	SA20 (64kB, MB91F467Dx) External bus (MB91F465DA)				SA21 (64kB, MB91F467Dx) External bus (MB91F465DA)				ROMS6
120000H to 13FFF8H	SA22 (64kB, MB91F467Dx) External bus (MB91F465DA)				SA23 (64kB, MB91F467Dx) External bus (MB91F465DA)				
140000H to 143FF8H	SA0 (8kB, MB91F467Dx) Reserved (MB91F465DA)				SA1 (8kB, MB91F467Dx) Reserved (MB91F465DA)				ROMS7
144000H to 17FF8H	SA2 (8kB, MB91F467Dx) Reserved (MB91F465DA)				SA3 (8kB, MB91F467Dx) Reserved (MB91F465DA)				
148000H to 14BFF8H	SA4 (8kB, MB91F467Dx)				SA5 (8kB, MB91F467Dx)				
14C000H to 14FFF8H	SA6 (8kB, MB91F467Dx)				SA7 (8kB, MB91F467Dx)				
150000H to 17FFF8H	Reserved								

PRELIMINARY

32bit read/write	dat[31:0]				dat[31:0]				
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
180000H to 1BFFF8H	External Bus Area								ROMS8
1C0000H to 1FFFF8H									ROMS9
200000H to 27FFF8H									ROMS10
280000H to 2FFFF8H									ROMS11
300000H to 37FFF8H									ROMS12
380000H to 3FFFF8H									ROMS13
400000H to 47FFF8H									ROMS14
480000H to 4FFFF8H									ROMS15

Notes: Write operations to address 0FFFF8H and 0FFFFCH are not possible. When reading these addresses, the values shown above will be read.

On MB91F465DA, write access to the flash is only possible in 16-bit mode.

PRELIMINARY

■ INTERRUPT VECTOR TABLE

Interrupt	Interrupt number		Interrupt level		Interrupt vector		Resource number*1
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	
Reset	0	00	—	—	3FC$_H$	000FFFFC$_H$	—
Mode vector	1	01	—	—	3F8$_H$	000FFFF8$_H$	—
System reserved	2	02	—	—	3F4$_H$	000FFFF4$_H$	—
System reserved	3	03	—	—	3F0$_H$	000FFFF0$_H$	—
System reserved	4	04	—	—	3EC$_H$	000FFFEC$_H$	—
CPU supervisor mode (INT #5 instruction) *2	5	05	—	—	3E8$_H$	000FFFE8$_H$	—
Memory Protection exception *2	6	06	—	—	3E4$_H$	000FFFE4$_H$	—
System reserved	7	07	—	—	3E0$_H$	000FFFE0$_H$	—
System reserved	8	08	—	—	3DC$_H$	000FFFDC$_H$	—
System reserved	9	09	—	—	3D8$_H$	000FFFD8$_H$	—
System reserved	10	0A	—	—	3D4$_H$	000FFFD4$_H$	—
System reserved	11	0B	—	—	3D0$_H$	000FFFD0$_H$	—
System reserved	12	0C	—	—	3CC$_H$	000FFFCC$_H$	—
System reserved	13	0D	—	—	3C8$_H$	000FFFC8$_H$	—
Undefined instruction exception	14	0E	—	—	3C4$_H$	000FFFC4$_H$	—
NMI request	15	0F	F$_H$ fixed		3C0$_H$	000FFFC0$_H$	—
External Interrupt 0	16	10	ICR00	440$_H$	3BC$_H$	000FFFBC$_H$	0, 16
External Interrupt 1	17	11			3B8$_H$	000FFFB8$_H$	1, 17
External Interrupt 2	18	12	ICR01	441$_H$	3B4$_H$	000FFFB4$_H$	2, 18
External Interrupt 3	19	13			3B0$_H$	000FFFB0$_H$	3, 19
External Interrupt 4	20	14	ICR02	442$_H$	3AC$_H$	000FFFAC$_H$	20
External Interrupt 5	21	15			3A8$_H$	000FFFA8$_H$	21
External Interrupt 6	22	16	ICR03	443$_H$	3A4$_H$	000FFFA4$_H$	22
External Interrupt 7	23	17			3A0$_H$	000FFFA0$_H$	23
External Interrupt 8	24	18	ICR04	444$_H$	39C$_H$	000FFF9C$_H$	—
External Interrupt 9	25	19			398$_H$	000FFF98$_H$	—
External Interrupt 10	26	1A	ICR05	445$_H$	394$_H$	000FFF94$_H$	—
System reserved	27	1B			390$_H$	000FFF90$_H$	—
External Interrupt 12	28	1C	ICR06	446$_H$	38C$_H$	000FFF8C$_H$	—
External Interrupt 13	29	1D			388$_H$	000FFF88$_H$	—
External Interrupt 14	30	1E	ICR07	447$_H$	384$_H$	000FFF84$_H$	—
System reserved	31	1F			380$_H$	000FFF80$_H$	—

(Continued)

PRELIMINARY

Interrupt	Interrupt number		Interrupt level		Interrupt vector		Resource number*1
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	
Reload Timer 0	32	20	ICR08	448H	37CH	000FFF7CH	4, 32
Reload Timer 1	33	21			378H	000FFF78H	5, 33
Reload Timer 2	34	22	ICR09	449H	374H	000FFF74H	34
Reload Timer 3	35	23			370H	000FFF70H	35
Reload Timer 4	36	24	ICR10	44AH	36CH	000FFF6CH	36
Reload Timer 5	37	25			368H	000FFF68H	37
Reload Timer 6	38	26	ICR11	44BH	364H	000FFF64H	38
Reload Timer 7	39	27			360H	000FFF60H	39
Free Run Timer 0	40	28	ICR12	44CH	35CH	000FFF5CH	40
Free Run Timer 1	41	29			358H	000FFF58H	41
Free Run Timer 2	42	2A	ICR13	44DH	354H	000FFF54H	42
Free Run Timer 3	43	2B			350H	000FFF50H	43
Free Run Timer 4	44	2C	ICR14	44EH	34CH	000FFF4CH	44
Free Run Timer 5	45	2D			348H	000FFF48H	45
Free Run Timer 6	46	2E	ICR15	44FH	344H	000FFF44H	46
Free Run Timer 7	47	2F			340H	000FFF40H	47
CAN 0	48	30	ICR16	450H	33CH	000FFF3CH	—
CAN 1	49	31			338H	000FFF38H	—
CAN 2	50	32	ICR17	451H	334H	000FFF34H	—
System reserved	51	33			330H	000FFF30H	—
System reserved	52	34	ICR18	452H	32CH	000FFF2CH	—
System reserved	53	35			328H	000FFF28H	—
System reserved	54	36	ICR19	453H	324H	000FFF24H	6, 48
System reserved	55	37			320H	000FFF20H	7, 49
System reserved	56	38	ICR20	454H	31CH	000FFF1CH	8, 50
System reserved	57	39			318H	000FFF18H	9, 51
LIN-USART 2 RX	58	3A	ICR21	455H	314H	000FFF14H	52
LIN-USART 2 TX	59	3B			310H	000FFF10H	53
System reserved	60	3C	ICR22	456H	30CH	000FFF0CH	54
System reserved	61	3D			308H	000FFF08H	55
System reserved	62	3E	ICR23 *3	457H	304H	000FFF04H	—
Delayed Interrupt	63	3F			300H	000FFF00H	—

(Continued)

PRELIMINARY

Interrupt	Interrupt number		Interrupt level		Interrupt vector		Resource number*1
	Deci-mal	Hexa-decimal	Setting Register	Register address	Offset	Default Vector address	
System reserved *4	64	40	(ICR24)	(458H)	2FCH	000FFEFCH	—
System reserved *4	65	41			2F8H	000FFEF8H	—
LIN-USART (FIFO) 4 RX	66	42	ICR25	459H	2F4H	000FFEF4H	10, 56
LIN-USART (FIFO) 4 TX	67	43			2F0H	000FFEF0H	11, 57
LIN-USART (FIFO) 5 RX	68	44	ICR26	45AH	2ECH	000FFEECH	12, 58
LIN-USART (FIFO) 5 TX	69	45			2E8H	000FFEE8H	13, 59
LIN-USART (FIFO) 6 RX	70	46	ICR27	45BH	2E4H	000FFEE4H	60
LIN-USART (FIFO) 6 TX	71	47			2E0H	000FFEE0H	61
LIN-USART (FIFO) 7 RX	72	48	ICR28	45CH	2DCH	000FFEDCH	62
LIN-USART (FIFO) 7 TX	73	49			2D8H	000FFED8H	63
I²C 0 / I²C 2	74	4A	ICR29	45DH	2D4H	000FFED4H	—
I²C 3	75	4B			2D0H	000FFED0H	—
System reserved	76	4C	ICR30	45EH	2CCH	000FFECCH	64
System reserved	77	4D			2C8H	000FFEC8H	65
System reserved	78	4E	ICR31	45FH	2C4H	000FFEC4H	66
System reserved	79	4F			2C0H	000FFEC0H	67
System reserved	80	50	ICR32	460H	2BCH	000FFEBCH	68
System reserved	81	51			2B8H	000FFEB8H	69
System reserved	82	52	ICR33	461H	2B4H	000FFEB4H	70
System reserved	83	53			2B0H	000FFEB0H	71
System reserved	84	54	ICR34	462H	2ACH	000FFEACH	72
System reserved	85	55			2A8H	000FFEA8H	73
System reserved	86	56	ICR35	463H	2A4H	000FFEA4H	74
System reserved	87	57			2A0H	000FFEA0H	75
System reserved	88	58	ICR36	464H	29CH	000FFE9CH	76
System reserved	89	59			298H	000FFE98H	77
System reserved	90	5A	ICR37	465H	294H	000FFE94H	78
System reserved	91	5B			290H	000FFE90H	79
Input Capture 0	92	5C	ICR38	466H	28CH	000FFE8CH	80
Input Capture 1	93	5D			288H	000FFE88H	81
Input Capture 2	94	5E	ICR39	467H	284H	000FFE84H	82
Input Capture 3	95	5F			280H	000FFE80H	83

(Continued)

PRELIMINARY

Interrupt	Interrupt number		Interrupt level		Interrupt vector		Resource number*1
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	
Input Capture 4	96	60	ICR40	468H	27CH	000FFE7CH	84
Input Capture 5	97	61			278H	000FFE78H	85
Input Capture 6	98	62	ICR41	469H	274H	000FFE74H	86
Input Capture 7	99	63			270H	000FFE70H	87
Output Compare 0	100	64	ICR42	46AH	26CH	000FFE6CH	88
Output Compare 1	101	65			268H	000FFE68H	89
Output Compare 2	102	66	ICR43	46BH	264H	000FFE64H	90
Output Compare 3	103	67			260H	000FFE60H	91
System reserved	104	68	ICR44	46CH	25CH	000FFE5CH	92
System reserved	105	69			258H	000FFE58H	93
System reserved	106	6A	ICR45	46DH	254H	000FFE54H	94
System reserved	107	6B			250H	000FFE50H	95
Sound Generator	108	6C	ICR46	46EH	24CH	000FFE4CH	—
Phase Frequency Modulator	109	6D			248H	000FFE48H	—
System reserved	110	6E	ICR47 *4	46FH	244H	000FFE44H	—
System reserved	111	6F			240H	000FFE40H	—
System reserved	112	70	ICR48	470H	23CH	000FFE3CH	15, 96
System reserved	113	71			238H	000FFE38H	97
System reserved	114	72	ICR49	471H	234H	000FFE34H	98
System reserved	115	73			230H	000FFE30H	99
PPG4	116	74	ICR50	472H	22CH	000FFE2CH	100
PPG5	117	75			228H	000FFE28H	101
PPG6	118	76	ICR51	473H	224H	000FFE24H	102
PPG7	119	77			220H	000FFE20H	103
PPG8	120	78	ICR52	474H	21CH	000FFE1CH	104
PPG9	121	79			218H	000FFE18H	105
PPG10	122	7A	ICR53	475H	214H	000FFE14H	106
PPG11	123	7B			210H	000FFE10H	107
PPG12	124	7C	ICR54	476H	20CH	000FFE0CH	108
PPG13	125	7D			208H	000FFE08H	109
PPG14	126	7E	ICR55	477H	204H	000FFE04H	110
PPG15	127	7F			200H	000FFE00H	111

(Continued)

PRELIMINARY

(Continued)

Interrupt	Interrupt number		Interrupt level		Interrupt vector		Resource number*1
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	
Up/Down Counter 0	128	80	ICR56	478H	1FCH	000FFDFCH	—
System reserved	129	81			1F8H	000FFDF8H	—
Up/Down Counter 2	130	82	ICR57	479H	1F4H	000FFDF4H	—
Up/Down Counter 3	131	83			1F0H	000FFDF0H	—
Real Time Clock	132	84	ICR58	47AH	1ECH	000FFDECH	—
Calibration Unit	133	85			1E8H	000FFDE8H	—
A/D Converter 0	134	86	ICR59	47BH	1E4H	000FFDE4H	14, 112
System reserved	135	87			1E0H	000FFDE0H	—
Alarm Comparator 0	136	88	ICR60	47CH	1DCH	000FFDDCH	—
System reserved	137	89			1D8H	000FFDD8H	—
Low Voltage Detection	138	8A	ICR61	47DH	1D4H	000FFDD4H	—
SMC Comparator 0 to 5	139	8B			1D0H	000FFDD0H	—
Timebase Overflow	140	8C	ICR62	47EH	1CCH	000FFDCCH	—
PLL Clock Gear	141	8D			1C8H	000FFDC8H	—
DMA Controller	142	8E	ICR63	47FH	1C4H	000FFDC4H	—
Main/Sub OSC stability wait	143	8F			1C0H	000FFDC0H	—
Security vector	144	90	—	—	1BCH	000FFDBCH	—
Used by the INT instruction.	145 to 255	91 to FF	—	—	1B8H to 000H	000FFDB8H to 000FFC00H	—

*1 : The ICRs are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2 : The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (000FFC00H) . The TBR is initialized to this value by a reset. The TBR is set to 000FFC00H after the internal boot ROM is executed.

*3 : ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr 0C03H : IOS[0])

*4 : Used by REALOS

PRELIMINARY

■ RECOMMENDED SETTINGS

1. PLL and Clockgear settings

Please note that for MB91F467Dx the core base clock frequencies are valid in the 1.8V operation mode of the Main regulator and Flash.

Recommended PLL divider and clockgear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	*1
4	2	24	16	24	192	96	
4	2	23	16	24	184	92	
4	2	22	16	24	176	88	
4	2	21	16	20	168	84	
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

*1 This setting is not possible at MB91F467Dx

PRELIMINARY

2. Clock Modulator settings

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 88MHz.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	026F	88	79.5	98.5	*1
1	3	026F	84	76.1	93.8	
1	3	026F	80	72.6	89.1	
1	5	02AE	80	68.7	95.8	
2	3	046E	80	68.7	95.8	
1	3	026F	76	69.1	84.5	
1	5	02AE	76	65.3	90.8	
1	7	02ED	76	62	98.1	*1
2	3	046E	76	65.3	90.8	
3	3	066D	76	62	98.1	*1
1	3	026F	72	65.5	79.9	
1	5	02AE	72	62	85.8	
1	7	02ED	72	58.8	92.7	
2	3	046E	72	62	85.8	
3	3	066D	72	58.8	92.7	
1	3	026F	68	62	75.3	
1	5	02AE	68	58.7	80.9	
1	7	02ED	68	55.7	87.3	
1	9	032C	68	53	95	
2	3	046E	68	58.7	80.9	
2	5	04AC	68	53	95	
3	3	066D	68	55.7	87.3	
4	3	086C	68	53	95	
1	3	026F	64	58.5	70.7	
1	5	02AE	64	55.3	75.9	
1	7	02ED	64	52.5	82	
1	9	032C	64	49.9	89.1	
1	11	036B	64	47.6	97.6	*1
2	3	046E	64	55.3	75.9	
2	5	04AC	64	49.9	89.1	

(Continued)

PRELIMINARY

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
3	3	066D	64	52.5	82	
4	3	086C	64	49.9	89.1	
5	3	0A6B	64	47.6	97.6	
1	3	026F	60	54.9	66.1	
1	5	02AE	60	51.9	71	
1	7	02ED	60	49.3	76.7	
1	9	032C	60	46.9	83.3	
1	11	036B	60	44.7	91.3	
2	3	046E	60	51.9	71	
2	5	04AC	60	46.9	83.3	
3	3	066D	60	49.3	76.7	
4	3	086C	60	46.9	83.3	
5	3	0A6B	60	44.7	91.3	
1	3	026F	56	51.4	61.6	
1	5	02AE	56	48.6	66.1	
1	7	02ED	56	46.1	71.4	
1	9	032C	56	43.8	77.6	
1	11	036B	56	41.8	84.9	
1	13	03AA	56	39.9	93.8	
2	3	046E	56	48.6	66.1	
2	5	04AC	56	43.8	77.6	
2	7	04EA	56	39.9	93.8	
3	3	066D	56	46.1	71.4	
3	5	06AA	56	39.9	93.8	
4	3	086C	56	43.8	77.6	
5	3	0A6B	56	41.8	84.9	
6	3	0C6A	56	39.9	93.8	
1	3	026F	52	47.8	57	
1	5	02AE	52	45.2	61.2	
1	7	02ED	52	42.9	66.1	
1	9	032C	52	40.8	71.8	
1	11	036B	52	38.8	78.6	
1	13	03AA	52	37.1	86.8	
1	15	03E9	52	35.5	96.9	*1
2	3	046E	52	45.2	61.2	

(Continued)

PRELIMINARY

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
2	5	04AC	52	40.8	71.8	
2	7	04EA	52	37.1	86.8	
3	3	066D	52	42.9	66.1	
3	5	06AA	52	37.1	86.8	
4	3	086C	52	40.8	71.8	
5	3	0A6B	52	38.8	78.6	
6	3	0C6A	52	37.1	86.8	
7	3	0E69	52	35.5	96.9	*1
1	3	026F	48	44.2	52.5	
1	5	02AE	48	41.8	56.4	
1	7	02ED	48	39.6	60.9	
1	9	032C	48	37.7	66.1	
1	11	036B	48	35.9	72.3	
1	13	03AA	48	34.3	79.9	
1	15	03E9	48	32.8	89.1	
2	3	046E	48	41.8	56.4	
2	5	04AC	48	37.7	66.1	
2	7	04EA	48	34.3	79.9	
3	3	066D	48	39.6	60.9	
3	5	06AA	48	34.3	79.9	
4	3	086C	48	37.7	66.1	
5	3	0A6B	48	35.9	72.3	
6	3	0C6A	48	34.3	79.9	
7	3	0E69	48	32.8	89.1	
1	3	026F	44	40.6	48.1	
1	5	02AE	44	38.4	51.6	
1	7	02ED	44	36.4	55.7	
1	9	032C	44	34.6	60.4	
1	11	036B	44	33	66.1	
1	13	03AA	44	31.5	73	
1	15	03E9	44	30.1	81.4	
2	3	046E	44	38.4	51.6	
2	5	04AC	44	34.6	60.4	
2	7	04EA	44	31.5	73	
2	9	0528	44	28.9	92.1	

(Continued)

PRELIMINARY

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
3	3	066D	44	36.4	55.7	
3	5	06AA	44	31.5	73	
4	3	086C	44	34.6	60.4	
4	5	08A8	44	28.9	92.1	
5	3	0A6B	44	33	66.1	
6	3	0C6A	44	31.5	73	
7	3	0E69	44	30.1	81.4	
8	3	1068	44	28.9	92.1	
1	3	026F	40	37	43.6	
1	5	02AE	40	34.9	46.8	
1	7	02ED	40	33.1	50.5	
1	9	032C	40	31.5	54.8	
1	11	036B	40	30	59.9	
1	13	03AA	40	28.7	66.1	
1	15	03E9	40	27.4	73.7	
2	3	046E	40	34.9	46.8	
2	5	04AC	40	31.5	54.8	
2	7	04EA	40	28.7	66.1	
2	9	0528	40	26.3	83.3	
3	3	066D	40	33.1	50.5	
3	5	06AA	40	28.7	66.1	
3	7	06E7	40	25.3	95.8	
4	3	086C	40	31.5	54.8	
4	5	08A8	40	26.3	83.3	
5	3	0A6B	40	30	59.9	
6	3	0C6A	40	28.7	66.1	
7	3	0E69	40	27.4	73.7	
8	3	1068	40	26.3	83.3	
9	3	1267	40	25.3	95.8	
1	3	026F	36	33.3	39.2	
1	5	02AE	36	31.5	42	
1	7	02ED	36	29.9	45.3	
1	9	032C	36	28.4	49.2	
1	11	036B	36	27.1	53.8	
1	13	03AA	36	25.8	59.3	

(Continued)

PRELIMINARY

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	15	03E9	36	24.7	66.1	
2	3	046E	36	31.5	42	
2	5	04AC	36	28.4	49.2	
2	7	04EA	36	25.8	59.3	
2	9	0528	36	23.7	74.7	
3	3	066D	36	29.9	45.3	
3	5	06AA	36	25.8	59.3	
3	7	06E7	36	22.8	85.8	
4	3	086C	36	28.4	49.2	
4	5	08A8	36	23.7	74.7	
5	3	0A6B	36	27.1	53.8	
6	3	0C6A	36	25.8	59.3	
7	3	0E69	36	24.7	66.1	
8	3	1068	36	23.7	74.7	
9	3	1267	36	22.8	85.8	
1	3	026F	32	29.7	34.7	
1	5	02AE	32	28	37.3	
1	7	02ED	32	26.6	40.2	
1	9	032C	32	25.3	43.6	
1	11	036B	32	24.1	47.7	
1	13	03AA	32	23	52.5	
1	15	03E9	32	22	58.6	
2	3	046E	32	28	37.3	
2	5	04AC	32	25.3	43.6	
2	7	04EA	32	23	52.5	
2	9	0528	32	21.1	66.1	
2	11	0566	32	19.5	89.1	
3	3	066D	32	26.6	40.2	
3	5	06AA	32	23	52.5	
3	7	06E7	32	20.3	75.9	
4	3	086C	32	25.3	43.6	
4	5	08A8	32	21.1	66.1	
5	3	0A6B	32	24.1	47.7	
5	5	0AA6	32	19.5	89.1	
6	3	0C6A	32	23	52.5	

(Continued)

PRELIMINARY

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
7	3	0E69	32	22	58.6	
8	3	1068	32	21.1	66.1	
9	3	1267	32	20.3	75.9	
10	3	1466	32	19.5	89.1	

*1 These settings are not possible at MB91F467Dx

PRELIMINARY

■ ELECTRICAL CHARACTERISTICS

1. Absolute maximum ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply slew rate	—	—	50	V/ms	
Power supply voltage 1*1	$V_{DD}5R$	– 0.3	+ 6.0	V	
Power supply voltage 2*1	$V_{DD}5$	– 0.3	+ 6.0	V	
Power supply voltage 3*1	$HV_{DD}5$	– 0.3	+ 6.0	V	
Power supply voltage 4*1	$V_{DD}35$	– 0.3	+ 6.0	V	
Relationship of the supply voltages	$HV_{DD}5$	$V_{DD}5$-0.3	$V_{DD}5$+0.3	V	SMC mode
		$V_{SS}5$-0.3	$V_{DD}5$+0.3	V	General purpose port mode
	$AV_{CC}5$	$V_{DD}5$-0.3	$V_{DD}5$+0.3	V	At least one pin of the Ports 25 to 29 (SMC, ANn) is used as digital input or output.
		$V_{SS}5$-0.3	$V_{DD}5$+0.3	V	All pins of the Ports 25 to 29 (SMC, ANn) follow the condition of V_{IA}
Analog power supply voltage*1	$AV_{CC}5$	– 0.3	+ 6.0	V	*2
Analog reference power supply voltage*1	AVRH	– 0.3	+ 6.0	V	*2
Input voltage 1*1	V_{I1}	Vss5 – 0.3	$V_{DD}5$ + 0.3	V	
Input voltage 2*1	V_{I2}	Vss5 – 0.3	$V_{DD}35$ + 0.3	V	External bus
Input voltage 3*1	V_{I3}	HVss5 – 0.3	$HV_{DD}5$ + 0.3	V	Stepper motor controller
Analog pin input voltage*1	V_{IA}	AVss5 – 0.3	AVcc5 + 0.3	V	
Output voltage 1*1	V_{O1}	Vss5 – 0.3	$V_{DD}5$ + 0.3	V	
Output voltage 2*1	V_{O2}	Vss5 – 0.3	$V_{DD}35$ + 0.3	V	External bus
Output voltage 3*1	V_{O3}	HVss5 – 0.3	$HV_{DD}5$ + 0.3	V	Stepper motor controller
Maximum clamp current	I_{CLAMP}	– 4.0	+ 4.0	mA	*3
Total maximum clamp current	$\Sigma \lvert I_{CLAMP} \rvert$	—	20	mA	*3
"L" level maximum output current*4	I_{OL}	—	10	mA	
		—	40	mA	Stepper motor controller
"L" level average output current*5	I_{OLAV}	—	8	mA	
		—	30	mA	Stepper motor controller
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
		—	360	mA	Stepper motor controller
"L" level total average output current*6	ΣI_{OLAV}	—	50	mA	
		—	230	mA	Stepper motor controller
"H" level maximum output current*4	I_{OH}	—	– 10	mA	
		—	– 40	mA	Stepper motor controller

PRELIMINARY

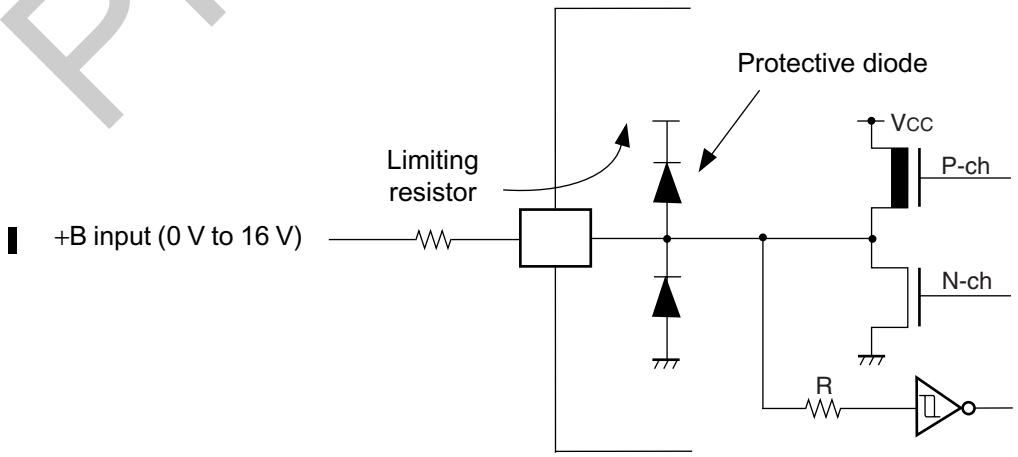
Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
"H" level average output current*5	I_{OHAV}	—	– 4	mA	
		—	– 30	mA	Stepper motor controller
"H" level total maximum output current	ΣI_{OH}	—	– 100	mA	
		—	– 360	mA	Stepper motor controller
"H" level total average output current*6	ΣI_{OHAV}	—	– 25	mA	
		—	– 230	mA	Stepper motor controller
Power consumption	P_D	—	1000	mW	
Operating temperature	T_A	– 40	+ 105	°C	
Storage temperature	Tstg	– 55	+ 150	°C	

*1 : The parameter is based on $V_{SS}5 = HV_{SS}5 = AV_{SS}5 = 0.0$ V.

*2 : $AV_{CC}5$ and AVRH5 must not exceed $V_{DD}5 + 0.3$ V.

*3 :
- Use within recommended operating conditions.
- Use with DC voltage (current).
- +B signals are input signals that exceed the $V_{DD}5$ voltage. +B signals should always be applied by connecting a limiting resistor between the +B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed the rated value at any time , either instantaneously or for an extended period, when the +B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the +B input potential can increase the potential at the power supply pin via a protective diode, possibly affecting other devices.
- Note that if the +B signal is input when the microcontroller is off (not fixed at 0 V), power is supplied through the +B input pin; therefore, the microcontroller may partially operate.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave +B input pins open.
- Note that analog input/output pins cannot accept +B signal input.
- Example of recommended circuit :

• Input/output equivalent circuit



PRELIMINARY

- *4 : Maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.
- *5 : Average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 100 ms period.
- *6 : Total average output current is defined as the value of the average current flowing through all of the corresponding pins for a 100 ms period.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

PRELIMINARY

2. Recommended operating conditions

($V_{SS}5 = AV_{SS}5 = 0.0$ V)

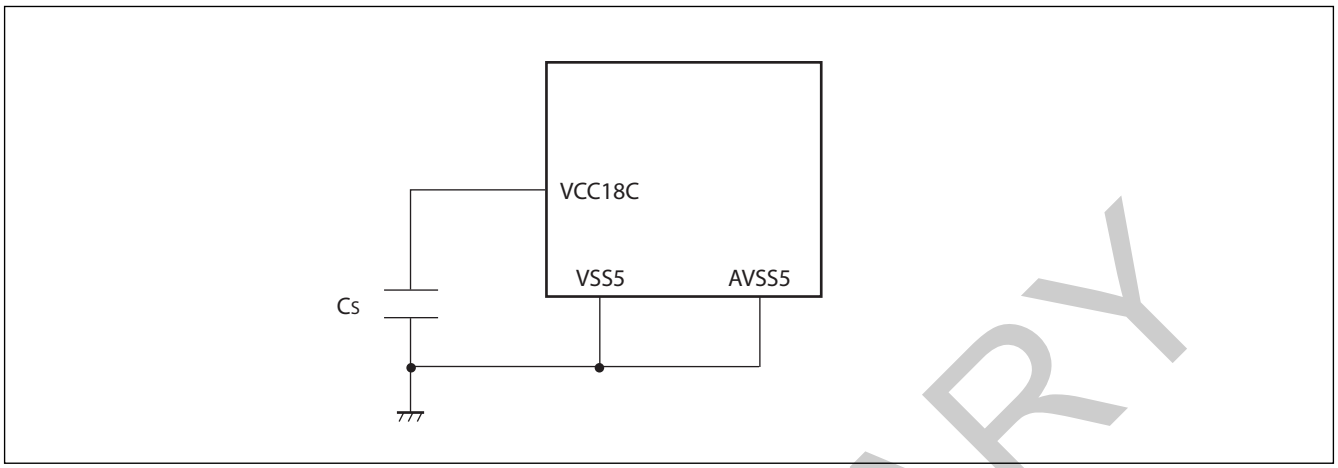
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{DD}5$	3.0	—	5.5	V	
	$V_{DD}5R$	3.0	—	5.5	V	Internal regulator
	$V_{DD}35$	3.0	—	5.5	V	External bus
	$HV_{DD}5$	4.5	—	5.5	V	Stepper motor controller
		3.0	—	5.5	V	Stepper motor controller (when all pins are used as general-purpose ports)
	$AV_{CC}5$	3.0	—	5.5	V	A/D converter
Smoothing capacitor at VCC18C pin	C_S	—	4.7	—	µF	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics.
Power supply slew rate		—	—	50	V/ms	
Operating temperature	T_A	– 40	—	+ 105	°C	
Stepper motor control slew rate			40		ns	Cload = 0 pF
Main Oscillation stabilisation time		10			ms	
Look-up time PLL (4 MHz ->16 ...100MHz)				0.6	ms	
ESD Protection (Human body model)	V_{surge}	2			kV	$R_{discharge}$ = 1.5kΩ $C_{discharge}$ = 100pF
RC Oscillator	$f_{RC100kHz}$ f_{RC2MHz}	50 1	100 2	200 4	kHz MHz	$VDD_{CORE} \geq 1.65V$

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

PRELIMINARY



PRELIMINARY

3. DC characteristics

Note: In the following tables, "V_{DD}" means $V_{DD}35$ for pins of ext. bus or $HV_{DD}5$ for SMC pins or $V_{DD}5$ for other pins.
In the following tables, "V_{SS}" means Hvss5 for ground Pins of the stepper motor and $V_{SS}5$ for the other pins.
($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input "H" voltage	V_{IH}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	CMOS hysteresis input
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$0.7 \times V_{DD}$	—	$V_{DD} + 0.3$	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				$0.74 \times V_{DD}$	—	$V_{DD} + 0.3$	V	3 V ≤ V_{DD} < 4.5 V
		—	AUTOMOTIVE Hysteresis input is selected	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	
		—	Port inputs if TTL input is selected	2.0	—	$V_{DD} + 0.3$	V	
	V_{IHR}	INITX	—	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	INITX input pin (CMOS Hysteresis)
	V_{IHM}	MD_2 to MD_0	—	$V_{DD} - 0.3$	—	$V_{DD} + 0.3$	V	Mode input pins
	V_{IHX0S}	X0, X0A	—	2.5	—	$V_{DD} + 0.3$	V	External clock in "Oscillation mode"
	V_{IHX0F}	X0	—	$0.8 \times V_{DD}$	—	$V_{DD} + 0.3$	V	External clock in "Fast Clock Input mode"
Input "L" voltage	V_{IL}	—	Port inputs if CMOS Hysteresis 0.8/0.2 input is selected	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	
		—	Port inputs if CMOS Hysteresis 0.7/0.3 input is selected	$V_{SS} - 0.3$	—	$0.3 \times V_{DD}$	V	
		—	Port inputs if AUTOMOTIVE Hysteresis input is selected	$V_{SS} - 0.3$	—	$0.5 \times V_{DD}$	V	4.5 V ≤ V_{DD} ≤ 5.5 V
				$V_{SS} - 0.3$	—	$0.46 \times V_{DD}$	V	3 V ≤ V_{DD} < 4.5 V
		—	Port inputs if TTL input is selected	$V_{SS} - 0.3$	—	0.8	V	
	V_{ILR}	INITX	—	$V_{SS} - 0.3$	—	$0.2 \times V_{DD}$	V	INITX input pin (CMOS Hysteresis)
	V_{ILM}	MD_2 to MD_0	—	$V_{SS} - 0.3$	—	$V_{SS} + 0.3$	V	Mode input pins
	V_{ILXDS}	X0, X0A	—	$V_{SS} - 0.3$	—	0.5	V	External clock in "Oscillation mode"

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($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input “L” voltage	V_{ILXDF}	X0	—	V_{SS} – 0.3	—	0.2 × V_{DD}	V	External clock in “Fast Clock Input mode”
Output “H” voltage	V_{OH2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = – 2mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = – 1.6mA	V_{DD} – 0.5	—	—	V	Driving strength set to 2 mA
	V_{OH5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = – 5mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = – 3mA	V_{DD} – 0.5	—	—	V	Driving strength set to 5 mA
	V_{OH3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OH} = – 3mA	V_{DD} – 0.5	—	—	V	*1
	V_{OH30}	High current outputs	4.5V ≤ V_{DD} ≤ 5.5V, T_A = -40 °C, I_{OH} = -40mA 4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = -30mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = -20mA	V_{DD} – 0.5			V	Driving strength set to 30mA
Output “L“ voltage	V_{OL2}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 2mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = + 1.6mA	—	—	0.4	V	Driving strength set to 2 mA
	V_{OL5}	Normal outputs	4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 5mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = + 3mA	—	—	0.4	V	Driving strength set to 5 mA
	V_{OL3}	I^2C outputs	3.0V ≤ V_{DD} ≤ 5.5V, I_{OH} = + 3mA	—	—	0.4	V	*1
	V_{OL30}	High current outputs	4.5V ≤ V_{DD} ≤ 5.5V, T_A = -40 °C, I_{OH} = +40mA 4.5V ≤ V_{DD} ≤ 5.5V, I_{OH} = +30mA 3.0V ≤ V_{DD} ≤ 4.5V, I_{OH} = +20mA			0.5	V	Driving strength set to 30mA
Input leak-age current	I_{IL}	Pnn_m *2	3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=25 °C	– 1	—	+ 1	µA	
			3.0V ≤ V_{DD} ≤ 5.5V $V_{SS}5 < V_I < V_{DD}$ T_A=105 °C	– 3	—	+ 3		

PRELIMINARY

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Analog input leakage current	I_{AIN}	ANn	3.0V ≤ V_{DD} ≤ 5.5V T_A=25 °C	− 1	—	+ 1	µA	
			3.0V ≤ V_{DD} ≤ 5.5V T_A=105 °C	− 3	—	+ 3	µA	
Pull-up resistance	R_{UP}	Pnn_m *2, INITX	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	Pnn_m *2	—	25	50	100	kΩ	
Input capacitance	C_{IN}	All except V_{DD}5, V_{DD}5R, V_{SS}5, AV_{CC}5, AV_{SS}, AVRH5	f = 1 MHz	-	5	15	pF	
Power supply current MB91-F467Dx	I_{CC}	V_{DD}5R	MB91F467Dx: CLKB: 96 MHz CLKP: 48 MHz CLKT: 48 MHz CLKCAN: 48 MHz	—	120	150	mA	Code fetch from Flash
	I_{CCH}	V_{DD}5R	T_A = + 25 °C	—	30	150	µA	At stop mode *3 *4
			T_A = + 105 °C	—	400	2000	µA	
			T_A = + 25 °C	—	100	500	µA	RTC : 4 MHz mode *3 *4
			T_A = + 105 °C	—	500	2400	µA	
			T_A = + 25 °C	—	50	250	µA	RTC : 100 kHz mode *3 *4
			T_A = + 105 °C	—	450	2200	µA	
	I_{LV}	V_{DD}5	—	—	70	150	µA	Low voltage detection
	I_{OSC}	V_{DD}5	—	—	250	500	µA	Main clock (4 MHz)
			—	—	20	40	µA	Sub clock (32 kHz)

PRELIMINARY

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current MB91-F465DA	I_{CC}	$V_{DD}5R$	MB91F465DA: CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 50 MHz	-	110	140	mA	Code fetch from Flash
	I_{CCH}	$V_{DD}5R$	T_A = + 25 °C	-	30	150	µA	At stop mode *3
			T_A = + 105 °C	-	300	2000	µA	
			T_A = + 25 °C	-	100	500	µA	RTC : 4 MHz mode *3
			T_A = + 105 °C	-	500	2400	µA	
			T_A = + 25 °C	-	50	250	µA	RTC : 100 kHz mode *3
			T_A = + 105 °C	-	400	2200	µA	
	I_{LV}	$V_{DD}5$	-	-	70	150	µA	Low voltage detection
	I_{OSC}	$V_{DD}5$	-	-	250	500	µA	Main clock (4 MHz)
			-	-	20	40	µA	Sub clock (32 kHz)

*1 I2C Spec on MB91F467Dx only guaranteed for 4.5 V < $V_{DD}5$ < 5.5 V.

*2 Pnn_m includes all pins unless the pins, which include analog inputs.

*3 Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled.

*4 On MB91F467Dx, the I2C pin consumes typical 200 µA and maximal 400 µA when “L” level is output, even if there is no load condition. When entering the standby mode while I2C outputs “L”, the above-mentioned current is added to ICCH. The I2C pins are recommended to use for port input or external interrupt in standby mode.

PRELIMINARY

4. A/D converter characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, $T_A = -40$ °C to + 105 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	– 3	—	+ 3	LSB	
Nolinearity error	—	—	– 2.5	—	+ 2.5	LSB	
Differential nolinearity error	—	—	– 1.9	—	+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRL–1.5	AVRL + 0.5	AVRL + 2.5	LSB	
Full scale reading voltage	V_{FST}	ANn	AVRH–3.5	AVRH–1.5	AVRH + 0.5	LSB	
Compare time	T_{comp}	—	0.6	—	16,500	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			2.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Sampling time	T_{samp}	—	0.4	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V, R_{EXT} < 2 kΩ
			1.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V, R_{EXT} < 1 kΩ
Conversion time	T_{conv}	—	1.0	—	—	µs	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			3.0	—	—	µs	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Input capacitance	C_{IN}	ANn	—	—	11	pF	
Input resistance	R_{IN}	ANn	—	—	2.6	kΩ	4.5 V ≤ $AV_{CC}5$ ≤ 5.5 V
			—	—	12.1	kΩ	3.0 V ≤ $AV_{CC}5$ ≤ 4.5 V
Analog input leakage current	I_{AIN}	ANn	– 1	—	+ 1	µA	T_A = + 25 °C
			– 3	—	+ 3	µA	T_A = + 105 °C
Analog input voltage range	V_{AIN}	ANn	AVRL	—	AVRH	V	
Offset between input channels	—	ANn	—	—	t.b.d.	LSB	

(Continued)

Note : The accuracy gets worse as AVRH - AVRL becomes smaller

PRELIMINARY

(Continued)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	AVRH	AVRH5	0.75 × $AV_{CC}5$	—	$AV_{CC}5$	V	
	AVRL	$AV_{SS}5$	$AV_{SS}5$	—	$AV_{CC}5$ × 0.25	V	
Power supply current	I_A	$AV_{CC}5$	—	2.5	5	mA	A/D Converter active
	I_{AH}	$AV_{CC}5$	—	—	5	µA	A/D Converter not operated *1
Reference voltage current	I_R	AVRH5	—	0.7	1	mA	A/D Converter active
	I_{RH}	AVRH5	—	—	5	µA	A/D Converter not operated *2

*1 : Supply current at $AV_{CC}5$, if A/D converter and ALARM comparator are not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

*2 : Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

Sampling Time Calculation

$T_{samp} = (2.6\ kOhm + R_{EXT}) \times 11pF \times 7$; for $4.5V \le AV_{CC}5 \le 5.5V$

$T_{samp} = (12.1\ kOhm + R_{EXT}) \times 11pF \times 7$; for $3.0V \le AV_{CC}5 \le 4.5V$

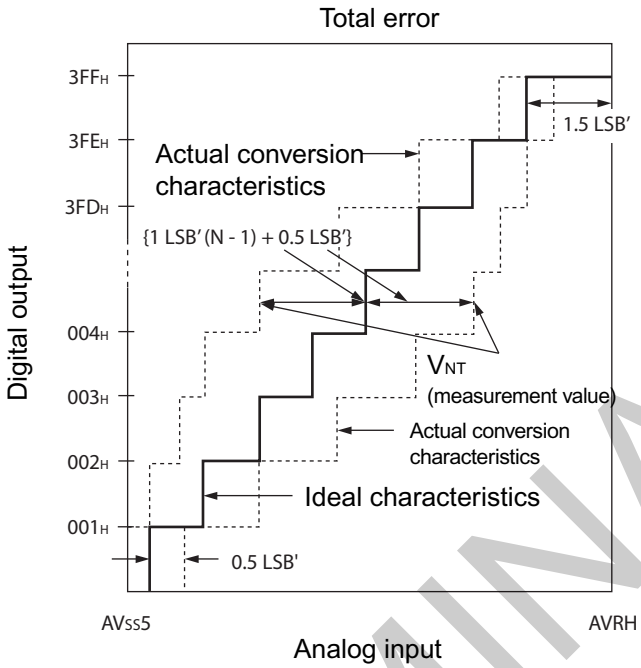
Conversion Time Calculation

$T_{conv} = T_{samp} + T_{comp}$

Definition of A/D converter terms

- Resolution
  Analog variation that is recognizable by the A/D converter.
- Linearity error
  Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B \leftrightarrow 00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B \leftrightarrow 11\ 1111\ 1111_B$).
- Differential linearity error
  Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.
- Total error
  This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and linearity error.

PRELIMINARY



- 1LSB' (ideal value) $= \frac{AVRH - AV_{SS}5}{1024}$ [V]

- Total error of digital output N $= \frac{V_{NT} - \{1\ LSB' \times (N - 1) + 0.5\ LSB'\}}{1\ LSB'}$

N : A/D converter digital output value
V_{OT}' (ideal value) = $AV_{SS}5 + 0.5$ LSB' [V]
V_{FST}' (ideal value) = AVRH – 1.5 LSB' [V]
V_{NT} : Voltage at which the digital output changes from (N + 1) H to N_H

(Continued)

PRELIMINARY

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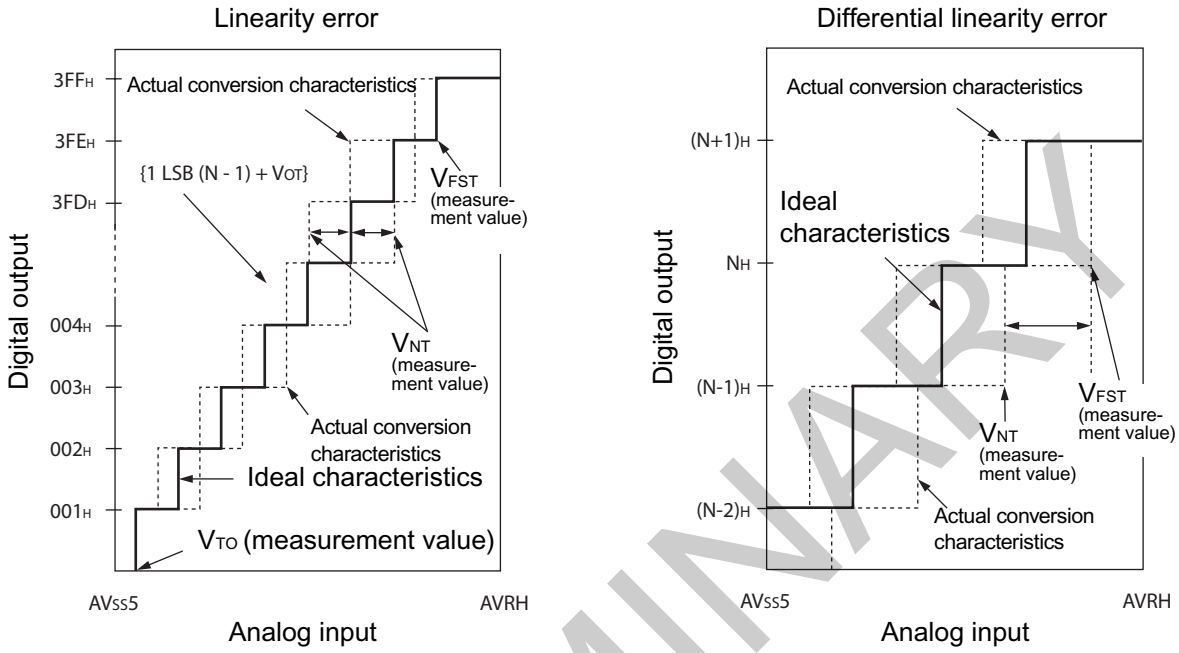


- Linearity error of digital output N $= \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB}$ [LSB]

- Differential linearity error of digital output N $= \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1$ [LSB]

- $1LSB = \frac{V_{FST} - V_{OT}}{1022}$ [V]

N : A/D converter digital output value
V_{OT} : Voltage at which the digital output changes from 000_H to 001_H.
V_{FST} : Voltage at which the digital output changes from $3FE_H$ to $3FF_H$.

PRELIMINARY

5. Alarm comparator characteristics

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	$AV_{CC}5$	—	25	40	µA	Alarm comparator enabled in fast mode (per channel) *1
	I_{A5ALMS}		—	7	10	µA	Alarm comparator enabled in normal mode (per channel) *1
	I_{A5ALMH}		—	—	5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM_n	− 1	—	+ 1	µA	T_A=25 °C
			− 3	—	+ 3	µA	T_A=105 °C
ALARM pin input voltage range	V_{ALIN}		0	—	$AV_{CC}5$	V	
Alarm upper limit voltage	V_{IAH}		$AV_{CC}5 \times 0.78$ − 3%	$AV_{CC}5 \times 0.78$	$AV_{CC}5 \times 0.78$ + 3%	V	
Alarm lower limit voltage	V_{IAL}		$AV_{CC}5 \times 0.36$ − 5%	$AV_{CC}5 \times 0.36$	$AV_{CC}5 \times 0.36$ + 5%	V	
Alarm hysteresis voltage	V_{IAHYS}		50	—	250	mV	
Alarm input resistance	R_{IN}		5	—	—	MΩ	
Comparion time	t_{COMPF}		—	0.1	0.2	µs	Alarm comparator enabled in fast mode *1
	t_{COMPS}		—	1	2	µs	Alarm comparator enabled in normal mode *1

Note: *1 : The fast Alarm Comparator mode is enabled by setting ACSR.MD=1
Setting ACSR.MD=0 sets the normal mode.

PRELIMINARY

6. FLASH memory program/erase characteristics

6.1. MB91F465DA

(T_A = 25°C, Vcc = 5.0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.9	3.6	s	Erasure programming time not included
Chip erase time	-	n*0.9	n*3.6	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	-	23	370	µs	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

6.2. MB91F467Dx

(T_A = 25°C, Vcc = 5.0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.5	2.0	s	Erasure programming time not included
Chip erase time	-	n*0.5	n*2.0	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	-	6	100	µs	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

PRELIMINARY

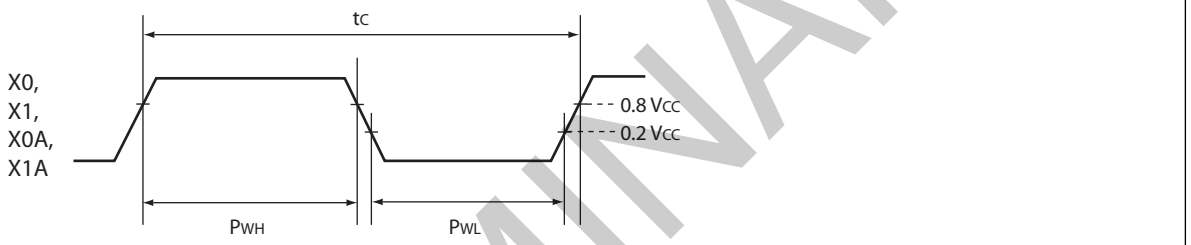
7. AC characteristics

7.1. Clock timing

($V_{DD}5$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

• Clock timing condition

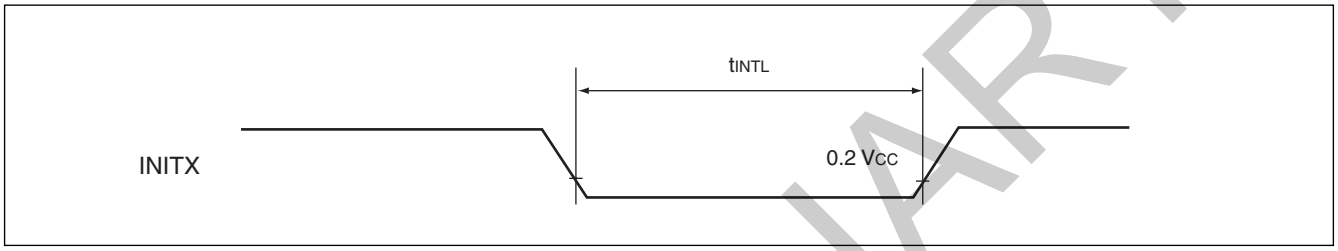


PRELIMINARY

7.2. Reset input ratings

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
INITX input time (at power-on)	t_{INTL}	INITX	—	8	—	ms
INITX input time (other than the above)				20	—	µs



PRELIMINARY

7.3. LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements
- All AC tests were measured under the following conditions:
- - IO_{drive} = 5 mA
- - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
- - $V_{SS}5$ = 0 V
- - T_a = -40 °C to +105 °C
- - C_l = 50 pF (load capacity value of pins when testing)
- - VOL = 0.2 x $V_{DD}5$,
- - VOH = 0.8 x $V_{DD}5$
- - EPILR = 0, PILR = 1 (Automotive Level = worst case)

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

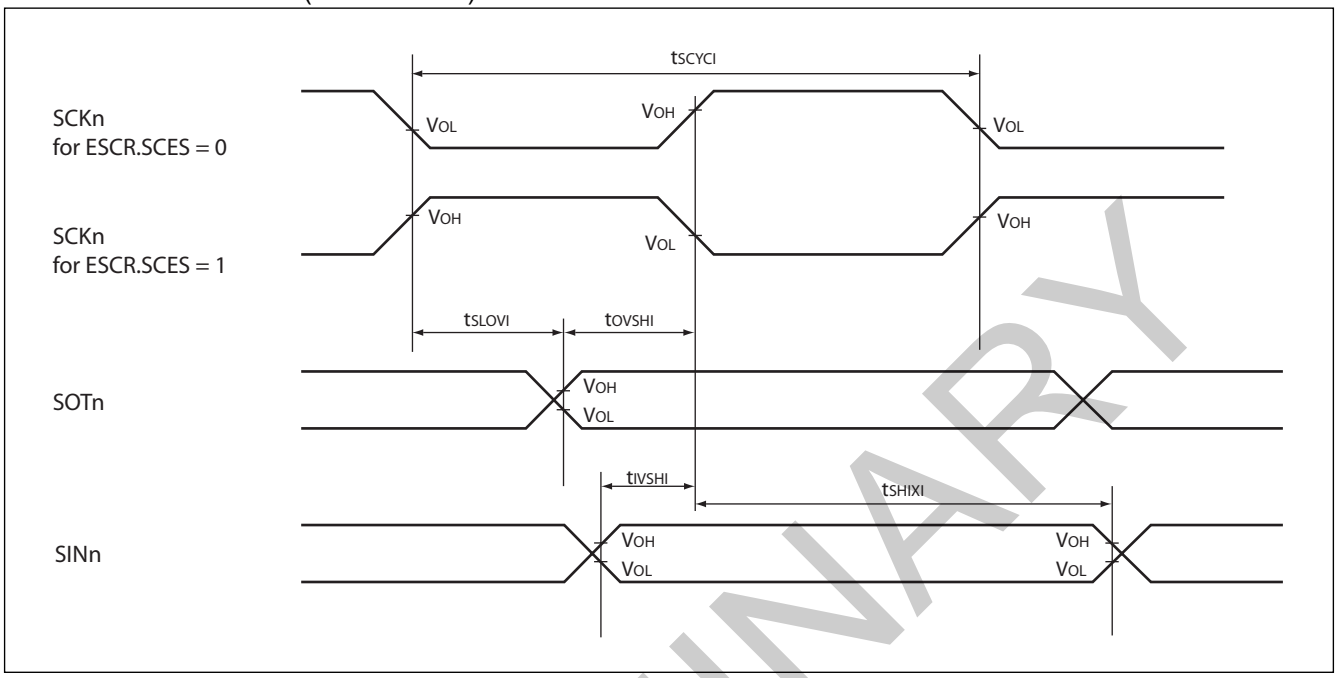
Parameter	Symbol	Pin name	Condition	$V_{DD}5$ = 3.0 V to 4.5 V		$V_{DD}5$ = 4.5 V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal clock operation (master mode)	4 t_{CLKP}	—	4 t_{CLKP}	—	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn SOTn		– 30	30	– 20	20	ns
SOT → SCK ↓ delay time	t_{OVSHI}	SCKn SOTn		m × t_{CLKP} – 30*	—	m × t_{CLKP} – 20*	—	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKn SINn		t_{CLKP} + 55	—	t_{CLKP} + 45	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXI}	SCKn SINn		0	—	0	—	ns
Serial clock “H” pulse width	t_{SHSLE}	SCKn	External clock operation (slave mode)	t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
Serial clock “L” pulse width	t_{SLSHE}	SCKn		t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn SOTn		—	2 t_{CLKP} + 55	—	2 t_{CLKP} + 45	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKn SINn		10	—	10	—	ns
SCK ↑ → valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP} + 10	—	t_{CLKP} + 10	—	ns
SCK rising time	t_{FE}	SCKn		—	20	—	20	ns
SCK falling time	t_{RE}	SCKn		—	20	—	20	ns

* : Parameter m depends on t_{SCYCI} and can be calculated as :
- if t_{SCYCI} = 2*k*t_{CLKP}, then m = k, where k is an integer > 2
- if t_{SCYCI} = (2*k + 1)*t_{CLKP}, then m = k + 1, where k is an integer > 1

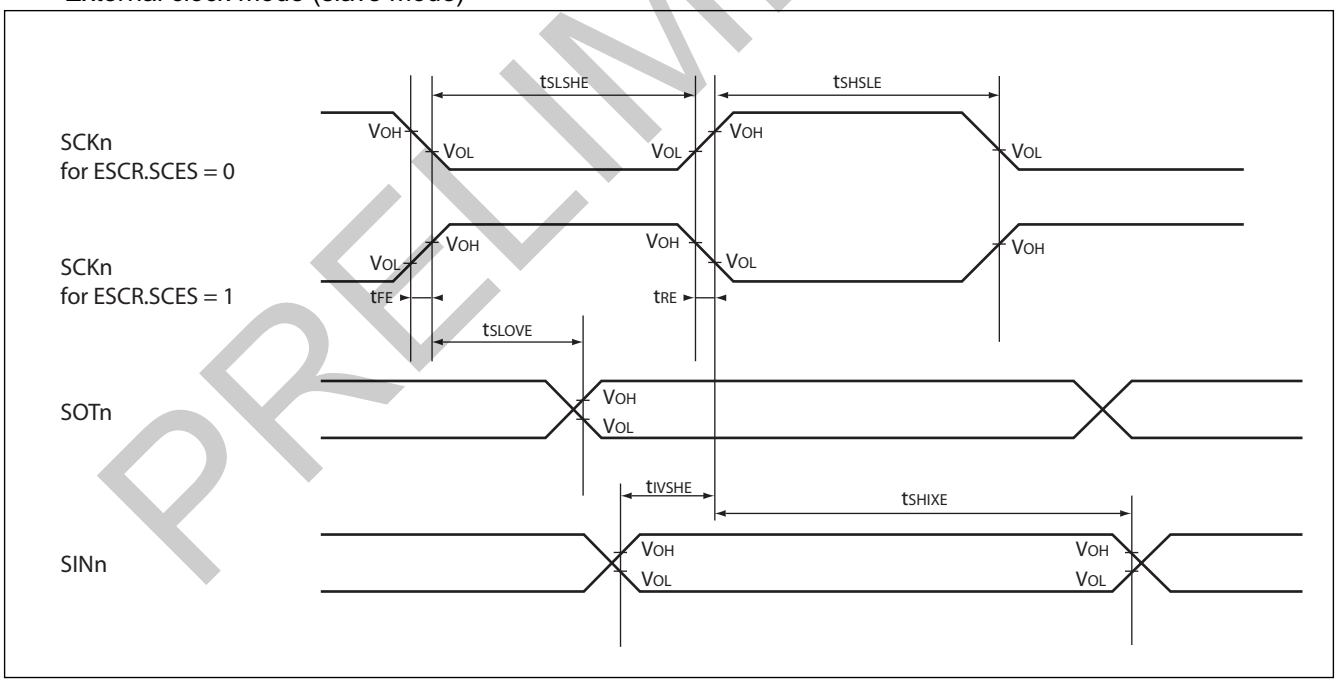
Notes :
- The above values are AC characteristics for CLK synchronous mode.
- t_{CLKP} is the cycle time of the peripheral clock.

PRELIMINARY

• Internal clock mode (master mode)



• External clock mode (slave mode)



PRELIMINARY

7.4. I²C AC Timings at $V_{DD}5$ = 3.0 to 5.5 V

- Conditions during AC measurements
  All AC tests were measured under the following conditions:
  - IO_{drive} = 3 mA
  - $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA (V_{DD} = 4.5 V to 5.5 V for MB91F467Dx)
  - $V_{SS}5$ = 0 V
  - Ta = − 40 °C to + 105 °C
  - C_l = 50 pF
  - VOL = 0.3 × $V_{DD}5$,
    VOH = 0.7 × $V_{DD}5$
  - EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × $V_{DD}5$/0.7 × $V_{DD}5$)

Fast mode:

($V_{DD}5$ = 3.5 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

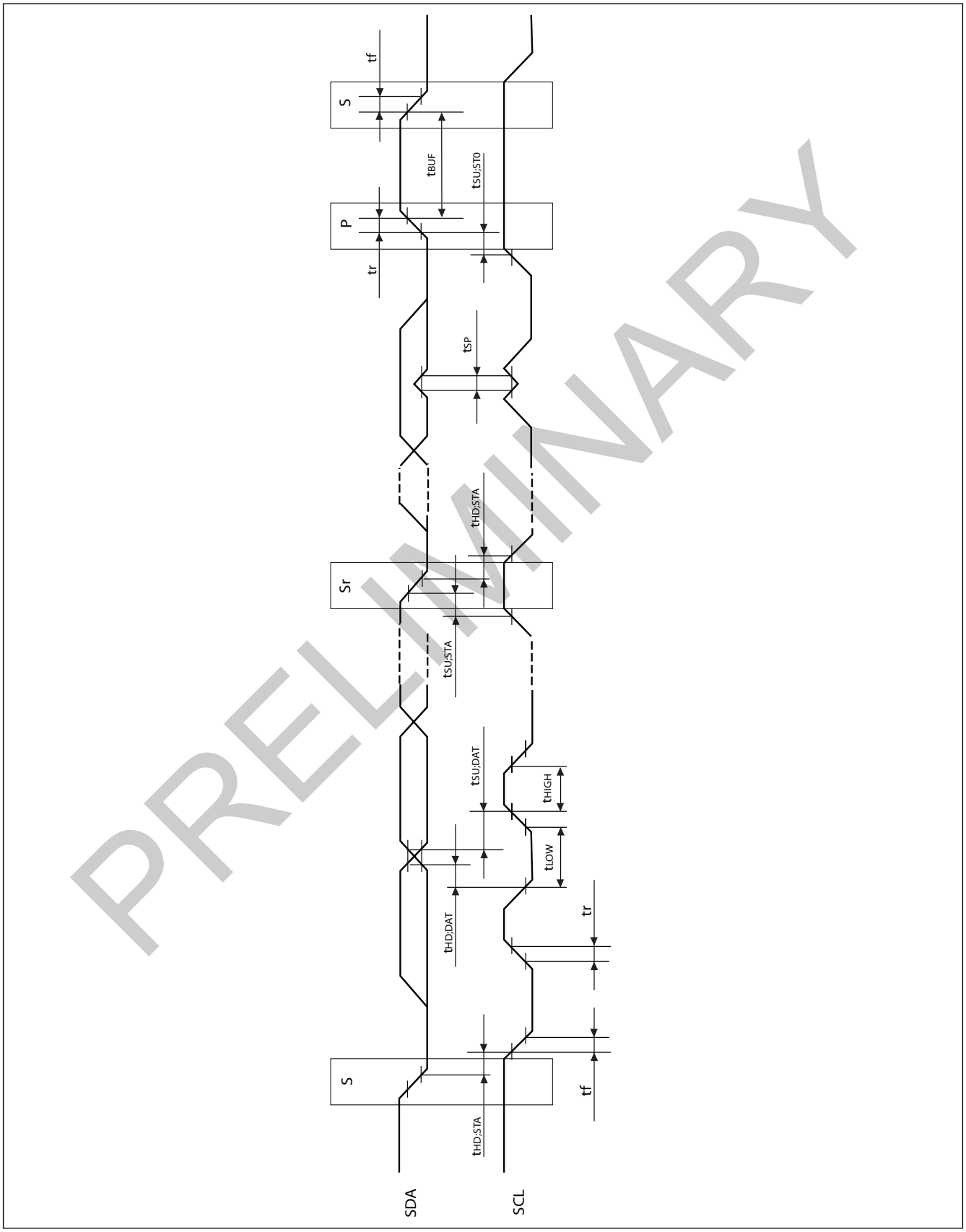
Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f_{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	SCLn, SDAn	0.6	—	µs	
LOW period of the SCL clock	t_{LOW}	SCLn	1.3	—	µs	
HIGH period of the SCL clock	t_{HIGH}	SCLn	0.6	—	µs	
Setup time for a repeated START condition	$t_{SU;STA}$	SCLn, SDAn	0.6	—	µs	
Data hold time for I²C-bus devices	$t_{HD;DAT}$	SCLn, SDAn	0	0.9	µs	
Data setup time	$t_{SU;DAT}$	SCLn SDAn	100	—	ns	
Rise time of both SDA and SCL signals	t_r	SCLn, SDAn	20 + 0.1Cb	300	ns	*1
Fall time of both SDA and SCL signals	t_f	SCLn, SDAn	20 + 0.1Cb	300	ns	*1
Setup time for STOP condition	$t_{SU;STO}$	SCLn, SDAn	0.6	—	µs	
Bus free time between a STOP and START condition	t_{BUF}	SCLn, SDAn	1.3	—	µs	
Capacitive load for each bus line	C_b	SCLn, SDAn	—	400	pF	
Pulse width of spike suppressed by input filter	t_{SP}	SCLn, SDAn	0	(1..1.5) × t_{CLKP}	ns	*2

*1 On MB91F467Dx only guaranteed for 4.5 V < $V_{DD}5$ < 5.5 V.

*2 The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I2C signals (SDA, SCL) and peripheral clock.

Note: t_{CLKP} is the cycle time of the peripheral clock.

PRELIMINARY



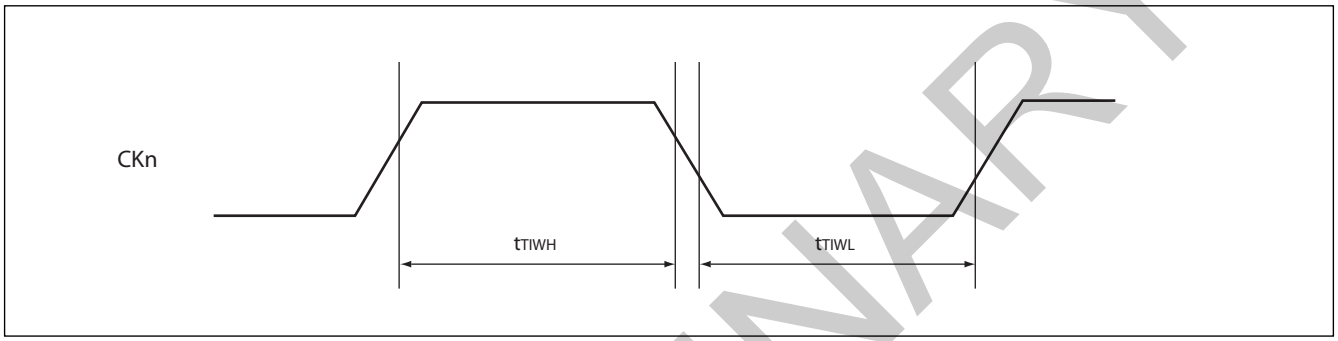
PRELIMINARY

7.5. Free-run timer clock

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input pulse width	t_{TIWH} t_{TIWL}	CKn	—	$4t_{CLKP}$	—	ns

Note : t_{CLKP} is the cycle time of the peripheral clock.

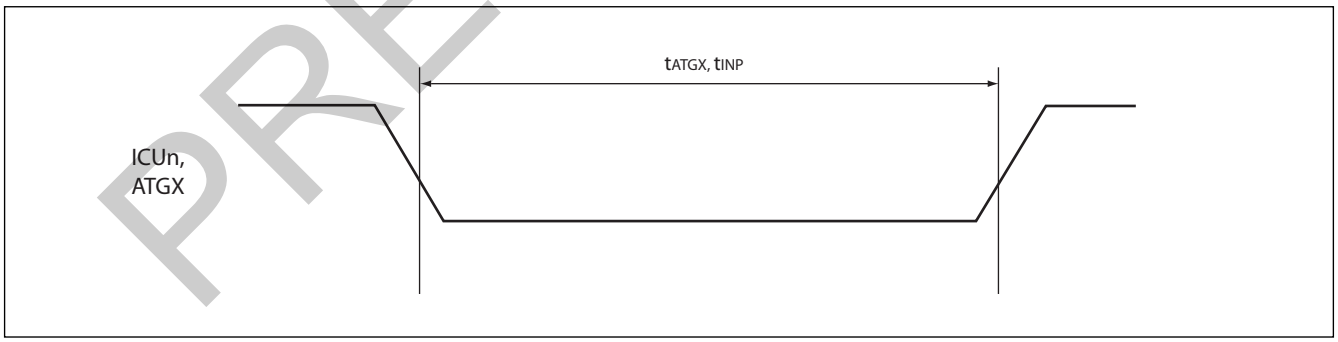


7.6. Trigger input timing

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit
				Min	Max	
Input capture input trigger	t_{INP}	ICUn	—	$5t_{CLKP}$	—	ns
A/D converter trigger	t_{ATGX}	ATGX	—	$5t_{CLKP}$	—	ns

Note : t_{CLKP} is the cycle time of the peripheral clock.



PRELIMINARY

7.7. External Bus AC Timings at $V_{DD}35$ = 4.5 to 5.5 V

- Conditions during AC measurements
  All AC tests were measured under the following conditions:
  - IO_{drive} = 5 mA
  - $V_{DD}35$ = 4.5 V to 5.5 V, I_{load} = 5 mA
  - $V_{SS}5$ = 0 V
  - Ta = – 40 °C to + 105 °C
  - C_l = 50 pF
  - VOL = 0.2 × $V_{DD}35$,
    VOH = 0.8 × $V_{DD}35$
  - EPILR = 0, PILR = 1 (Automotive Level = worst case)

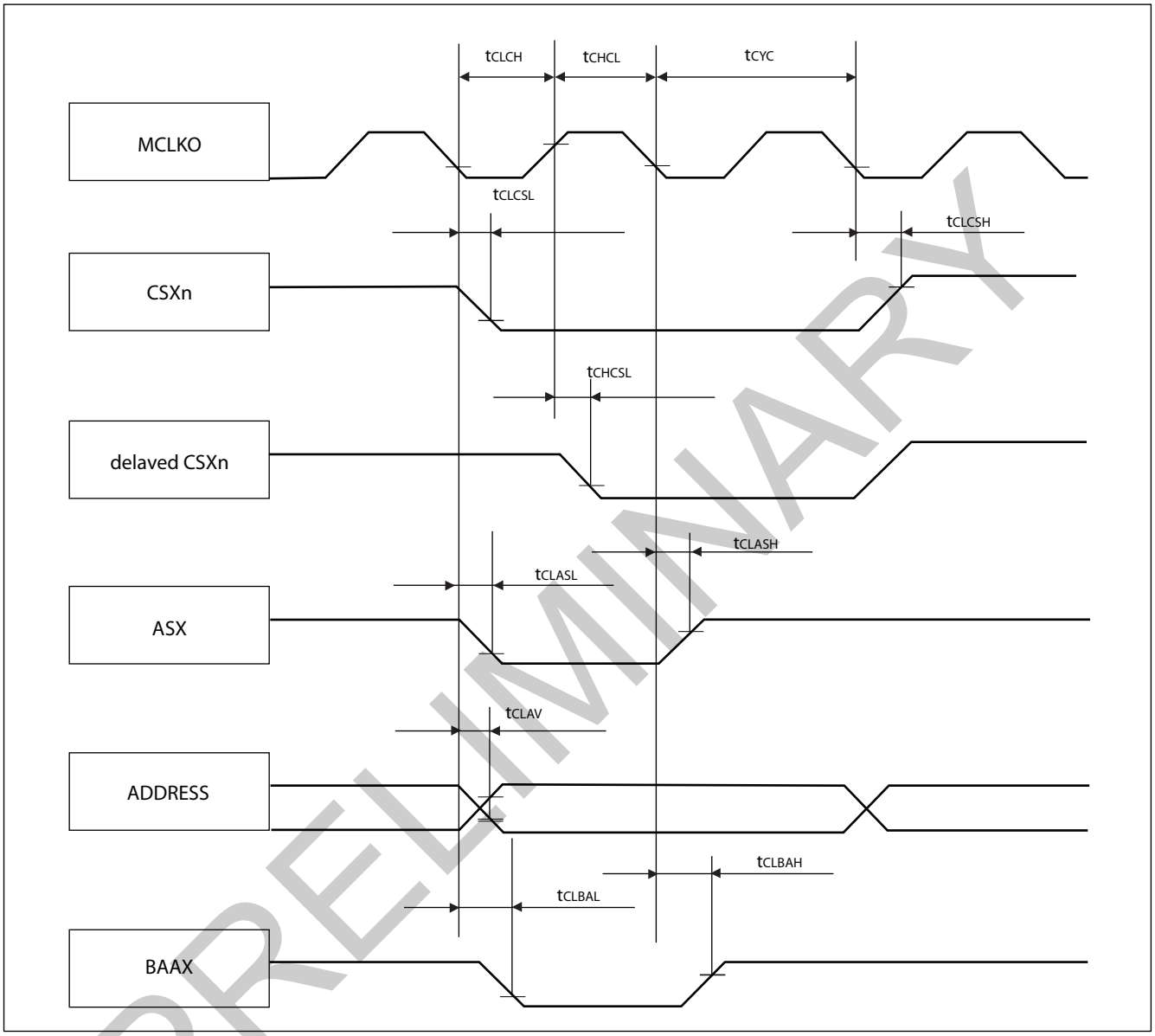
7.7.1. Basic Timing

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO	t_{CLCH}	MCLKO	1/2 x t_{CLKT} – 7	1/2 × t_{CLKT} + 7	ns
	t_{CHCL}		1/2 × t_{CLKT} – 7	1/2 × t_{CLKT} + 7	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	—	9	ns
	t_{CLCSH}		—	8	ns
MCLKO ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		– 5	+ 2	ns
MCLKO ↓ to ASX delay time	t_{CLASL}	MCLKO ASX	—	8	ns
	t_{CLASH}		—	8	ns
MCLKO ↓ to BAAX delay time	t_{CLBAL}	MCLKO BAAX	—	5	ns
	t_{CLBAH}		1	—	ns
MCLKO ↓ to Address valid delay time	t_{CLAV}	MCLKO A25 to A0	—	11	ns

Note : t_{CLKT} is the cycle time of the external bus clock.

PRELIMINARY



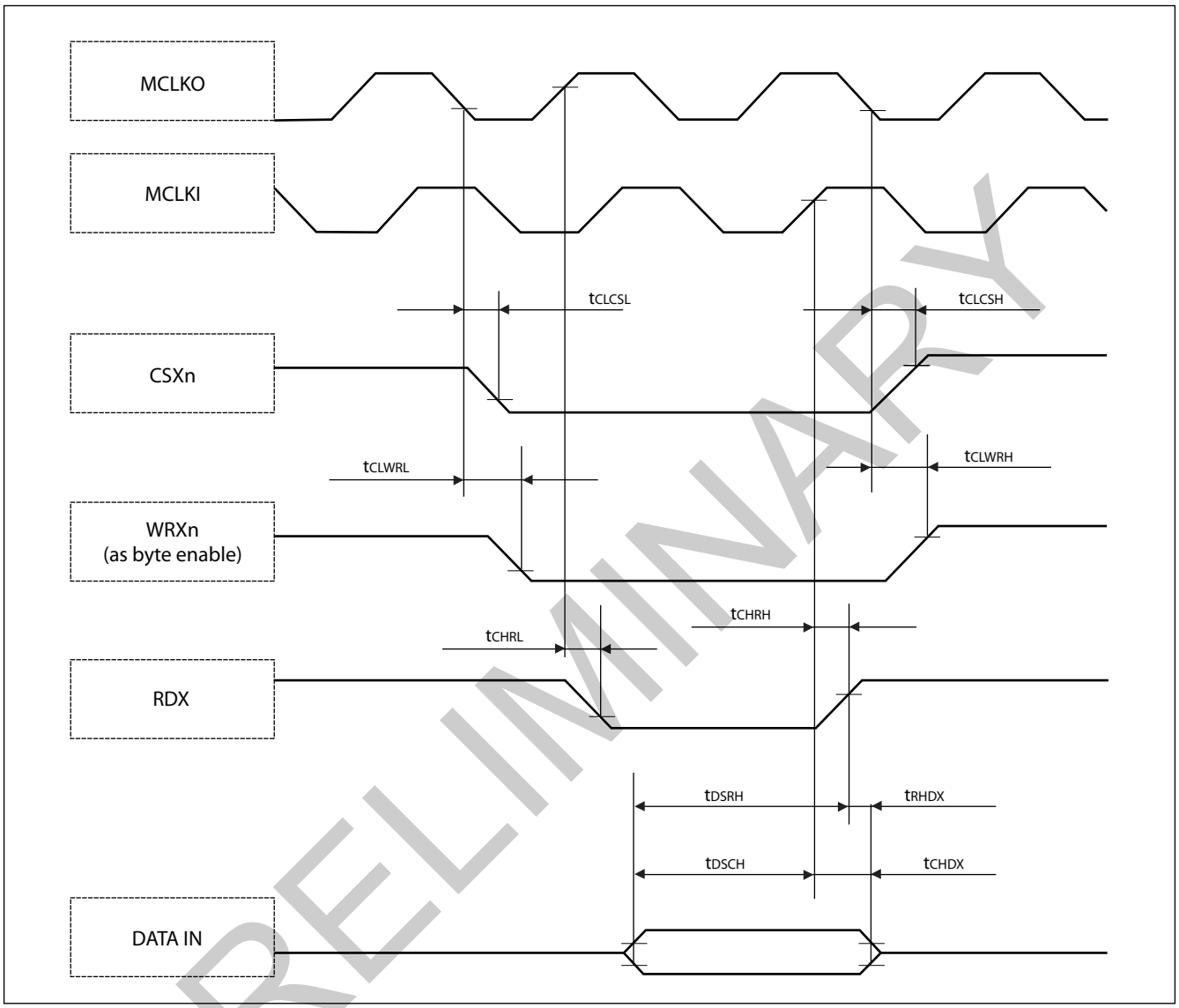
PRELIMINARY

7.7.2. Synchronous/Asynchronous read access with external MCLKI input

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↑ /MCLKI ↑ to RDX delay time	t_{CHRL}	MCLKO RDX	– 5	2	ns
	t_{CHRH}	MCLKI RDX	8	16	ns
Data valid to RDX ↑ setup time	t_{DSRH}	RDX D31 to D0	19	—	ns
RDX ↑ to Data valid hold time (external MCLKI input)	t_{RHDX}	RDX D31 to D0	0	—	ns
Data valid to MCLKI ↑ setup time	t_{DSCH}	MCLKI D31 to D0	3	—	ns
MCLKI ↑ to Data valid hold time	t_{CHDX}	MCLKI D31 to D0	1	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	t_{CLWRL}	MCLKO WRXn	—	9	ns
	t_{CLWRH}		– 1	—	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	—	9	ns
	t_{CLCSH}		—	8	ns

PRELIMINARY

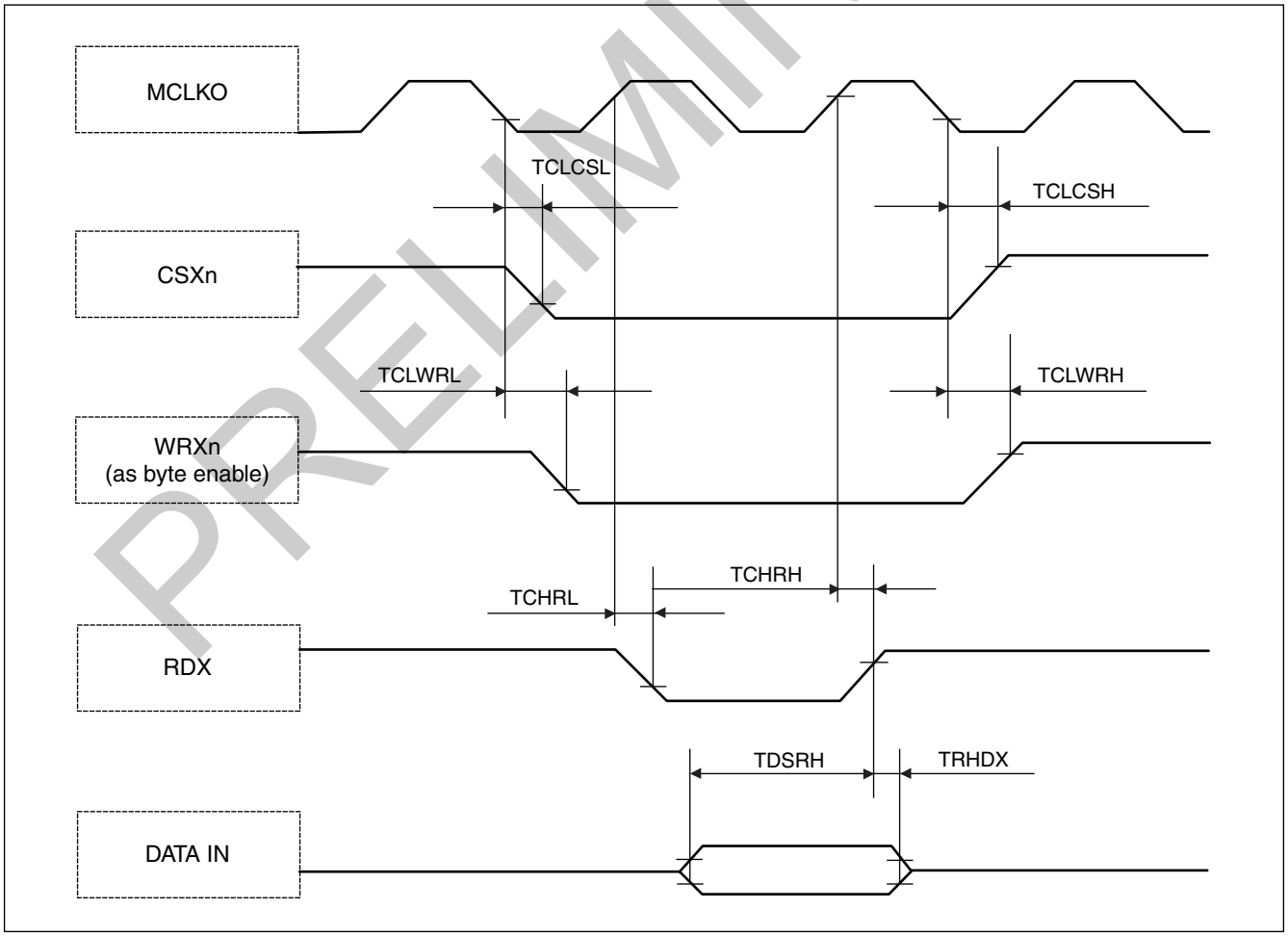


PRELIMINARY

7.7.3. Synchronous/Asynchronous read access with internal MCLKO --> MCLKI feedback

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↑ to RDX delay time	TCHRL	MCLKO RDX	– 5	2	ns
	TCHRH		– 5	2	ns
Data valid to RDX ↑ setup time	TDSRH	RDX D31 to D0	20	—	ns
RDX ↑ to Data valid hold time (internal MCLKO → MCLKI / /MCLKI feedback)	TRHDX	RDX D31 to D0	0	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	TCLWRL	MCLKO WRXn	—	9	ns
	TCLWRH		– 1	—	ns
MCLKO ↓ to CSXn delay time	TCLCSL	MCLKO CSXn	—	9	ns
	TCLCSH		—	8	ns

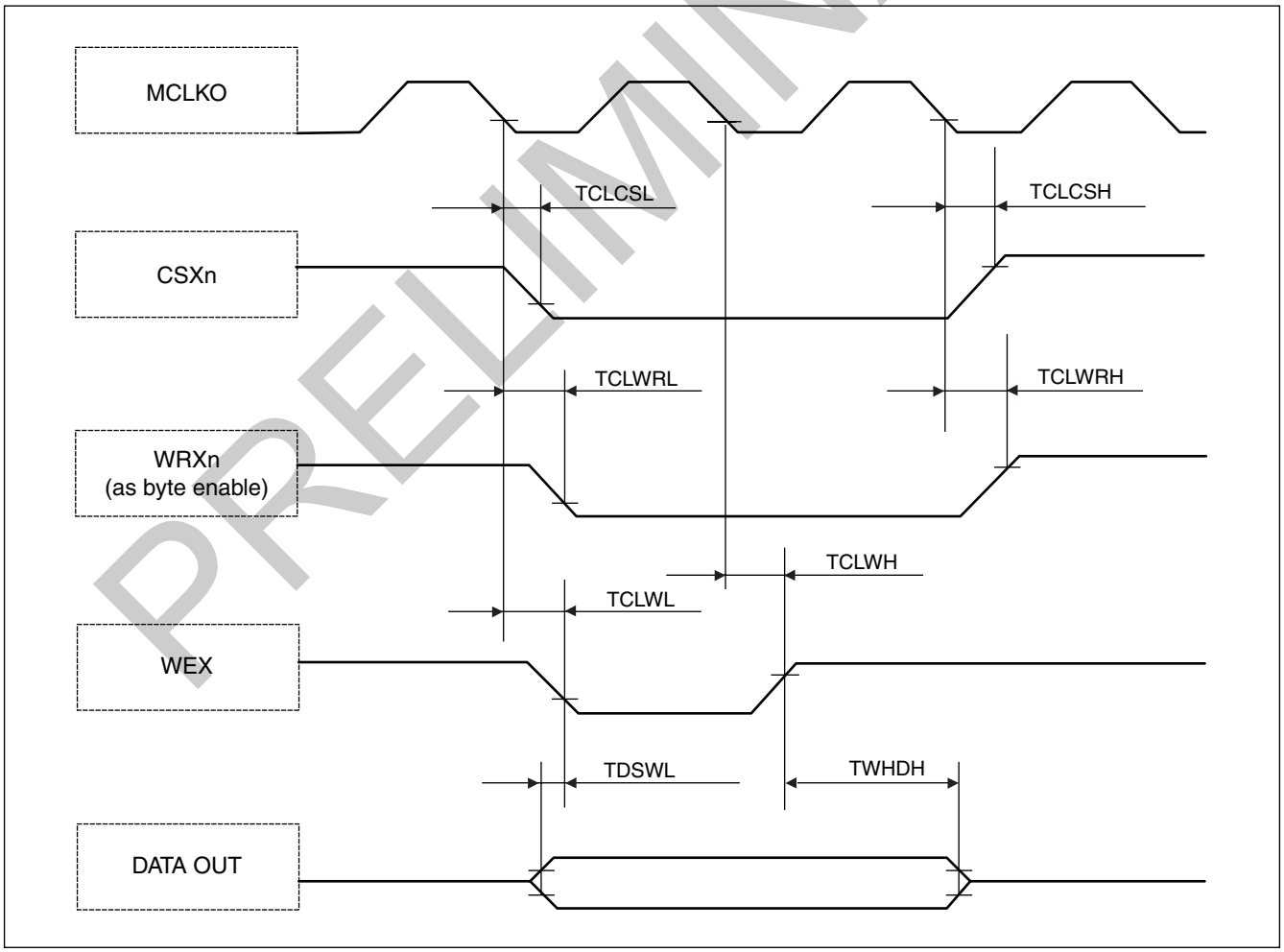


PRELIMINARY

7.7.4. Synchronous write access - byte control type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WEX delay time	TCLWL	MCLKO WEX	—	9	ns
	TCLWH		2	—	ns
Data valid to WEX ↓ setup time	TDSWL	WEX D31 to D0	– 11	—	ns
WEX ↑ to Data valid hold time	TWHDH	WEX D31 to D0	t_{CLKT} – 10	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	TCLWRL	MCLKO WRXn	—	9	ns
	TCLWRH		– 1	—	ns
MCLKO ↓ to CSXn delay time	TCLCSL	MCLKO CSXn	—	9	ns
	TCLCSH		—	8	ns

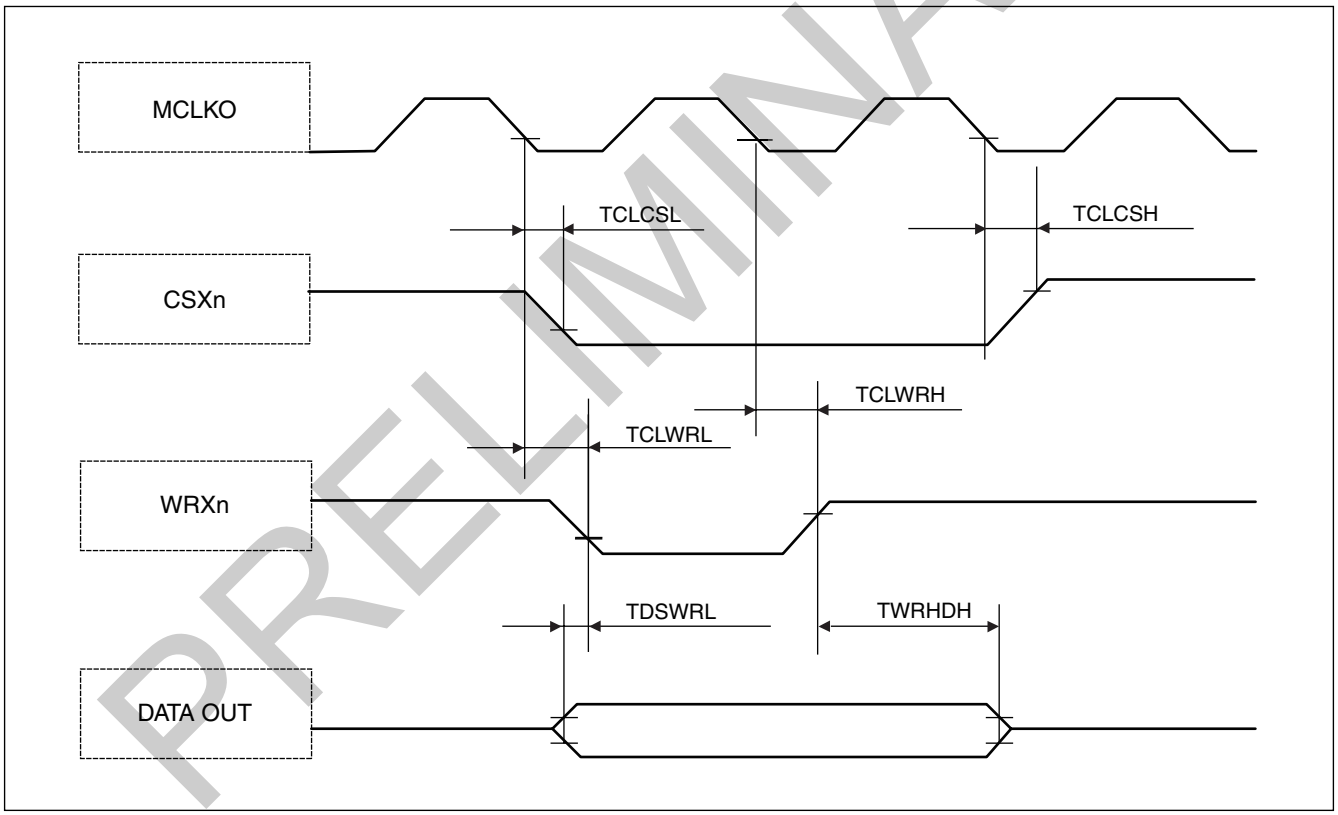


PRELIMINARY

7.7.5. Synchronous write access - no byte control type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WRXn delay time	TCLWRL	MCLKO WRXn	—	9	ns
	TCLWRH		– 1	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D0	– 12	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D0	t_{CLKT} – 8	—	ns
MCLKO ↓ to CSXn delay time	TCLCSL	MCLKO CSXn	—	9	ns
	TCLCSH		—	8	ns

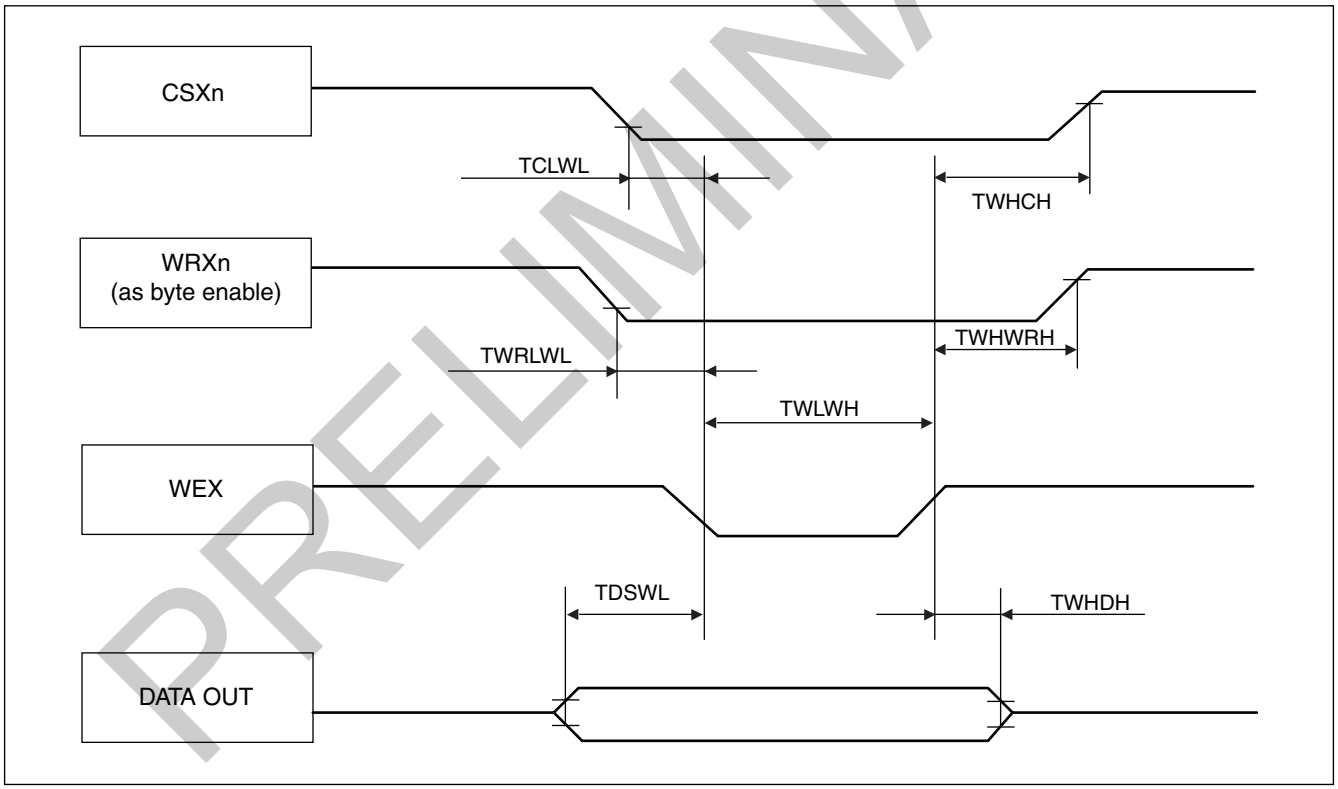


PRELIMINARY

7.7.6. Asynchronous write access - byte control type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	TWLWH	WEX	t_{CLKT} – 2	—	ns
Data valid to WEX ↓ setup time	TDSWL	WEX D31 to D0	1/2 × t_{CLKT} – 13	—	ns
WEX ↑ to Data valid hold time	TWHDH	WEX D31 to D0	1/2 × t_{CLKT} – 10	—	ns
WEX to WRXn delay time	TWRLWL	WEX WRXn	—	1/2 × t_{CLKT} + 2	ns
	TWHWRH		1/2 × t_{CLKT} – 4	—	ns
WEX to CSXn delay time	TCLWL	WEX CSXn	—	1/2 × t_{CLKT}	ns
	TWHCH		1/2 × t_{CLKT} – 5	—	ns

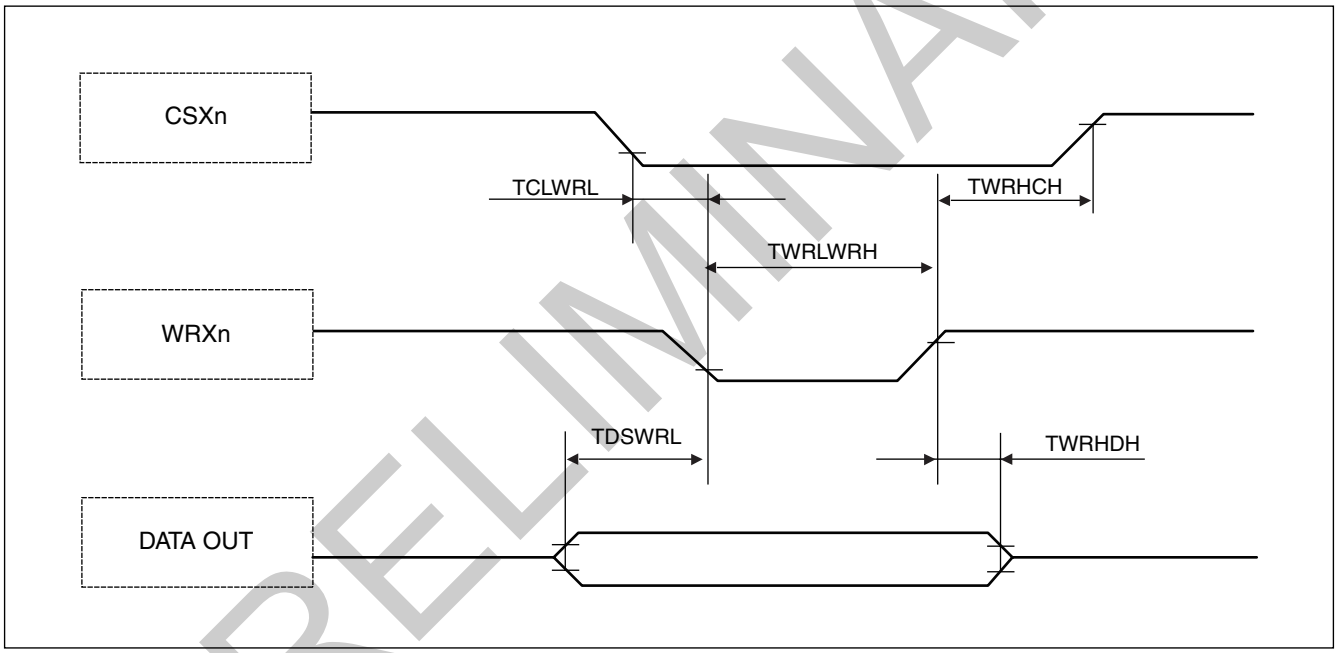


PRELIMINARY

7.7.7. Asynchronous write access - no byte control type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	TWRLWRH	WRXn	t_{CLKT} – 1	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D0	1/2 × t_{CLKT} – 14	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D0	1/2 × t_{CLKT} – 7	—	ns
WRXn to CSXn delay time	TCLWRL	WRXn CSXn	—	1/2 × t_{CLKT} – 1	ns
	TWRHCH		1/2 × t_{CLKT} – 3	—	ns

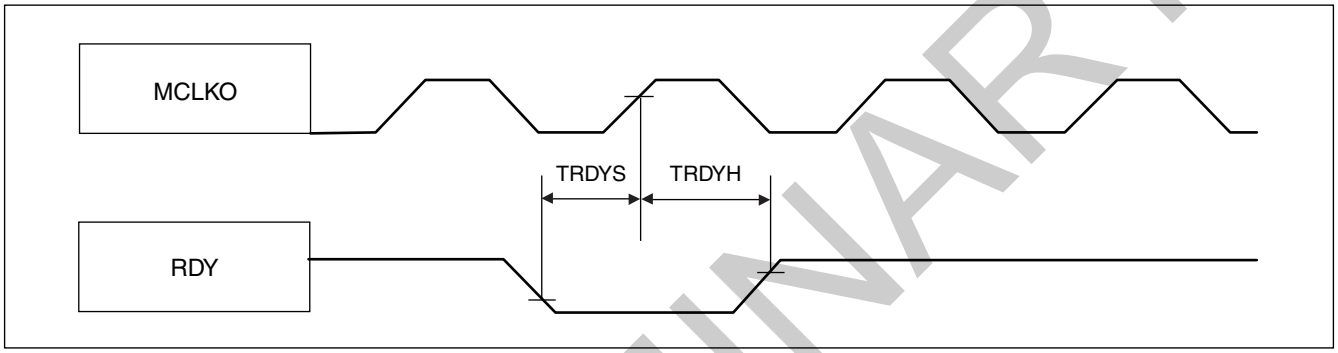


PRELIMINARY

7.7.8. RDY waitcycle insertion

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	TRDYS	MCLKO RDY	21	—	ns
RDY hold time	TRDYH	MCLKO RDY	0	—	ns



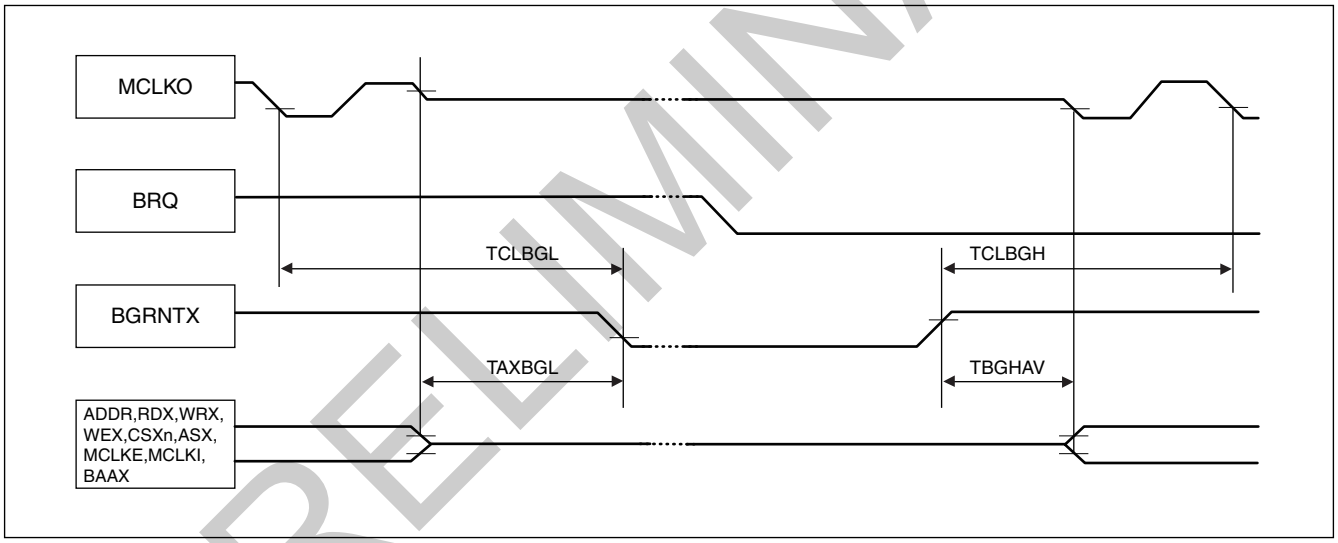
PRELIMINARY

7.7.9. Bus hold timing

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to BGRNTX delay time	TCLBGL	MCLKO BGRNTX	—	$2 \times t_{CLKT} + 5$	ns
	TCLBGH		—	$2 \times t_{CLKT} + 2$	ns
Bus HIZ to BGRNTX ↓	TAXBGL	BGRNTX MCLK* A0 to An RDX, ASX WRXn,WEX CSXn,BAAX	$t_{CLKT} - 6$	—	ns
BGRNTX ↑ to Bus drive	TBGHAV		$t_{CLKT} + 8$	—	ns

Note : BRQ must be kept High until the bus is granted (this is acknowledged by the falling edge of BGRNTX).
It must be kept High as long as the bus shall be hold.
After releasing the bus (BRQ set to Low) this is acknowledged by the rising edge of BGRNTX.

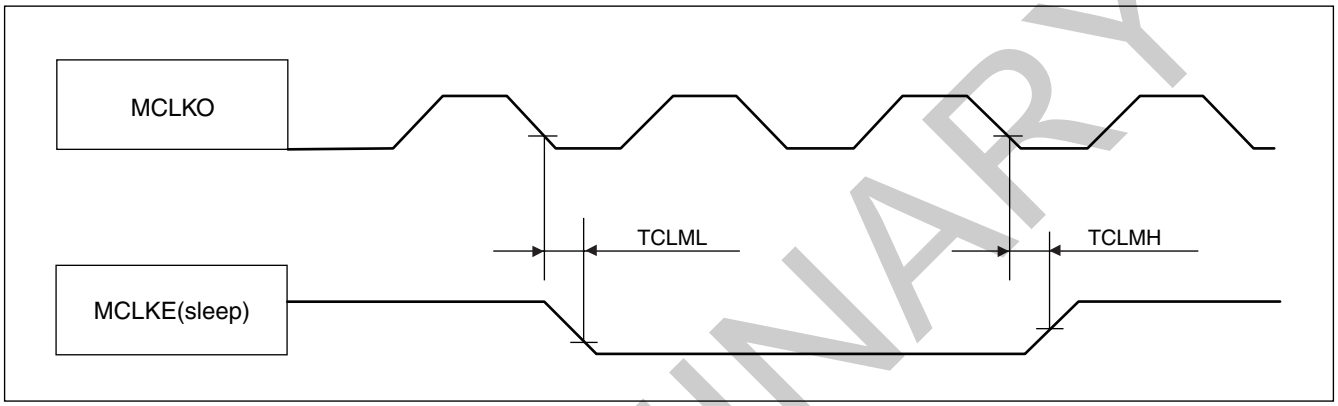


PRELIMINARY

7.7.10. Clock relationships

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to MCLKE (in sleep mode)	TCLML	MCLKO MCLKE	—	7	ns
	TCLMH		– 1	—	ns



PRELIMINARY

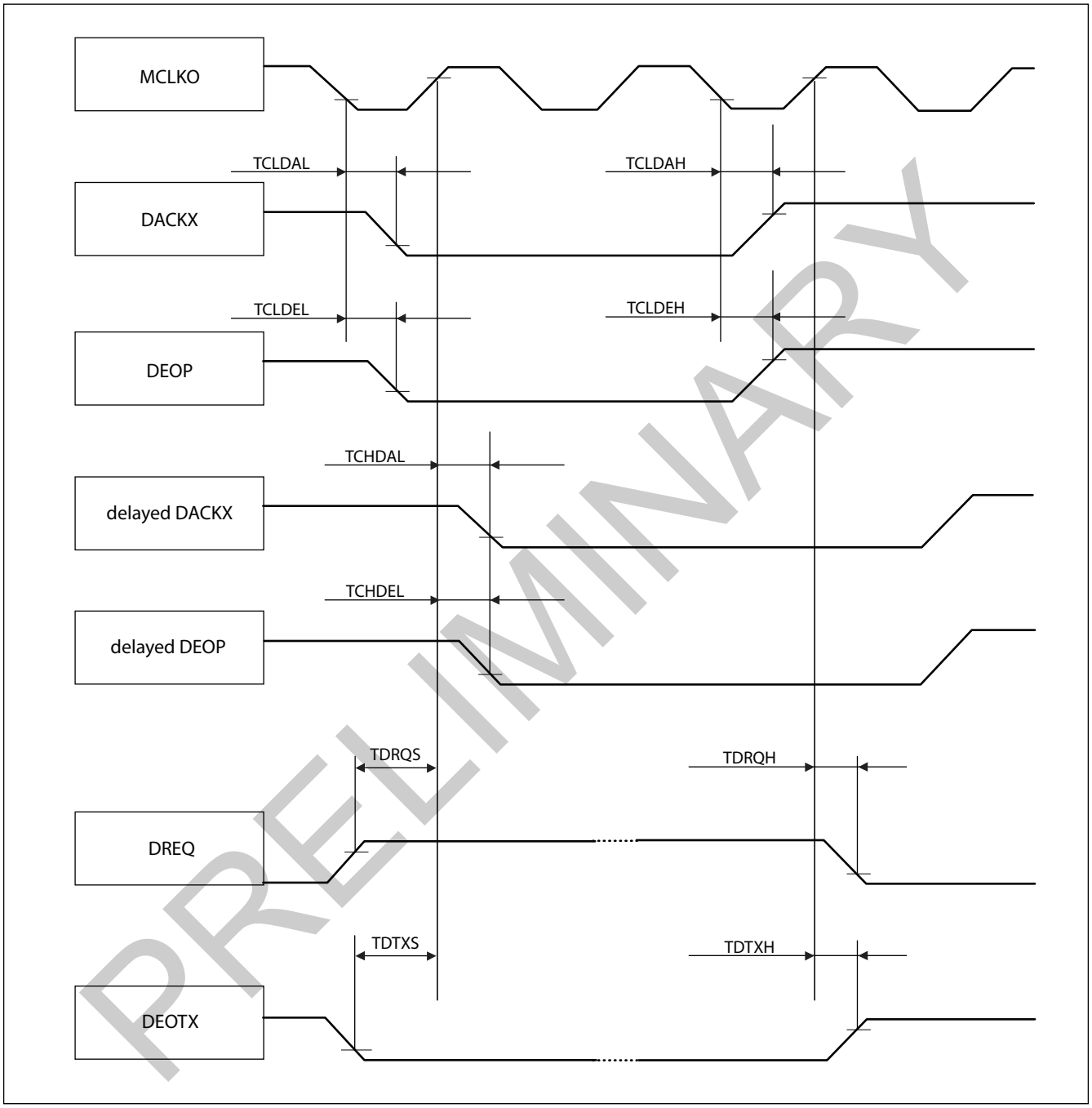
7.7.11. DMA transfer

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to DACKX delay time	TCLDAL	MCLKO DACKXn	—	9	ns
	TCLDAH		—	6	ns
MCLKO ↓ to DEOP delay time	TCLDEL	MCLKO DEOPn	—	8	ns
	TCLDEH		—	9	ns
MCLKO ↑ to DACKX delay time (ADDR → delayed CS)	TCHDAL	MCLKO DACKXn	– 4	3	ns
MCLKO ↑ to DEOP delay time (ADDR → delayed CS)	TCHDEL	MCLKO DEOPn	– 4	3	ns
DREQ setup time	TDRQS	MCLKO DREQn	23	—	ns
DREQ hold time	TDRQH	MCLKO DREQn	0	—	ns
DEOTXn setup time	TDTXS	MCLKO DEOTXn	24	—	ns
DEOTXn hold time	TDTXH	MCLKO DEOTXn	0	—	ns

Note : DREQ and DEOTX must be applied for at least 5 × t_{CLKT} to ensure that they are really sampled and evaluated. Under best case conditions (DMA not busy) only setup and hold times are required.

PRELIMINARY



PRELIMINARY

7.8. External Bus AC Timings at $V_{DD}35$ = 3.0 to 4.5 V

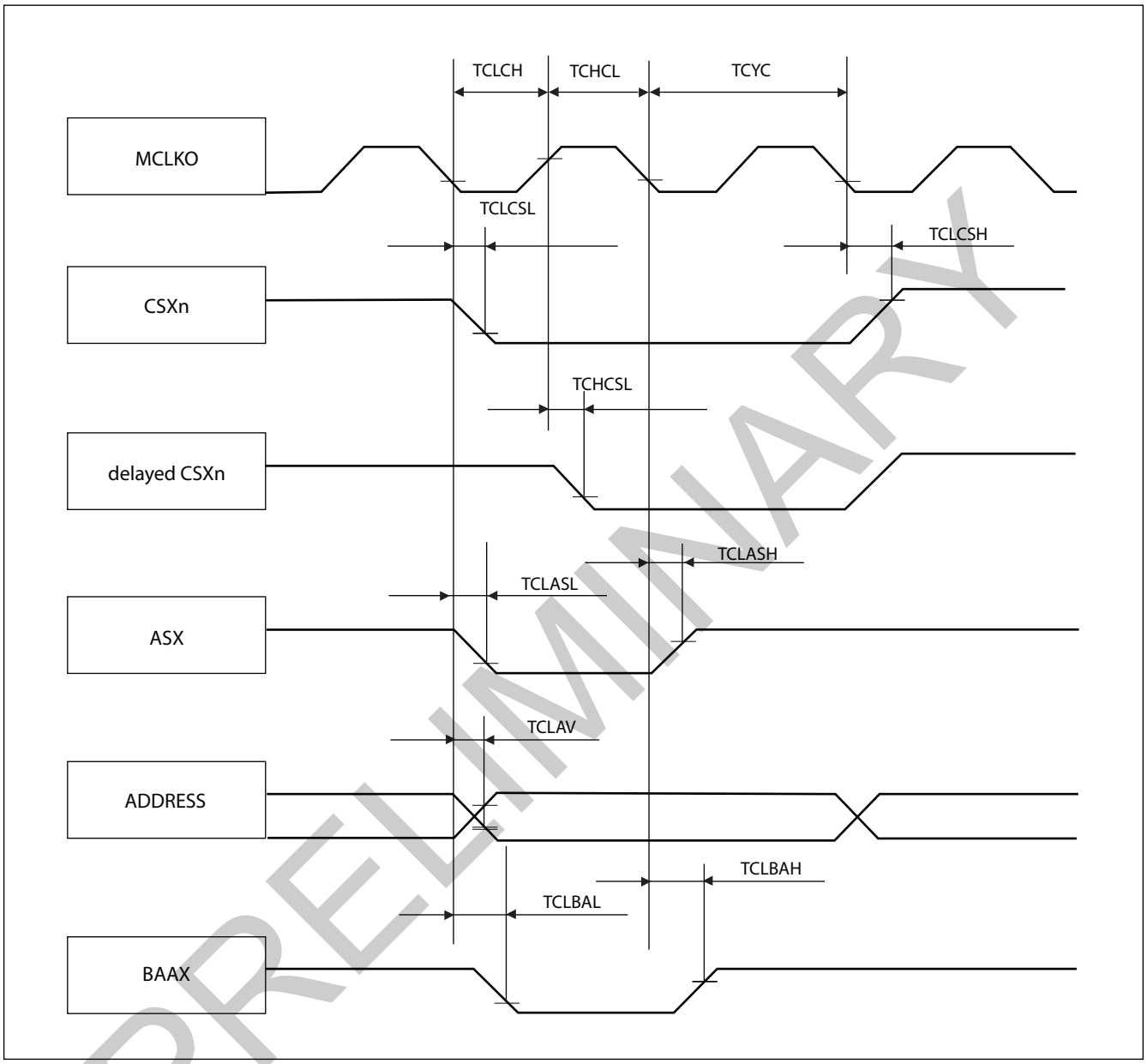
- Conditions during AC measurements
  All AC tests were measured under the following conditions:
  - IO_{drive} = 5 mA
  - $V_{DD}35$ = 3.0 V to 4.5 V, I_{load} = 3 mA
  - $V_{SS}5$ = 0 V
  - Ta = – 40 °C to + 105 °C
  - C_l = 50 pF
  - VOL = 0.2 × $V_{DD}35$,
    VOH = 0.8 × $V_{DD}35$
  - EPILR = 0, PILR = 1 (Automotive Level = worst case)

7.8.1. Basic Timing

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO	TCLCH	MCLKO	1/2 × t_{CLKT} – 13	1/2 × t_{CLKT} + 13	ns
	TCHCL		1/2 × t_{CLKT} – 13	1/2 × t_{CLKT} + 13	ns
MCLKO ↓ to CSXn delay time	TCLCSL	MCLKO CSXn	—	6	ns
	TCLCSH		—	7	ns
MCLKO ↑ to CSXn delay time (Addr → CS delay)	TCHCSL		– 11	0	ns
MCLKO ↓ to ASX delay time	TCLASL	MCLKO ASX	—	6	ns
	TCLASH		—	9	ns
MCLKO ↓ to BAAX delay time	TCLBAL	MCLKO BAAX	—	3	ns
	TCLBAH		1	—	ns
MCLKO ↓ to Address valid delay time	TCLAV	MCLKO A25 to A0	—	13	ns

PRELIMINARY



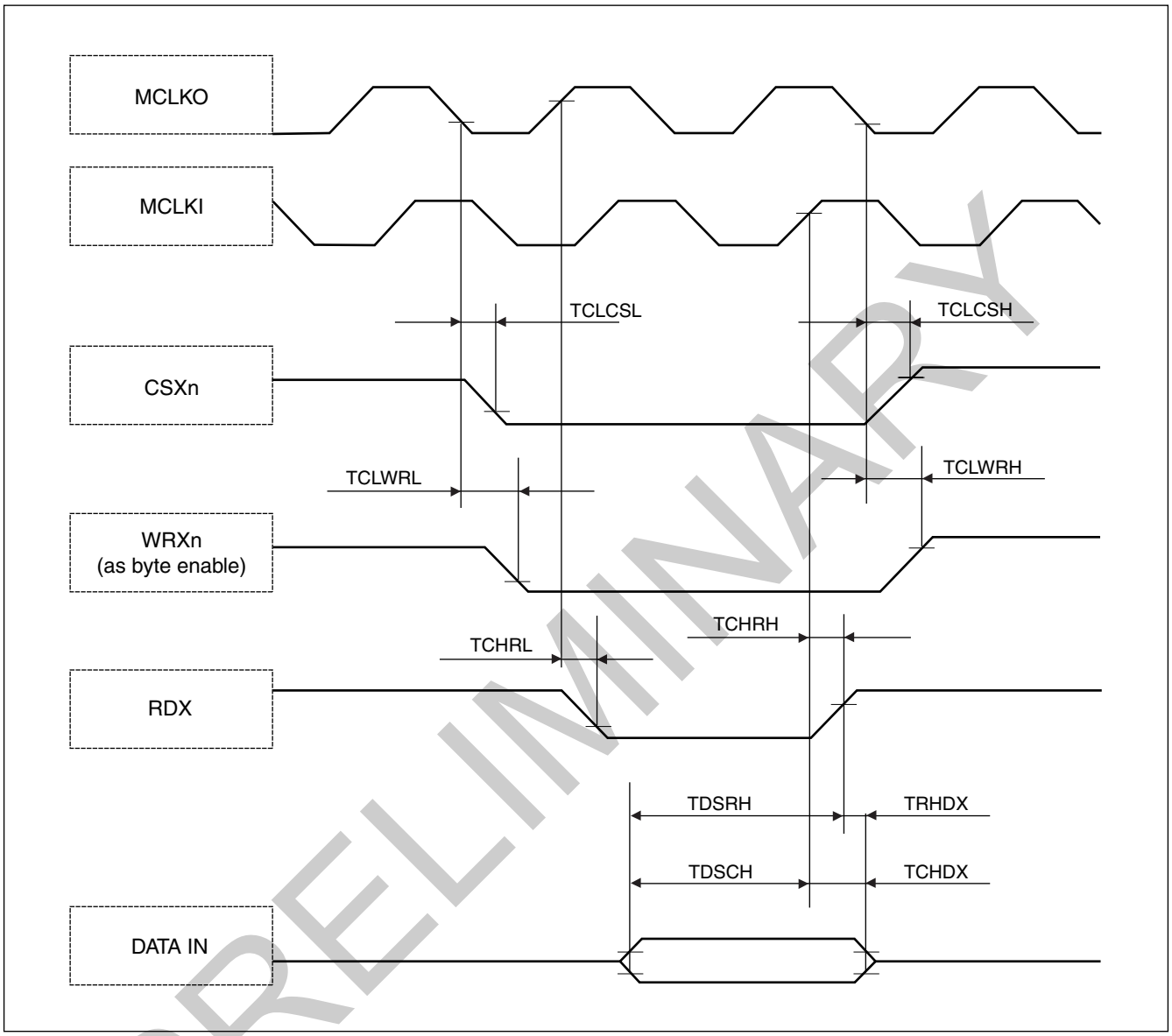
PRELIMINARY

7.8.2. Synchronous/Asynchronous read access with external MCLKI input

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↑/MCLKI ↑ to RDX delay time	TCHRL	MCLKO RDX	– 12	0	ns
	TCHRH	MCLKI RDX	12	26	ns
Data valid to RDX ↑ setup time	TDSRH	RDX D31 to D0	28	—	ns
RDX ↑ to Data valid hold time (external MCLKI input)	TRHDX	RDX D31 to D0	0	—	ns
Data valid to MCLKI ↑ setup time	TDSCH	MCLKI D31 to D0	3	—	ns
MCLKI ↑ to Data valid hold time	TCHDX	MCLKI D31 to D0	1	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	TCLWRL	MCLKO WRXn	—	6	ns
	TCLWRH		0	—	ns
MCLKO ↓ to CSXn delay time	TCLCSL	MCLKO CSXn	—	6	ns
	TCLCSH		—	7	ns

PRELIMINARY

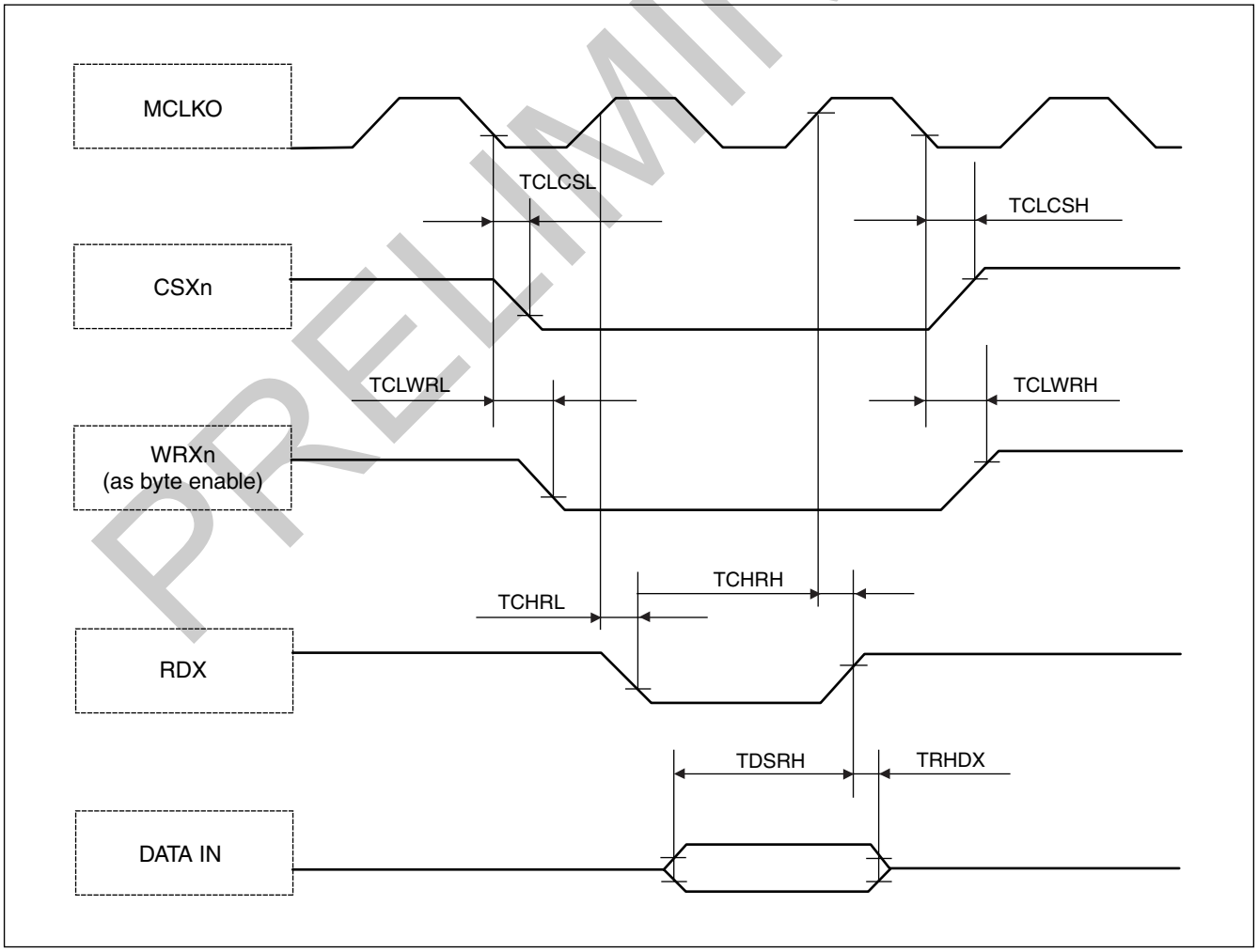


PRELIMINARY

7.8.3. Synchronous/Asynchronous read access with internal MCLKO --> MCLKI feedback

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↑ to RDX delay time	TCHRL	MCLKO RDX	– 12	0	ns
	TCHRH		– 9	1	ns
Data valid to RDX ↑ setup time	TDSRH	RDX D31 to D0	29	—	ns
RDX ↑ to Data valid hold time (internal MCLKO → MCLKI / /MCLKI feedback)	TRHDX	RDX D31 to D0	0	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	TCLWRL	MCLKO WRXn	—	6	ns
	TCLWRH		0	—	ns
MCLKO ↓ to CSXn delay time	TCLCSL	MCLKO CSXn	—	6	ns
	TCLCSH		—	7	ns

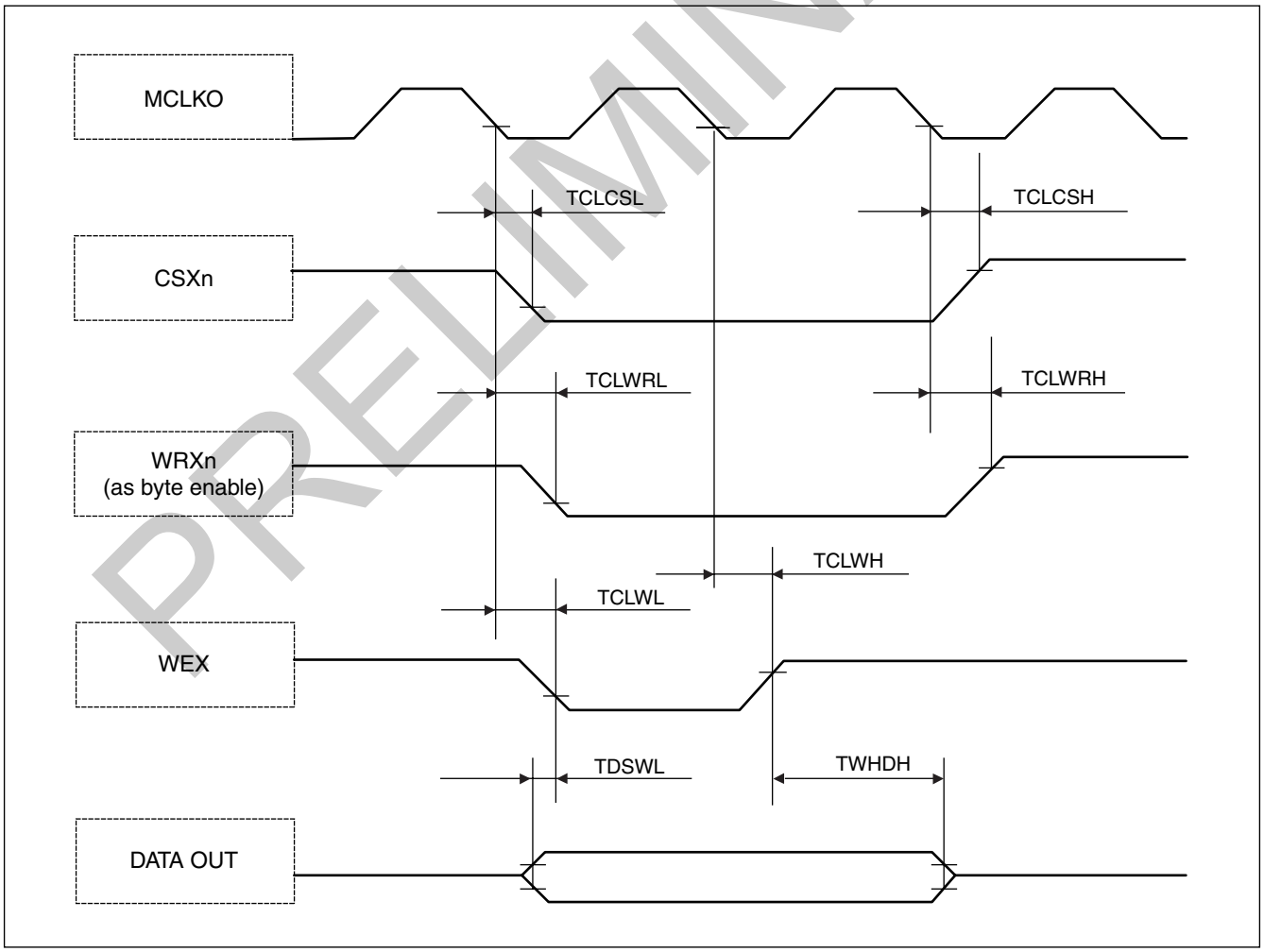


PRELIMINARY

7.8.4. Synchronous write access - byte control type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WEX delay time	TCLWL	MCLKO WEX	—	7	ns
	TCLWH		1	—	ns
Data valid to WEX ↓ setup time	TDSWL	WEX D31 to D0	– 20	—	ns
WEX ↑ to Data valid hold time	TWHDH	WEX D31 to D0	t_{CLKT} – 19	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	TCLWRL	MCLKO WRXn	—	6	ns
	TCLWRH		0	—	ns
MCLKO ↓ to CSXn delay time	TCLCSL	MCLKO CSXn	—	6	ns
	TCLCSH		—	7	ns

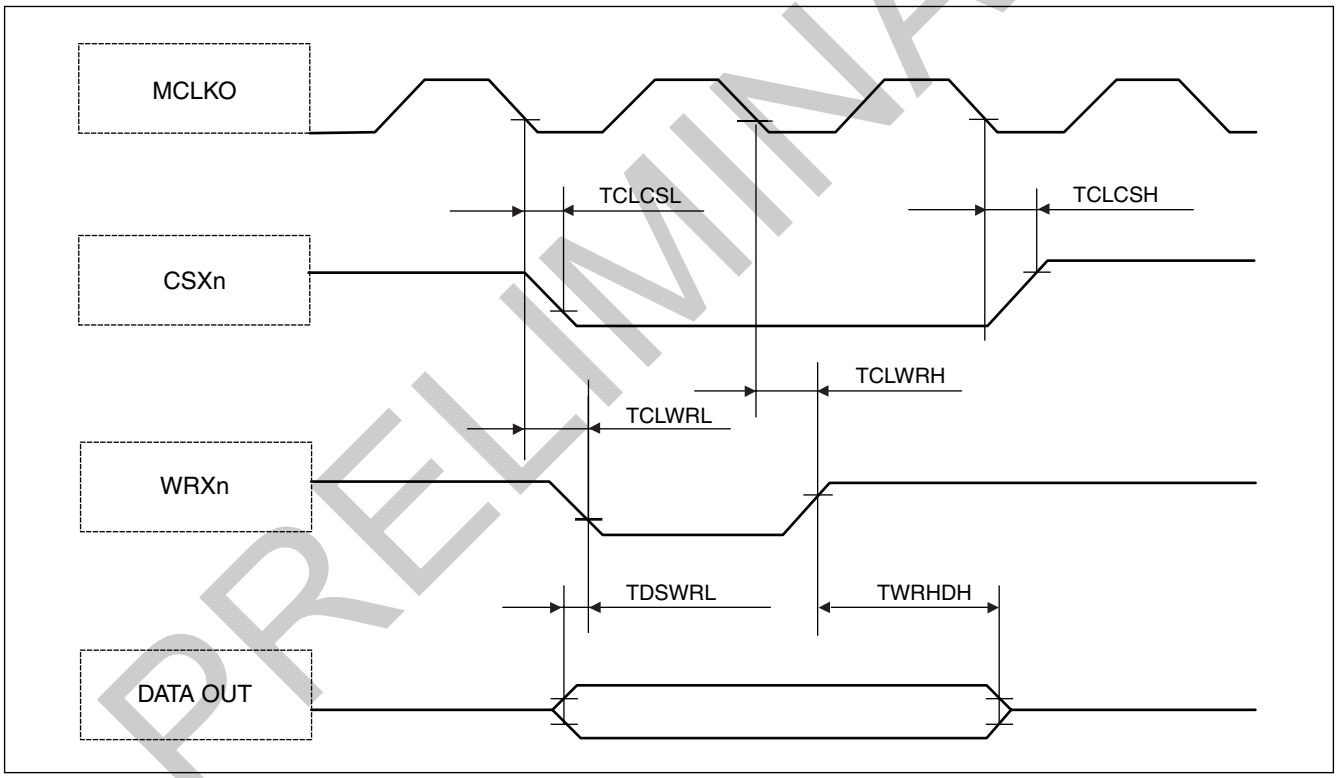


PRELIMINARY

7.8.5. Synchronous write access - no byte control type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WRXn delay time	TCLWRL	MCLKO WRXn	—	6	ns
	TCLWRH		0	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D0	– 20	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D0	t_{CLKT} – 14	—	ns
MCLKO ↓ to CSXn delay time	TCLCSL	MCLKO CSXn	—	6	ns
	TCLCSH		—	7	ns

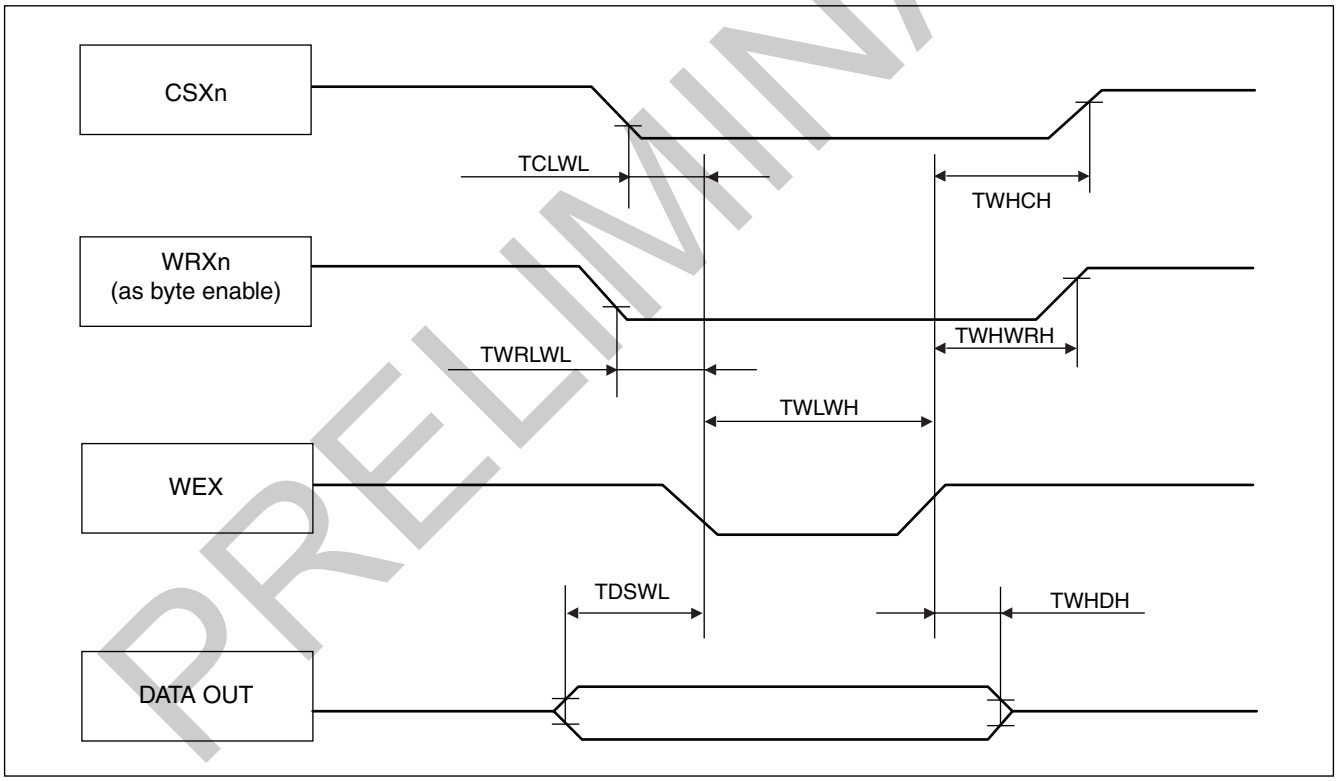


PRELIMINARY

7.8.6. Asynchronous write access - byte control type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	TWLWH	WEX	t_{CLKT} – 2	—	ns
Data valid to WEX ↓ setup time	TDSWL	WEX D31 to D0	1/2 × t_{CLKT} – 20	—	ns
WEX ↑ to Data valid hold time	TWHDH	WEX D31 to D0	1/2 × t_{CLKT} – 20	—	ns
WEX to WRXn delay time	TWRLWL	WEX WRXn	—	1/2 × t_{CLKT} + 3	ns
	TWHWRH		1/2 × t_{CLKT} – 7	—	ns
WEX to CSXn delay time	TCLWL	WEX CSXn	—	1/2 × t_{CLKT} – 1	ns
	TWHCH		1/2 × t_{CLKT} – 4	—	ns

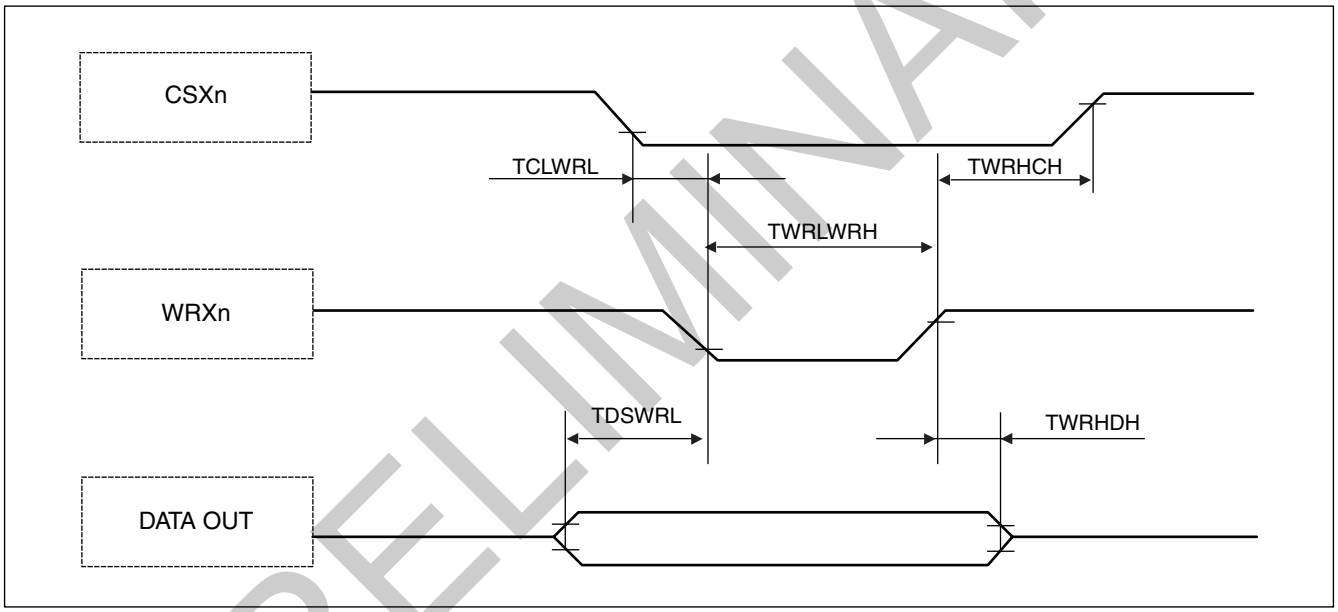


PRELIMINARY

7.8.7. Asynchronous write access - no byte control type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn ↓ to WRXn ↑ pulse width	TWRLWRH	WRXn	t_{CLKT} – 2	—	ns
Data valid to WRXn ↓ setup time	TDSWRL	WRXn D31 to D0	1/2 × t_{CLKT} – 21	—	ns
WRXn ↑ to Data valid hold time	TWRHDH	WRXn D31 to D0	1/2 × t_{CLKT} – 18	—	ns
WRXn to CSXn delay time	TCLWRL	WRXn CSXn	—	1/2 × t_{CLKT} – 1	ns
	TWRHCH		1/2 × t_{CLKT} – 4	—	ns

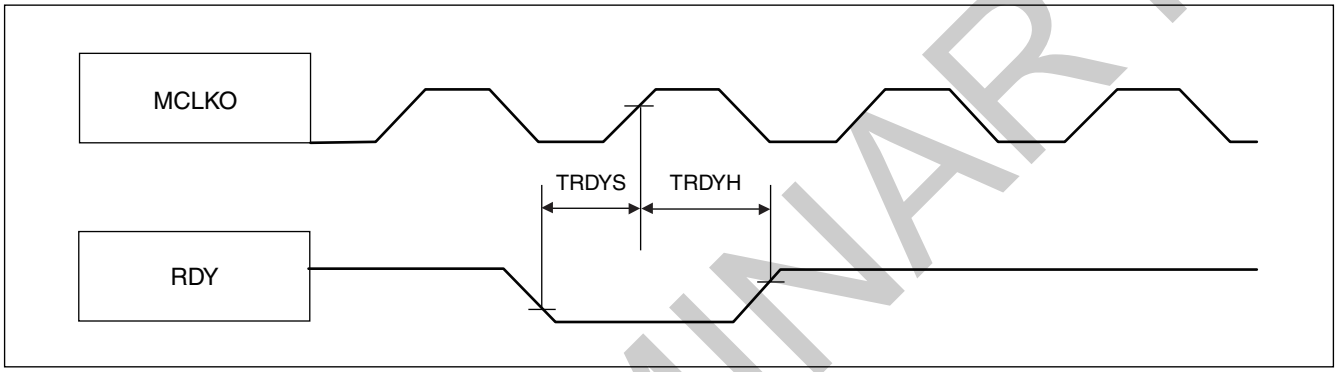


PRELIMINARY

7.8.8. RDY waitcycle insertion

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	TRDYS	MCLKO RDY	37	—	ns
RDY hold time	TRDYH	MCLKO RDY	0	—	ns



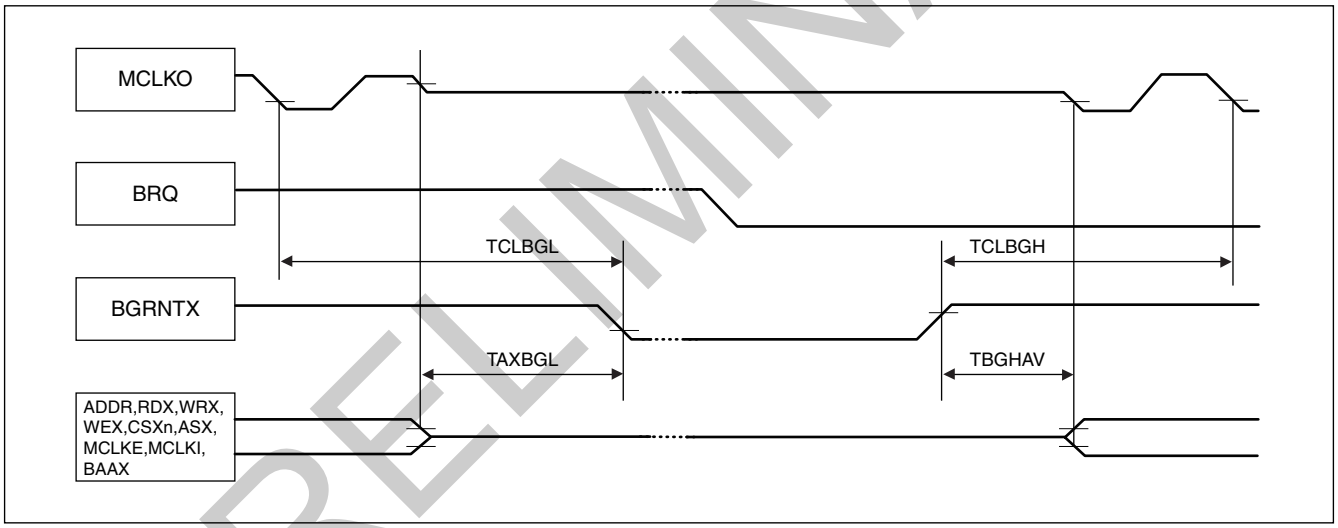
PRELIMINARY

7.8.9. Bus hold timing

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to BGRNTX delay time	TCLBGL	MCLKO BGRNTX	—	$2 \times t_{CLKT} + 16$	ns
	TCLBGH		—	$2 \times t_{CLKT} + 3$	ns
Bus HIZ to BGRNTX ↓	TAXBGL	BGRNTX MCLK* A0 to An RDX, ASX WRXn,WEX CSXn,BAAX	$t_{CLKT} + 1$	—	ns
BGRNTX ↑ to Bus drive	TBGHAV		$t_{CLKT} + 1$	—	ns

Note : BRQ must be kept High until the bus is granted (this is acknowledged by the falling edge of BGRNTX).
It must be kept High as long as the bus shall be hold.
After releasing the bus (BRQ set to Low) this is acknowledged by the rising edge of BGRNTX.

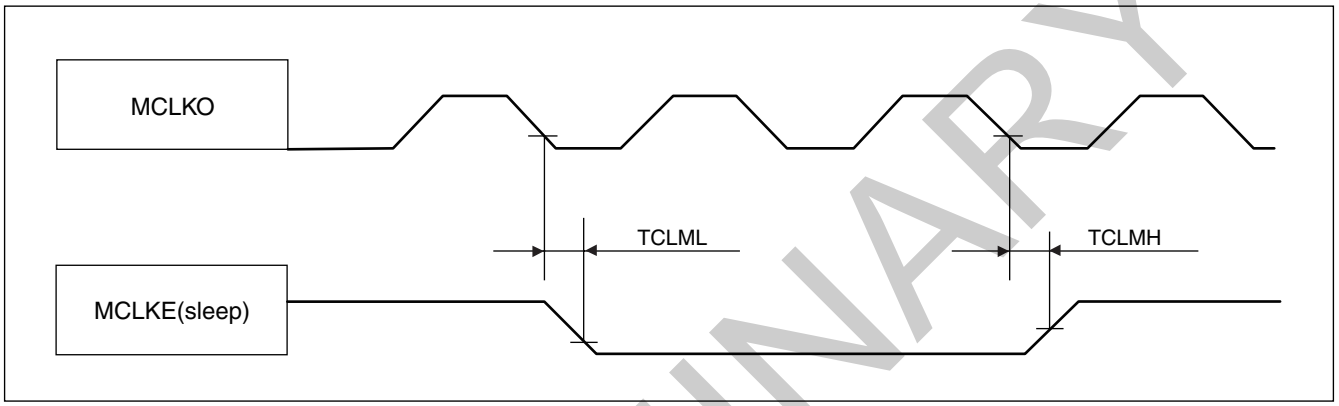


PRELIMINARY

7.8.10. Clock relationships

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to MCLKE (in sleep mode)	TCLML	MCLKO MCLKE	—	3	ns
	TCLMH		0	—	ns



PRELIMINARY

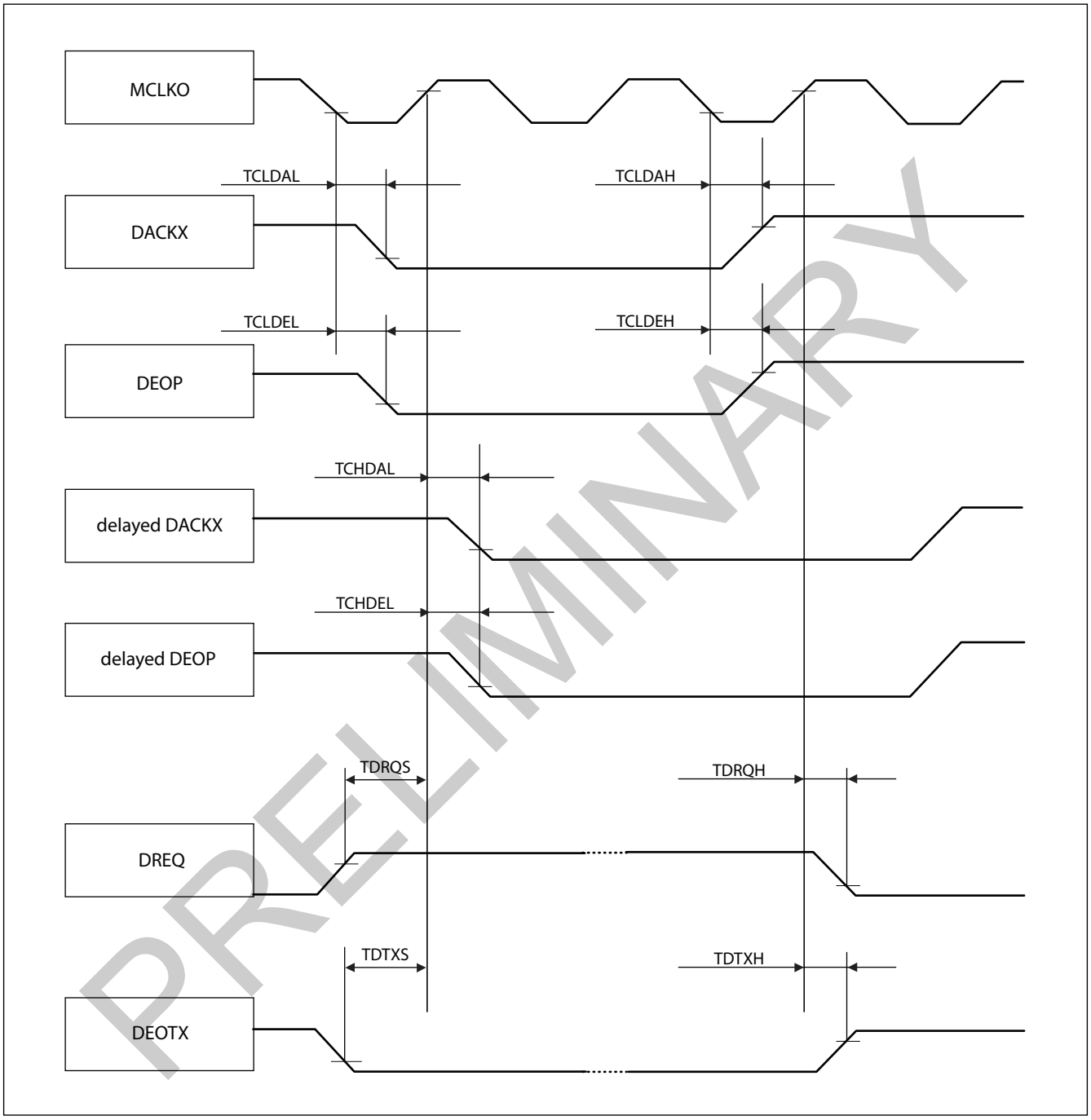
7.8.11. DMA transfer

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to DACKX delay time	TCLDAL	MCLKO DACKXn	—	7	ns
	TCLDAH		—	8	ns
MCLKO ↓ to DEOP delay time	TCLDEL	MCLKO DEOPn	—	7	ns
	TCLDEH		—	11	ns
MCLKO ↑ to DACKX delay time (ADDR → delayed CS)	TCHDAL	MCLKO DACKXn	– 10	2	ns
MCLKO ↑ to DEOP delay time (ADDR → delayed CS)	TCHDEL	MCLKO DEOPn	– 10	1	ns
DREQ setup time	TDRQS	MCLKO DREQn	38	—	ns
DREQ hold time	TDRQH	MCLKO DREQn	0	—	ns
DEOTXn setup time	TDTXS	MCLKO DEOTXn	39	—	ns
DEOTXn hold time	TDTXH	MCLKO DEOTXn	0	—	ns

Note : DREQ and DEOTX must be applied for at least 5 × t_{CLKT} to ensure that they are really sampled and evaluated. Under best case conditions (DMA not busy) only setup and hold times are required.

PRELIMINARY



PRELIMINARY

PRELIMINARY

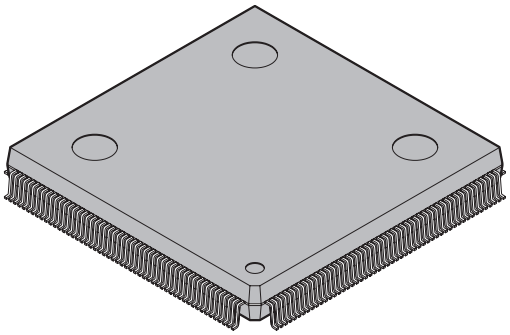
■ ORDERING INFORMATION

Part number	Package	Remarks
MB91F467DBPFVS-GSE2	208-pin plastic QFP (FPT-208P-M04)	Lead-free package

PRELIMINARY

■ PACKAGE DIMENSION

208-pin plastic QFP

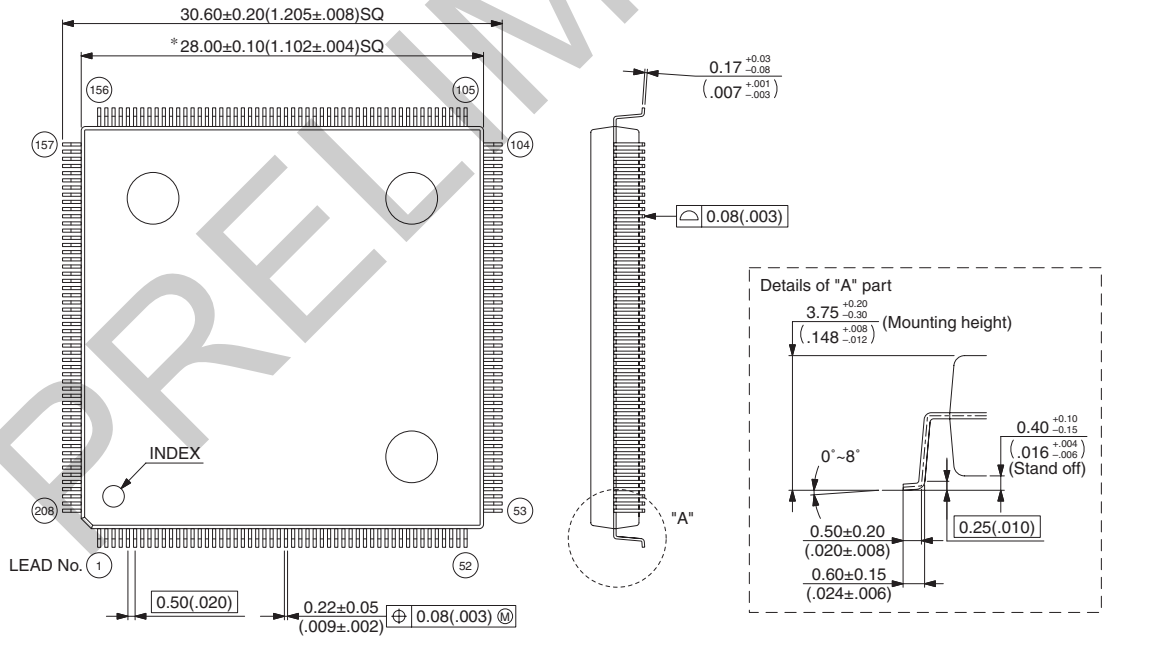


(FPT-208P-M04)

Lead pitch	0.50 mm
Package width × package length	28.0 × 28.0 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	3.95 mm MAX
Weight	5.71g
Remark	Low heat resistance type

208-pin plastic QFP
(FPT-208P-M04)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

PRELIMINARY

■ REVISION HISTORY

Version	Date	Remark
2.0	2007-09-04	Initial version
2.1	2007-10-08	Revision history table added Fixed PDF generation problem before section “AD converter characteristics” Absolute maximum ratings: Smoothing capacitor size at VCC18C changed to “typ 4.7uF” Output voltage 2 is max. V_{DD}35 Recommended operating conditions: Power supply slew rate fixed Exchanged the sequence of device names into “MB91F465DA, MB91F467DA” where they appeare on one line
2.2	2007-10-16	Moved revision history to the end of file Features: Added Clock Monitor Corrected VCC18C pin number in table “Power supply/Ground pins” pg.14 Electrical characteristics: Added section 7.FLASH memory program/erase characteristics
2.3	2007-10-22	DC characterisitcs: Corrected I_{CC}H in STOP + RTC 100kHz mode and I_{LV} (Icc of low volt detection) max. value
2.4	2007-10-25	FLASH memory program/erase characteristics: Typo fixed in note *1 Recommended operating conditions: Corrected text for smoothing capacitor at VCC18C pin Naming inconsistency AVSS / AVSS5 fixed Features: added Up/Down counter Product lineup: fixed number of interrupt channels Handling devices: changed the notes about external clock supply and removed section “Single phase clock supply” Clock timing: removed “Single phase clock supply” from freq. table
2.5	2008-1-11	DC characterisitcs: I_{IL} = +/- 3 uA at 105 deg.C IO CIRCUIT TYPE: Corrected oscillator pin block diagrams ELECTRICAL CHARACTERISTICS: re-arranged section sequence Fixed typos in ALARM comparator spec. Added MB91F467DB (called F467Dx if the text item is for bot revisions) Corrected IO-MAP according to latest proofread on F460G series Various corrections after proofread by FJ
2.6	2008-02-04	Added MEMO and DISCLAIMER
2.7	2008-02-18	AC-Characteristics: Replaced “rising”/”falling” with arrow-up/arrow-down

PRELIMINARY

■ MEMO AND DISCLAIMER

MEMO

PRELIMINARY

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MEMO

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