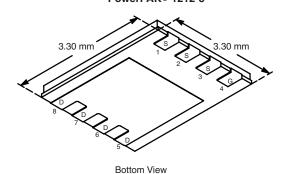




# N-Channel 25-V (D-S) MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>a</sup>	Q <sub>g</sub> (Typ.)	
25	0.0051 at V <sub>GS</sub> = 10 V	35	13 nC	
	0.0069 at V <sub>GS</sub> = 4.5 V	35	13110	

### PowerPAK® 1212-8



Ordering Information: SiS430DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

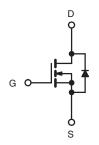
## **FEATURES**

- Halogen-free
- TrenchFET<sup>®</sup> Power MOSFET
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested

# RoHS COMPLIANT

### **APPLICATIONS**

- DC/DC Converter
  - POL
  - Server



N-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage	$V_{DS}$	25			
Gate-Source Voltage		V <sub>GS</sub>	± 20		
Continuous Drain Current (T <sub>J</sub> = 150 °C)	$T_C = 25 ^{\circ}C$ $T_C = 70 ^{\circ}C$		35 <sup>a</sup> 35 <sup>a</sup>		
	$T_A = 25 ^{\circ}\text{C}$ $T_A = 70 ^{\circ}\text{C}$	= 25 °C	21.5 <sup>b, c</sup>	Α	
Pulsed Drain Current		I <sub>DM</sub>	60		
Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	30		
Avalanche Energy	L = 0.1 IIII1	E <sub>AS</sub>	45	mJ	
Continuous Source-Drain Diode Current $T_C = 25 ^{\circ}\text{C}$ $T_A = 25 ^{\circ}\text{C}$		I <sub>S</sub>	35 <sup>a</sup> 3.2 <sup>b, c</sup>	Α	
Maximum Power Discipation	T <sub>C</sub> = 25 °C T <sub>C</sub> = 70 °C		52 33	w	
Maximum Power Dissipation	T <sub>A</sub> = 25 °C T <sub>A</sub> = 70 °C	P <sub>D</sub>	3.8 <sup>b, c</sup> 2 <sup>b, c</sup>		
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150	°C	
Soldering Recommendations (Peak Tempera		260			

THERMAL RESISTANCE RATINGS						
Parameter		Symbol Typical		Maximum	Unit	
Maximum Junction-to-Ambient <sup>b, f</sup>	t ≤ 10 s	$R_{thJA}$	24	33	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	$R_{thJC}$	1.9	2.4	]	

#### Notes:

- a. Package Limited.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK 1212 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under Steady State conditions is 81 °C/W.

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SPECIFICATIONS T <sub>J</sub> = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	1			ı	ı	ı	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	25			V	
V <sub>DS</sub> Temperature Coefficient	$\Delta V_{DS}/T_{J}$	I <sub>D</sub> = 250 μA		25		mV/°C	
V <sub>GS(th)</sub> Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	,		- 5.5			
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	1.2		2.5	V	
Gate-Source Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V			1	μΑ	
		$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			5		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	20			Α	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.0042	0.0051	Ω	
Diam-Cource On-Clate Resistance	1 1DS(on)	$V_{GS} = 4.5 \text{ V}, I_D = 18.5 \text{ A}$		0.0056	0.0069		
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	$V_{DS} = 15 \text{ V}, I_{D} = 20 \text{ A}$		61		S	
Dynamic <sup>b</sup>							
Input Capacitance	C <sub>iss</sub>			1600		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>DS</sub> = 12.5 V, V <sub>GS</sub> = 0 V, f = 1 MHz		410			
Reverse Transfer Capacitance	C <sub>rss</sub>			155			
Total Gate Charge	$Q_g$	V <sub>DS</sub> = 12.5 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		26.5	40	nC	
Total Gate Grange				13	19.5		
Gate-Source Charge	$Q_{gs}$	$V_{DS} = 12.5 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 20 \text{ A}$		4.6			
Gate-Drain Charge	Q <sub>gd</sub>			4.1			
Gate Resistance	$R_g$	f = 1 MHz		1.5	3	Ω	
Turn-On Delay Time	t <sub>d(on)</sub>			20	30		
Rise Time	t <sub>r</sub>	$V_{DD} = 12.5 \text{ V}, R_{L} = 1.25 \Omega$		12	20	-	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$		25	40		
Fall Time	t <sub>f</sub>			10	15		
Turn-On Delay Time	t <sub>d(on)</sub>			10	15	ns	
Rise Time	t <sub>r</sub>	$V_{DD} = 12.5 \text{ V}, R_L = 1.25 \Omega$		10	15	- - -	
Turn-Off Delay Time	t <sub>d(off)</sub>	$I_D \cong 10 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		20	30		
Fall Time	t <sub>f</sub>			10	15		
<b>Drain-Source Body Diode Characteristi</b>	cs				L		
Continuous Source-Drain Diode Current	I <sub>S</sub>	T <sub>C</sub> = 25 °C			35		
Pulse Diode Forward Current	I <sub>SM</sub>				60	A	
Body Diode Voltage	V <sub>SD</sub>	I <sub>S</sub> = 10 A, V <sub>GS</sub> = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t <sub>rr</sub>			35	55	ns	
Body Diode Reverse Recovery Charge	Q <sub>rr</sub>	I <sub>F</sub> = 10 A, dl/dt = 100 A/μs, T <sub>J</sub> = 25 °C		35	55	nC	
Reverse Recovery Fall Time	t <sub>a</sub>			17		1	
Reverse Recovery Rise Time	t <sub>b</sub>			18		ns	

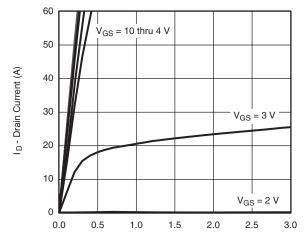
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$ 

b. Guaranteed by design, not subject to production testing.

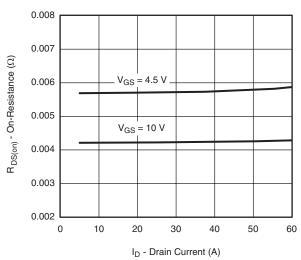


## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

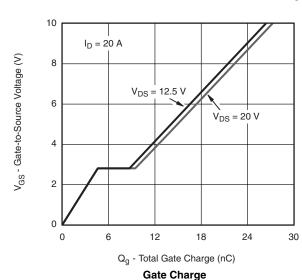


 $V_{DS}$  - Drain-to-Source Voltage (V)

### **Output Characteristics**



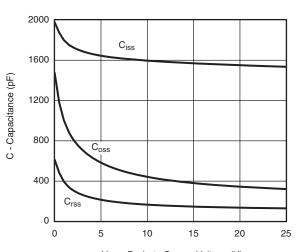
On-Resistance vs. Drain Current and Gate Voltage



 $T_{C} = 25 \, ^{\circ}C$ 16  $T_{C} = 25 \, ^{\circ}C$   $T_{C} = -55 \, ^{\circ}C$ 0.0 0.5 1.0 1.5 2.0 2.5 3.0

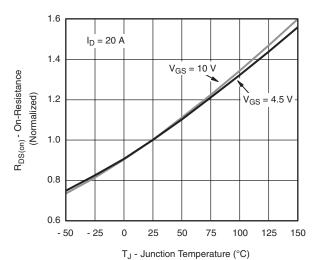
V<sub>GS</sub> - Gate-to-Source Voltage (V)

Transfer Characteristics



 $V_{\mathsf{DS}}$  - Drain-to-Source Voltage (V)

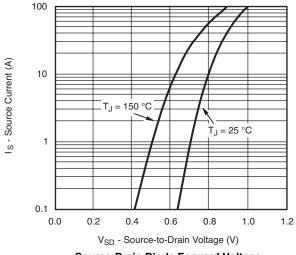


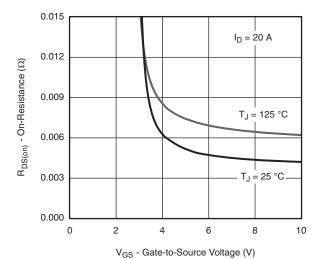


On-Resistance vs. Junction Temperature

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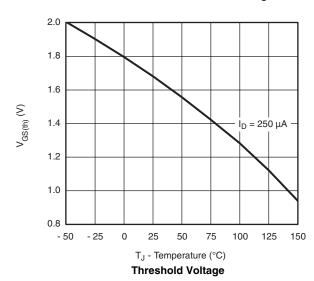
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

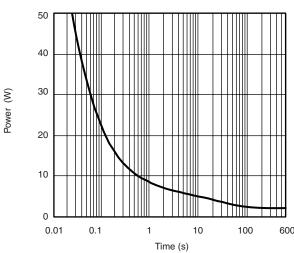




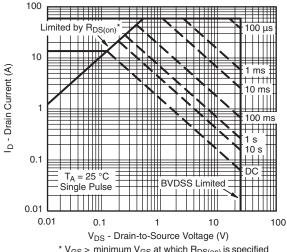
#### Source-Drain Diode Forward Voltage







Single Pulse Power (Junction-to-Ambient)



 $^{\star}$   $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified

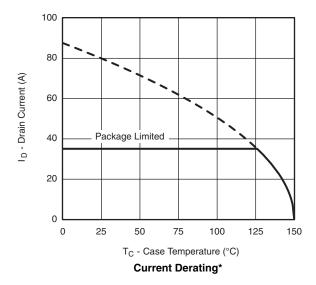
Safe Operating Area, Junction-to-Ambient

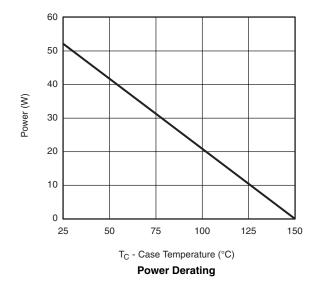






# TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





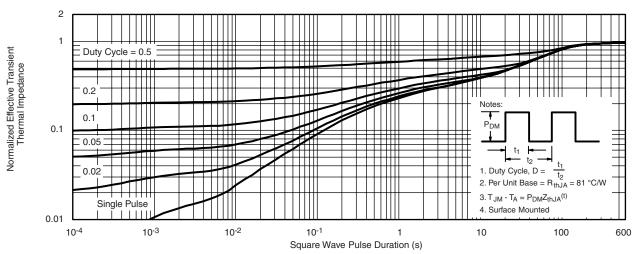
Document Number: 69025 S-82655-Rev. A, 03-Nov-08

<sup>\*</sup> The power dissipation  $P_D$  is based on  $T_{J(max)} = 150$  °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

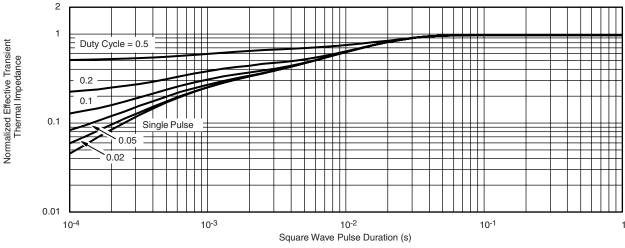
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## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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