

Integrated Device Technology, Inc.

HIGH-SPEED BiCMOS 10-BIT REGISTER

ADVANCE INFORMATION
IDT54/74FBT821A
IDT54/74FBT821B
IDT54/74FBT821C

FEATURES:

- IDT54/74FBT821A equivalent to the 54/74BCT821
- IDT54/74FBT821B 25% faster than the 821A
- IDT54/74FBT821C 10% faster than the 821B
- Significant reduction in ground bounce from standard CMOS devices
- TTL compatible input and output levels
- Low power in all three states
- $\pm 10\%$ power supply for both military and commercial grades
- JEDEC standard pinout for DIP, SOIC and LCC packages
- Military product compliant to MIL-STD-883, Class B

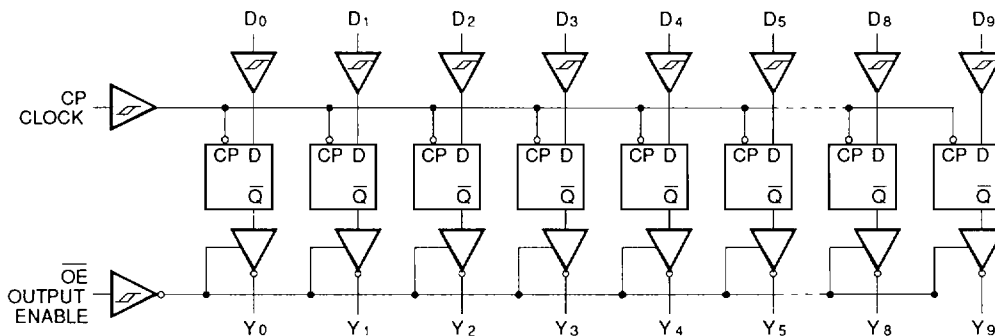
DESCRIPTION:

The FBT series of BiCMOS registers are built using advanced BiCEMOS™, a dual metal BiCMOS technology. This technology is designed to supply the highest device speeds while maintaining CMOS power levels.

The IDT54/74FBT821A is a buffered, 10-bit wide version of the '374/'574 function.

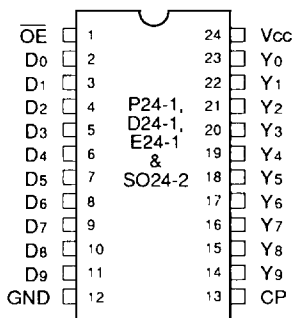
The FBT series of buffers are ideal for use in designs needing to drive large capacitive loads with low static (DC) current loading. All data inputs have a 200mV typical input hysteresis for improved noise rejection.

FUNCTIONAL BLOCK DIAGRAM

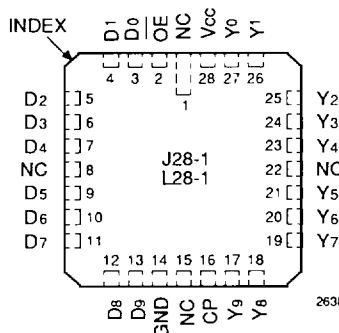


2638 drw 01

PIN CONFIGURATIONS



DIP/SOIC/CERPACK
TOP VIEW



LCC/PLCC
TOP VIEW

2638 drw 02

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MILITARY AND COMMERCIAL TEMPERATURE RANGES

JUNE 1990

PIN DESCRIPTION

Pin Names	I/O	Description
D ₀ -D ₉	I	The D flip-flop data inputs.
\overline{OE}	I	Three-state Output Enable input (Active LOW).
CP	I	Clock Pulse for the register; enters data into the register on the LOW-to-HIGH transition.
Y ₀ -Y ₉	O	The register three-state outputs.

2638 tbl 01

FUNCTION TABLE⁽¹⁾

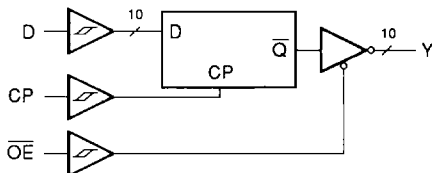
Inputs			Output	Function
OE	D _i	CP	Y _i	
H	L	↑	Z	Load Data
H	H	↑	Z	
L	L	↑	L	
L	H	↑	H	

2638 tbl 02

NOTE:

- 1 H = HIGH
- L = LOW
- X = Don't Care
- ↑ = LOW-to-HIGH Transition
- Z = High Impedance

LOGIC SYMBOL



2638 d/w 03

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Rating	Commercial	Military	Unit
V _{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T _A	Operating Temperature	0 to +70	-55 to +125	°C
T _{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T _{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P _T	Power Dissipation	0.5	0.5	W
I _{OUT}	DC Output Current	120	120	mA

NOTE:

2638 tbl 03

- 1 Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	pF

NOTE:

2638 tbl 04

- 1 This parameter is measured at characterization but not tested.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: TA = 0°C to +70°C, VCC = 5.0V ± 10%; Military: TA = -55°C to +125°C, VCC = 5.0V ± 10%

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Unit	
V _{IH}	Input HIGH Level	Guaranteed Logic HIGH Level	2.0	—	—	V	
V _{IL}	Input LOW Level	Guaranteed Logic LOW Level	—	—	0.8	V	
I _{IH}	Input HIGH Current	V _{CC} = Max., V _I = 2.7V	—	—	10	μA	
I _{IL}	Input LOW Current	V _{CC} = Max., V _I = 0.5V	—	—	-10	μA	
I _{OZH}	High Impedance	V _{CC} = Max. V _O = 2.7V	—	—	50	μA	
I _{OZL}	Output Current		V _O = 0.5V	—	—		-50
I _I	Input HIGH Current	V _{CC} = Max., V _I = 5.5V	—	—	100	μA	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _N = -18mA	—	-0.7	-1.2	V	
I _{OS}	Short Circuit Current	V _{CC} = Max., V _O = GND ⁽³⁾	-75	—	-225	mA	
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -12mA MIL.	2.4	3.3	—	V
			I _{OH} = -15mA COM'L.	—	—	—	—
	I _{OH} = -18mA MIL.		2.0	3.0	—	V	
	I _{OH} = -24mA COM'L.		—	—	—	—	—
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 32mA MIL.	—	0.3	0.5	V
			I _{OL} = 48mA COM'L.	—	—	—	—
V _H	Input Hysteresis		V _{CC} = 5V	—	200	—	mV
I _{OFF}	Bus Leakage Current		V _{CC} = 0V, V _O = 4.5V	—	—	100	μA
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} = GND or V _{CC}	—	0.2	1.5	mA	

NOTES:

2638 tbl 05

- 1 For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- 2 Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
- 3 Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current (Inputs TTL HIGH)	VCC = Max. VIN = 3.4V ⁽³⁾		—	—	2.0	mA/
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	VCC = Max., Outputs Open OE = GND One Input Toggling 50% Duty Cycle	VIN = VCC VIN = GND	—	—	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	VCC = Max., Outputs Open f _i = 10MHz, 50% Duty Cycle OE = GND One Bit Toggling	VIN = VCC VIN = GND	—	—	4.0	mA
			VIN = 3.4V VIN = GND	—	—	5.0	
		VCC = Max., Outputs Open f _i = 2.5MHz, 50% Duty Cycle OE = GND	VIN = VCC VIN = GND	—	—	7.8 ⁽⁵⁾	
			VIN = 3.4V VIN = GND	—	—	17.8 ⁽⁵⁾	

NOTES:

2638 tbl 06

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at VCC = 5.0V, +25°C ambient, and maximum loading
- Per TTL driven input (VIN = 3.4V); all other inputs at VCC or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the ICC formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} \cdot D_H \cdot N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (VIN = 3.4V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 f_i = input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition ⁽¹⁾	IDT54/74FBT821A				IDT54/74FBT821B				IDT54/74FBT821C				Unit
			Com'l.		Mil.		Com'l.		Mil.		Com'l.		Mil.		
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
tPLH tPHL	Propagation Delay Clock to Y _i (\overline{OE} = LOW)	CL = 50pF RL = 500Ω	—	10.0	—	—	—	7.5	—	—	—	6.0	—	—	ns
tPZ tPZL	Output EnableTime \overline{OE} to Y _i		—	12.0	—	—	—	8.0	—	—	—	7.0	—	—	ns
tPHZ tPLZ	Output Disable Time \overline{OE} to Y _i		—	8.0	—	—	—	7.5	—	—	—	6.5	—	—	ns
tsU	Data to CP		—	7.0	—	—	—	3.0	—	—	—	3.0	—	—	ns
tH	Data to CP		—	1.0	—	—	—	1.0	—	—	—	1.0	—	—	ns
tW	Clock Pulse Width		—	7.0	—	—	—	5.0	—	—	—	5.0	—	—	ns

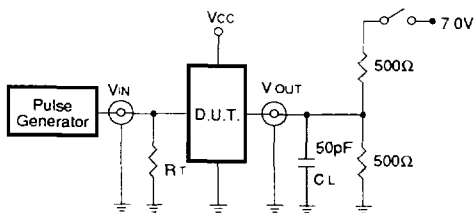
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays

2638 (b) 07

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



SWITCH POSITION

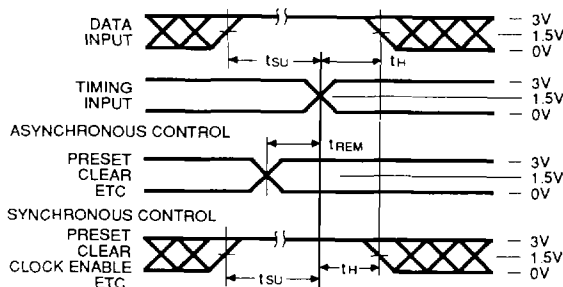
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Outputs	Open

DEFINITIONS:

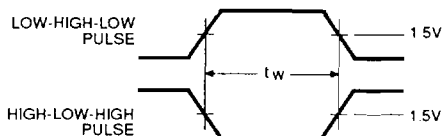
C_L = Load capacitance; includes jig and probe capacitance.
 R_T = Termination resistance; should be equal to Z_{OUT} of the Pulse Generator.

2638 ml.08

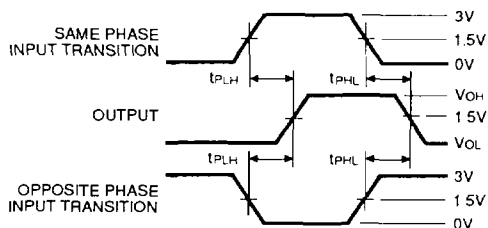
SET-UP, HOLD AND RELEASE TIMES



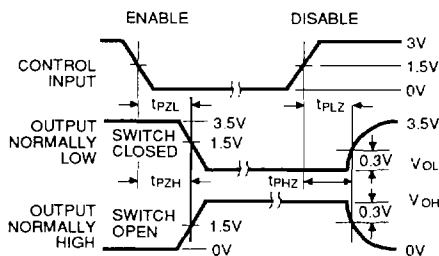
PULSE WIDTH



PROPAGATION DELAY



ENABLE AND DISABLE TIMES

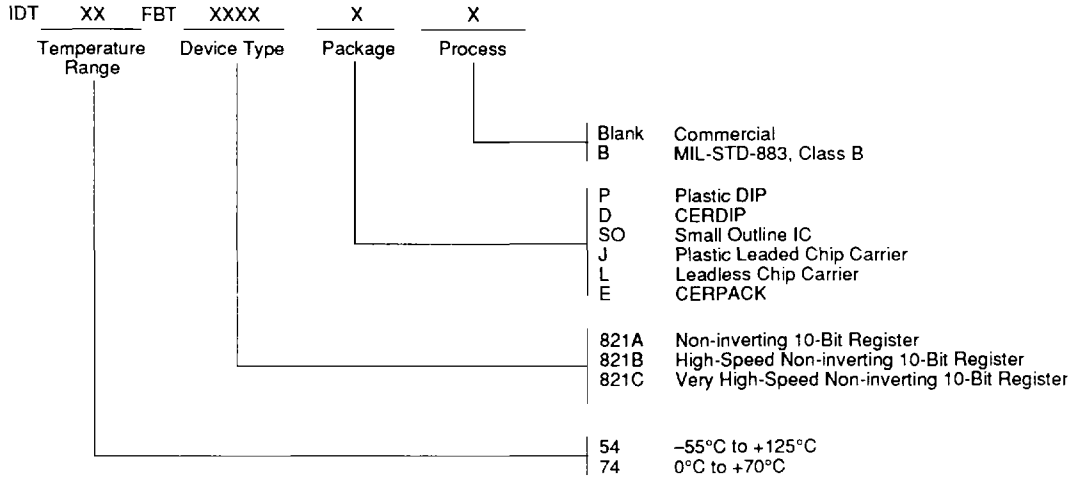


NOTES

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses. Rate \leq 1.0 MHz, $Z_o \leq$ 50Ω, $t_F \leq$ 2.5ns; $t_R \leq$ 2.5ns.

2638 drw.04

ORDERING INFORMATION



263B drw 04