

8-INPUT MULTIPLEXER; 3-STATE

FEATURES

- True and complement outputs
- Both outputs are 3-state for further multiplexer expansion
- Multifunction capability
- Permits multiplexing from n-lines to one line
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT251 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT251 are the logic implementations of single-pole 8-position switches with the state of three select inputs (S_0, S_1, S_2) controlling the switch positions.

Assertion (Y) and negation (\bar{Y}) outputs are both provided.

The output enable input (\bar{OE}) is active LOW. The logic function provided at the output, when activated, is:

$$Y = \bar{OE} \cdot (I_0 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + I_1 \cdot S_0 \cdot \bar{S}_1 \cdot \bar{S}_2 + \\ + I_2 \cdot \bar{S}_0 \cdot S_1 \cdot \bar{S}_2 + I_3 \cdot S_0 \cdot S_1 \cdot \bar{S}_2 + \\ + I_4 \cdot \bar{S}_0 \cdot \bar{S}_1 \cdot S_2 + I_5 \cdot S_0 \cdot \bar{S}_1 \cdot S_2 + \\ + I_6 \cdot \bar{S}_0 \cdot S_1 \cdot S_2 + I_7 \cdot S_0 \cdot S_1 \cdot S_2)$$

Both outputs are in the high impedance OFF-state (Z) when the output enable input is HIGH, allowing multiplexer expansion by tying the outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay I_h to Y I_h to \bar{Y} S_n to Y S_n to \bar{Y}	$C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$	15 17 20 21	19 19 20 21	ns ns ns ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	44	46	pF

$GND = 0 \text{ V}$; $T_{amb} = 25^\circ \text{C}$; $t_r = t_f = 6 \text{ ns}$

Notes

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF

f_o = output frequency in MHz V_{CC} = supply voltage in V

$$\Sigma (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$$

- For HC, the condition is $V_I = GND$ to V_{CC}

For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

PACKAGE OUTLINES

SEE PACKAGE INFORMATION SECTION

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 3, 2, 1, 15, 14, 13, 12	I_0 to I_7	multiplexer inputs
5	Y	multiplexer output
6	\bar{Y}	complementary multiplexer output
7	\bar{OE}	3-state output enable input (active LOW)
8	GND	ground (0 V)
11, 10, 9	S_0, S_1, S_2	select inputs
16	V_{CC}	positive supply voltage

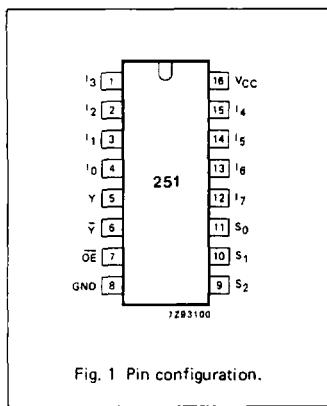


Fig. 1 Pin configuration.

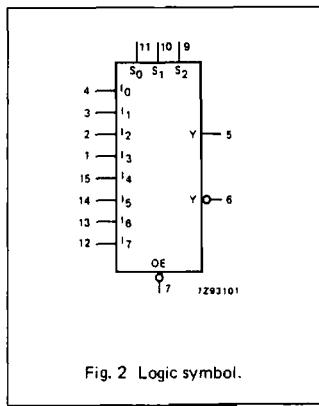


Fig. 2 Logic symbol.

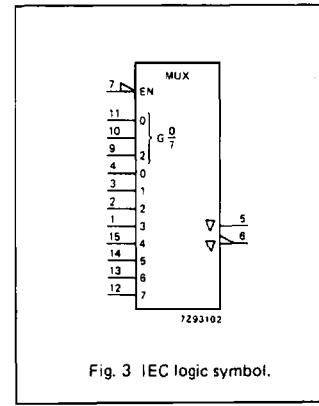


Fig. 3 IEC logic symbol.

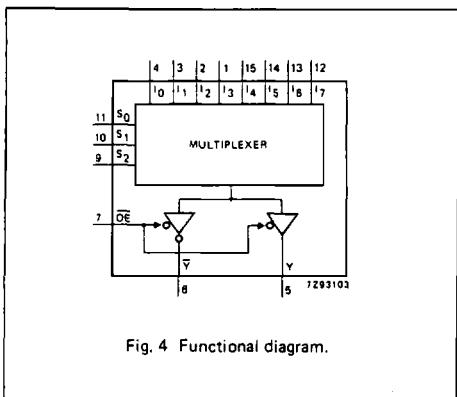


Fig. 4 Functional diagram.

FUNCTION TABLE

INPUTS													OUTPUTS	
OE	S ₂	S ₁	S ₀	I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	Ȳ	Y	
H	X	X	X	X	X	X	X	X	X	X	X	Z	Z	
L	L	L	L	L	H	X	X	X	X	X	X	H	L	
L	L	L	L	H	X	L	X	X	X	X	X	L	H	
L	L	L	L	H	X	H	X	X	X	X	X	L	H	
L	L	L	H	L	X	X	L	X	X	X	X	H	L	
L	L	L	H	L	X	X	H	X	X	X	X	L	H	
L	L	L	H	H	X	X	X	H	X	X	X	L	H	
L	H	L	L	X	X	X	X	L	X	X	X	H	L	
L	H	L	L	X	X	X	X	H	X	X	X	L	H	
L	H	H	L	X	X	X	X	X	X	X	X	H	L	
L	H	H	H	X	X	X	X	X	X	X	X	L	H	
L	H	H	H	X	X	X	X	X	X	X	X	H	L	

H = HIGH voltage level

L = LOW voltage level

X = don't care

Z = high impedance OFF-state

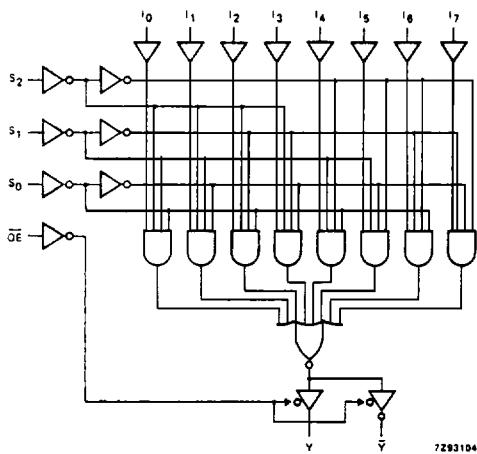


Fig. 5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HC							V _{CC} V	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay I _n to Y	50 18 14	170 34 29		215 43 37		255 51 43		ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay I _n to \bar{Y}	55 20 16	175 35 30		220 44 37		265 53 45		ns	2.0 4.5 6.0	Fig. 7	
t _{PHL} / t _{PLH}	propagation delay S _n to Y	66 24 19	205 41 35		255 51 43		310 62 53		ns	2.0 4.5 6.0	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay S _n to \bar{Y}	69 25 20	205 41 35		255 51 43		310 62 53		ns	2.0 4.5 6.0	Fig. 7	
t _{PZH} / t _{PZL}	3-state output enable time \bar{OE} to Y, \bar{Y}	36 13 10	140 28 24		175 35 30		210 42 36		ns	2.0 4.5 6.0	Fig. 8	
t _{PHZ} / t _{PLZ}	3-state output disable time \bar{OE} to Y, \bar{Y}	39 14 11	140 28 24		170 35 30		210 42 36		ns	2.0 4.5 6.0	Fig. 8	
t _{THL} / t _{TLH}	output transition time	19 7 6	75 15 13		95 19 16		110 22 19		ns	2.0 4.5 6.0	Figs 6 and 7	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard

I_{CC} category: MSI**Note to HCT types**

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
 To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
I _n	1.00
S ₀	1.50
S ₁ , S ₂	1.50
OE	1.50

AC CHARACTERISTICS FOR 74HCTGND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HCT							V _{CC} V	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay I _n to Y		22	35		44		53	ns	4.5	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay I _n to \bar{Y}		22	35		44		53	ns	4.5	Fig. 7	
t _{PHL} / t _{PLH}	propagation delay S _n to Y		24	44		55		66	ns	4.5	Fig. 6	
t _{PHL} / t _{PLH}	propagation delay S _n to \bar{Y}		25	44		55		66	ns	4.5	Fig. 7	
t _{PZH} / t _{PZL}	3-state output enable time OE to Y, \bar{Y}		13	28		35		42	ns	4.5	Fig. 8	
t _{PHZ} / t _{PLZ}	3-state output disable time OE to Y, \bar{Y}		14	28		35		42	ns	4.5	Fig. 8	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Figs 6 and 7	

AC WAVEFORMS

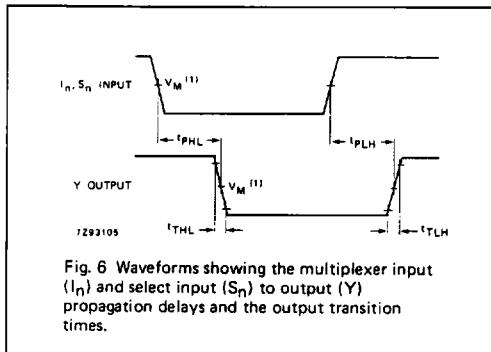


Fig. 6 Waveforms showing the multiplexer input (I_n) and select input (S_n) to output (Y) propagation delays and the output transition times.

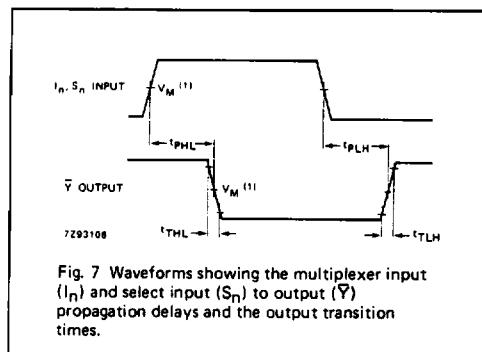


Fig. 7 Waveforms showing the multiplexer input (I_n) and select input (S_n) to output (\bar{Y}) propagation delays and the output transition times.

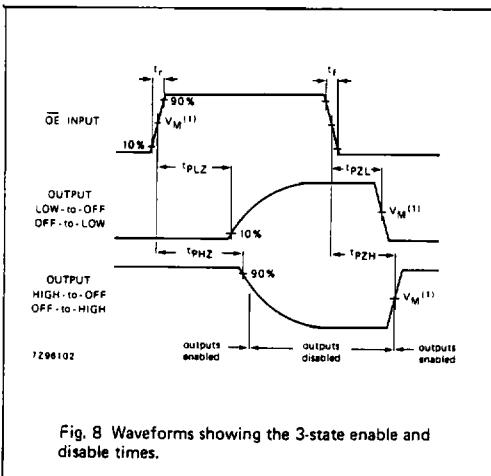


Fig. 8 Waveforms showing the 3-state enable and disable times.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
- HCT: $V_M = 1.3\text{ V}$; $V_I = \text{GND to } 3\text{ V}$.