



## Description

The MK3732-15 is a low cost, low phase noise, high performance VCXO and PLL clock synthesizer designed to replace expensive discrete VCXOs and oscillators. The on-chip Voltage Controlled Crystal Oscillator (VCXO) accepts a 0 to 3.3 V input voltage to cause the output clocks to vary by  $\pm 100$  ppm. Using ICS's patented VCXO and analog Phase-Locked Loop (PLL) techniques, the device uses an inexpensive 10 MHz to 18 MHz pullable crystal input to produce one or two output clocks. To achieve lowest phase noise, the REFCLK can be turned off.

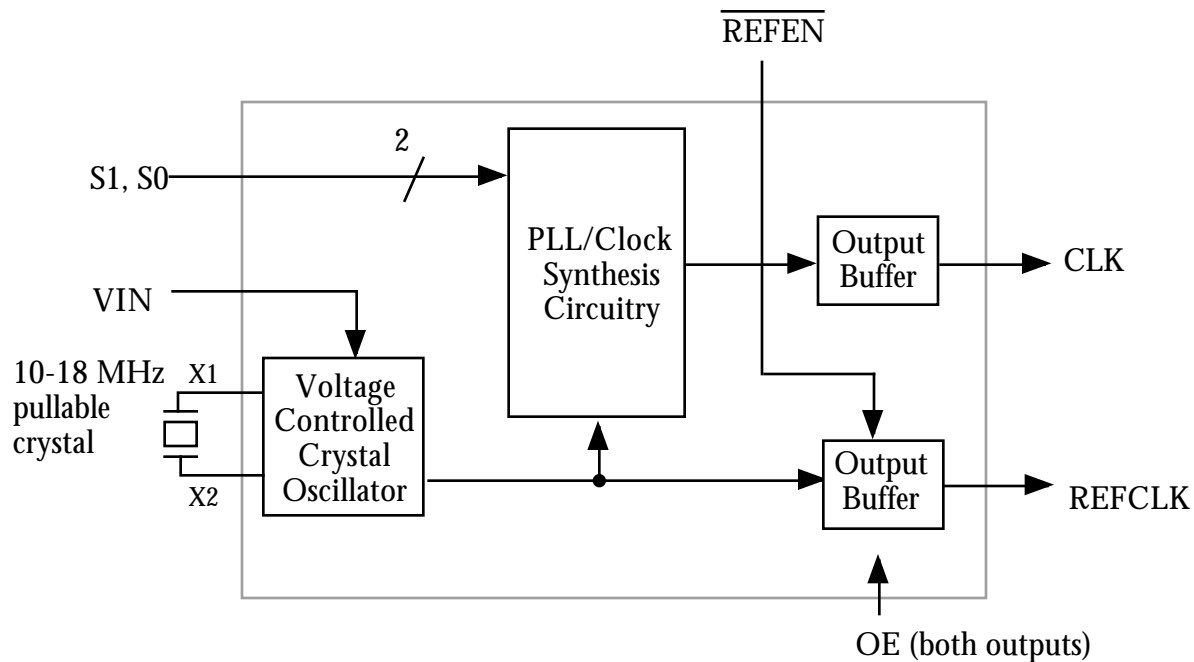
ICS manufactures the largest variety of clocks for set-top boxes and Communications. Consult ICS to eliminate VCXOs, crystals, oscillators and buffers from your board.

## Features



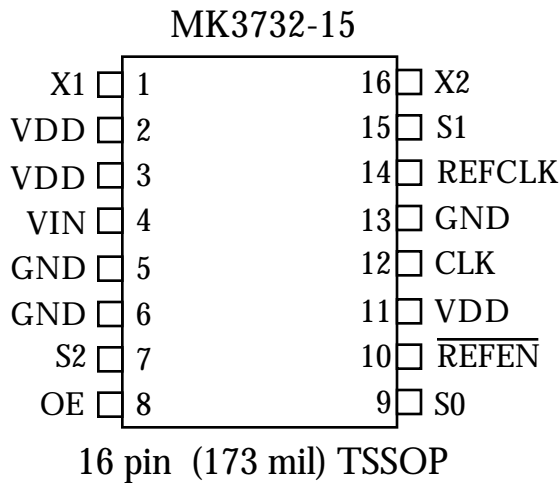
- Packaged in 16 pin TSSOP
- Ideal for ADI's ADSL chipsets
- For MPEG 2 decoders
- Can replace a VCXO and crystal/oscillator
- Uses an inexpensive pullable crystal
- On-chip patented VCXO with pull range of 200 ppm ( $\pm 100$  ppm) minimum
- VCXO tuning voltage of 0 to 3.3 V
- Zero ppm synthesis error in all clocks
- Full CMOS output swings with 12 mA output drive capability at TTL levels
- Advanced, low power, sub-micron CMOS process
- 3.3V only operating voltage

## Block Diagram





## Pin Assignment



## Clock Select Table

S2	S1	S0	CLK
0	0	0	REF/2
0	0	M	x0.666
0	0	1	x2.6666
0	1	0	x4
0	1	M	x1.5
0	1	1	x1.3333
1	0	0	Test
1	0	M	x4
1	0	1	x2
1	1	0	x3
1	1	M	x5
1	1	1	x6

For Analog Devices' ADSL chipset, use a 17.664 MHz crystal, and the 101 setting for a 35.328 MHz output clock. Pin 10 should be grounded to get the 17.664 MHz clock output on pin 14.

0 = connect directly to GND, M = leave unconnected (floating), 1 = connect directly to VDD.

## Pin Descriptions

Number	Name	Type	Description
1	X1	XI	Crystal connection. Connect to a pullable crystal of 10-18 MHz.
2, 3, 11	VDD	P	VDD. Connect to +3.3V.
4	VIN	VI	Voltage Input to VCXO. Zero to 3.3 V signal which controls the frequency of the VCXO.
5, 6, 13	GND	P	Connect to ground.
7	S2	I	Select input #2. Selects CLK output per table above.
8	OE	I	Output Enable. Tri-states outputs when low.
9	S0	TI	Select input #0. Selects CLK output per table above.
10	<u>REFEN</u>	I	Reference Enable (active low). When pin is connected to ground, the REFCLK is running.
12	CLK	O	VCXO Clock Output per table above.
14	REFCLK	O	Buffered crystal VCXO clock
15	S1	I	Select input #1. Selects CLK output per table above.
16	X2	XO	Crystal connection. Connect to a pullable crystal of 10-18 MHz.

Key: I = Input with internal pull-up resistor; TI = tri-level input; O = output; P = power supply connection; VI = analog voltage input; XI, XO = crystal pins.

## External Components

The MK3732-15 requires a minimum number of external components for proper operation. Decoupling capacitors of 0.01µF should be connected between VDD and GND on pins 3 and 5, and VDD and GND on pins 11 and 13, as close to the MK3732-15 as possible. A series termination resistor of 33 Ω may be used for each clock output. The input crystal must be connected as close to the chip as possible. The input crystal should be a fundamental mode, parallel resonant, pullable, AT cut. A crystal with 14 pF load capacitance is recommended. Consult ICS/MicroClock for recommended suppliers. **IMPORTANT** - consult the application note MAN05 for layout guidelines.



## Electrical Specifications

Parameter	Conditions	Minimum	Typical	Maximum	Units
<b>ABSOLUTE MAXIMUM RATINGS (note 1)</b>					
Supply voltage, VDD	Referenced to GND			7	V
Inputs and Clock Outputs	Referenced to GND	-0.5		VDD+0.5	V
Ambient Operating Temperature		0		70	°C
Soldering Temperature	Max of 10 seconds			260	°C
Storage temperature		-65		150	°C
<b>DC CHARACTERISTICS (VDD = 3.3V unless noted)</b>					
Core Operating Voltage, VDD		3.15	3.30	3.45	V
Input High Voltage, VIH, X1 pin only		3.5	2.5		V
Input Low Voltage, VIL, X1 pin only			2.5	1.5	V
Input High Voltage, VIH, binary input	OE	2			V
Input Low Voltage, VIL, binary input	OE			0.8	V
Input High Voltage, VIH, trinary inputs	S1, S0	VDD-0.5			V
Input Low Voltage, VIL, trinary inputs	S1, S0			0.5	V
Output High Voltage, VOH	IOH=-12mA	2.4			V
Output Low Voltage, VOL	IOL=12mA			0.4	V
Output High Voltage, VOH, CMOS level	IOH=-8mA	VDD-0.4			V
Operating Supply Current, IDD	No Load		9		mA
Short Circuit Current	Each output		±50		mA
Input Capacitance	S1, S0, OE		5		pF
Frequency synthesis error	All clocks			0	ppm
VIN, VCXO control voltage		0		3.3	V
<b>AC CHARACTERISTICS (VDD = 3.3V unless noted)</b>					
Input Crystal Frequency		10		18	MHz
Output Clock Rise Time	0.8 to 2.0V			1.5	ns
Output Clock Fall Time	2.0 to 0.8V			1.5	ns
Output Clock Duty Cycle	At VDD/2	40		60	%
Maximum Absolute Jitter, short term			±150		ps
Phase Noise, relative to carrier, note 3	10 kHz offset		-115		dBc/Hz
Output pullability, note 2	0V VIN 3.3V	±100			ppm

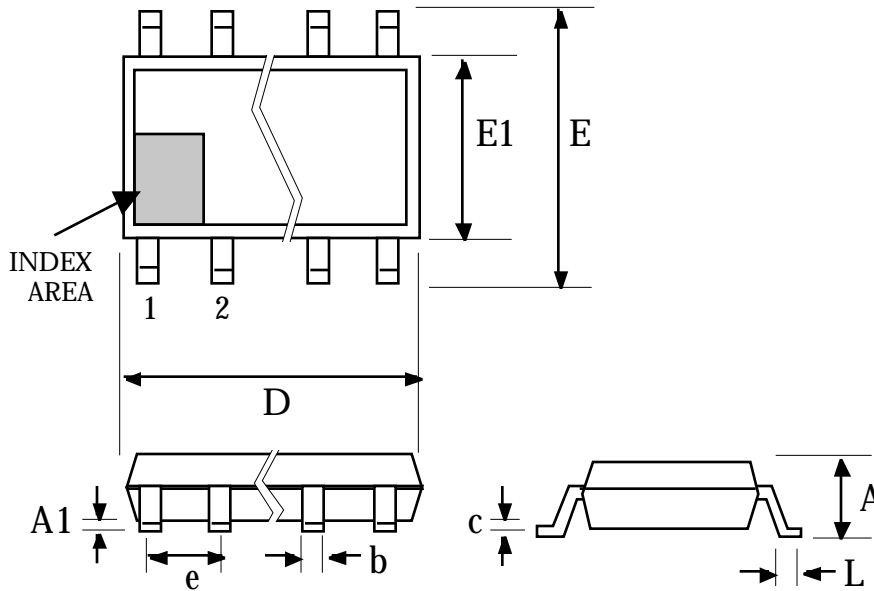
- Notes: 1. Stresses beyond those listed under Absolute Maximum Ratings could cause permanent damage to the device. Prolonged exposure to levels above the operating limits but below the Absolute Maximums may affect device reliability.  
2. With an ICS/MicroClock approved pullable crystal.  
3. To achieve this level of phase noise (lowest), REFCLK must be turned off by connecting  $\overline{\text{REFEN}}$  to VDD.



### Package Outline and Package Dimensions

(For current dimensional specifications, see JEDEC Publication No. 95.)

#### 16 pin TSSOP



Symbol	Millimeters	
	Min	Max
A	-	1.20
A1	0.05	0.15
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BSC	
E1	4.30	4.50
e	0.65 BSC	
L	0.45	0.75

### Ordering Information

Part/Order Number	Shipping packaging	Marking (both)	Package	Temperature
MK3732-15G	tubes	ICS (top line)	16 pin TSSOP	0-70 °C
MK3732-15GTR	tape and reel	3732-15G (2nd line)	16 pin TSSOP	0-70 °C

#### Revision history:

Version	Revision	Comments
-	12139	Original
A	8280	Preliminary

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