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Defense Electronics
Supply Center
Dayton, Ohio

Original date
of drawing:
5 June 1987

AMSC N/A

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SIZE
A

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REV

MILITARY DRAWING

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TITLE: MICROCIRCUITS, DIGITAL HIGH-SPEED CMOS 4-BIT BINARY UP/DOWN COUNTER MONOLITHIC SILICON

DWG NO. 5962-86891

PAGE 1 OF 17

5962-E194-2

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-86891	01	E	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54HC191	4-bit synchronous binary up/down counter with preset

Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, 1/4" x 7/8"), dual-in-line package
2	C-2 (20-terminal, .350" x .350"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
DC input voltage	-0.5 V dc to V_{CC} +0.5 V dc
DC output voltage	-0.5 V dc to V_{CC} +0.5 V dc
Clamp diode current	±20 mA
DC output current (per pin)	±25 mA
DC V_{CC} or GND current (per pin)	±50 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	500 mW 2/
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case E	See MIL-M-38510, appendix C
Case 2	80°C/W 3/
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage	+2.0 V dc to +6.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C
Input rise or fall time:	
V_{CC} = 2.0 V	0 to 1000 ns
V_{CC} = 4.5 V	0 to 500 ns
V_{CC} = 6.0 V	0 to 400 ns

Maximum operating frequency (f_{MAX})

T_C = +25°C:

V_{CC} = 2.0 V	4 MHz
V_{CC} = 4.5 V	20 MHz
V_{CC} = 6.0 V	24 MHz

T_C = -55°C to +125°C:

V_{CC} = 2.0 V	2.8 MHz
V_{CC} = 4.5 V	13 MHz
V_{CC} = 6.0 V	15 MHz

Minimum setup time, data A, B, C, D to load (t_{SU1}):

T_C = +25°C:

V_{CC} = 2.0 V	150 ns
V_{CC} = 4.5 V	30 ns
V_{CC} = 6.0 V	25 ns

T_C = -55°C, +125°C:

V_{CC} = 2.0 V	230 ns
V_{CC} = 4.5 V	46 ns
V_{CC} = 6.0 V	38 ns

Minimum setup time, enable to clock, (t_{SU2}):

T_C = +25°C:

V_{CC} = 2.0 V	205 ns
V_{CC} = 4.5 V	41 ns
V_{CC} = 6.0 V	35 ns

T_C = -55°C, +125°C:

V_{CC} = 2.0 V	306 ns
V_{CC} = 4.5 V	61 ns
V_{CC} = 6.0 V	53 ns

Minimum hold time, data A, B, C, D after load (t_{H1}):

T_C = +25°C:

V_{CC} = 2.0 V	5 ns
V_{CC} = 4.5 V	5 ns
V_{CC} = 6.0 V	5 ns

T_C = -55°C, +125°C:

V_{CC} = 2.0 V	5 ns
V_{CC} = 4.5 V	5 ns
V_{CC} = 6.0 V	5 ns

Minimum hold time, enable after clock (t_{H2}):

T_C = +25°C:

V_{CC} = 2.0 V	5 ns
V_{CC} = 4.5 V	5 ns
V_{CC} = 6.0 V	5 ns

T_C = -55°C, +125°C:

V_{CC} = 2.0 V	5 ns
V_{CC} = 4.5 V	5 ns
V_{CC} = 6.0 V	5 ns

Width of clock, or load input pulse (t_W):

T_C = +25°C:

V_{CC} = 2.0 V	125 ns
V_{CC} = 4.5 V	25 ns
V_{CC} = 6.0 V	21 ns

T_C = -55°C, +125°C:

V_{CC} = 2.0 V	190 ns
V_{CC} = 4.5 V	38 ns
V_{CC} = 6.0 V	32 ns

Minimum recovery time (t_{REC}):

T_C = +25°C:

V_{CC} = 2.0 V	150 ns
V_{CC} = 4.5 V	30 ns
V_{CC} = 6.0 V	25 ns

T_C = -55°C, +125°C:
V_{CC} = 2.0 V - 225 ns
V_{CC} = 4.5 V - 45 ns
V_{CC} = 6.0 V - 38 ns

1/ Unless otherwise specified all voltages are referenced to ground.
2/ For T_C = +100°C to +125°C, derate linearly at 12 mW/°C.
3/ When a thermal resistance for this case is published in MIL-M-38510, appendix C, that value shall supersede the value indicated herein.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ (Unless otherwise specified)		Group A subgroups	Limits Min	Limits Max	Unit
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 20\ \mu A$	$V_{CC} = 2.0$ V	1, 2, 3	1.9		V
			$V_{CC} = 4.5$ V		4.4		
			$V_{CC} = 6.0$ V		5.9		
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 4.0$ mA	$V_{CC} = 4.5$ V		3.7		
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 5.2$ mA	$V_{CC} = 6.0$ V		5.2		
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 20\ \mu A$	$V_{CC} = 2.0$ V	1, 2, 3		0.1	V
			$V_{CC} = 4.5$ V			0.1	
			$V_{CC} = 6.0$ V			0.1	
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 4.0$ mA	$V_{CC} = 4.5$ V			0.4	
		$V_{IN} = V_{IH}$ or V_{IL} $\lvert I_O \rvert \le 5.2$ mA	$V_{CC} = 6.0$ V			0.4	
High level input voltage 2/	V_{IH}		$V_{CC} = 2.0$ V	1, 2, 3	1.5		V
			$V_{CC} = 4.5$ V		3.15		
			$V_{CC} = 6.0$ V		4.2		
Low level input voltage 2/	V_{IL}		$V_{CC} = 2.0$ V	1, 2, 3		0.3	V
			$V_{CC} = 4.5$ V			0.9	
			$V_{CC} = 6.0$ V			1.2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ (Unless otherwise specified)		Group A subgroups	Limits Min	Limits Max	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V T_C = +25°C See 4.3.1c		4		10	pF
Quiescent current	I_{CC}	V_{CC} = 6.0 V, I_O = 0 µA V_{IN} = V_{CC} or GND		1, 2, 3		160	µA
Input leakage current	I_{IN}	V_{CC} = 6.0 V V_{IN} = V_{CC} or GND		1, 2, 3		±1	µA
Functional test		See 4.3.1d		7			
Propagation delay time, load to Q_A, Q_B, Q_C, Q_D 3/ See figure 4	t_{PHL1} t_{PLH1}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		264	ns
			V_{CC} = 4.5 V			53	
			V_{CC} = 6.0 V			45	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		396	ns
			V_{CC} = 4.5 V			79	
			V_{CC} = 6.0 V			67	
Propagation delay time, data A, B, C, D to Q_A, Q_B, Q_C, Q_D 3/ See figure 4	t_{PHL2} t_{PLH2}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		240	ns
			V_{CC} = 4.5 V			48	
			V_{CC} = 6.0 V			41	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		360	ns
			V_{CC} = 4.5 V			72	
			V_{CC} = 6.0 V			61	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ (Unless otherwise specified)		Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay time, clock to ripple clock 3/ See figure 4	t_{PHL3} t_{PLH3}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		150	ns
			V_{CC} = 4.5 V			30	
			V_{CC} = 6.0 V			26	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		225	ns
			V_{CC} = 4.5 V			45	
			V_{CC} = 6.0 V			38	
Propagation delay time, clock to Q_A, Q_B, Q_C, Q_D 3/ See figure 4	t_{PHL4} t_{PLH4}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		220	ns
			V_{CC} = 4.5 V			44	
			V_{CC} = 6.0 V			37	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		330	ns
			V_{CC} = 4.5 V			66	
			V_{CC} = 6.0 V			56	
Propagation delay time, clock to MAX/MIN 3/ See figure 4	t_{PHL5} t_{PLH5}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		255	ns
			V_{CC} = 4.5 V			51	
			V_{CC} = 6.0 V			43	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		385	ns
			V_{CC} = 4.5 V			77	
			V_{CC} = 6.0 V			65	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C < T_C < +125°C$ (Unless otherwise specified)		Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay time, down/up to ripple clock 3/ See figure 4	t_{PHL6} t_{PLH6}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		228	ns
			V_{CC} = 4.5 V			46	
			V_{CC} = 6.0 V			38	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		342	ns
			V_{CC} = 4.5 V			68	
			V_{CC} = 6.0 V			59	
Propagation delay time, down/up to MAX/MIN 3/ See figure 4	t_{PHL7} t_{PLH7}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		200	ns
			V_{CC} = 4.5 V			40	
			V_{CC} = 6.0 V			34	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		300	ns
			V_{CC} = 4.5 V			60	
			V_{CC} = 6.0 V			51	
Propagation delay time, enable to ripple clock 3/ See figure 4	t_{PHL8} t_{PLH8}	T_C = +25°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	9		150	ns
			V_{CC} = 4.5 V			30	
			V_{CC} = 6.0 V			26	
		T_C = -55°C, +125°C C_L = 50 pF ±10%	V_{CC} = 2.0 V	10, 11		225	ns
			V_{CC} = 4.5 V			45	
			V_{CC} = 6.0 V			38	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ (Unless otherwise specified)		Group A subgroups	Limits Min	Limits Max	Unit
Transition time 4/ See figure 4	t_{THL} t_{TLH}	$T_C = +25°C$ $C_L = 50$ pF ±10%	$V_{CC} = 2.0$ V	9		75	ns
			$V_{CC} = 4.5$ V			15	
			$V_{CC} = 6.0$ V			13	
		$T_C = -55°C, +125°C$ $C_L = 50$ pF ±10%	$V_{CC} = 2.0$ V	10, 11		110	ns
			$V_{CC} = 4.5$ V			22	
			$V_{CC} = 6.0$ V			19	

1/ For a power supply of 5 V ±10% the worst case output voltages (V_{OH} and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5$ V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.8 V). The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V should be used. Power dissipation capacitance (C_{PD}), typically 45 pF, determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

2/ Test not required if applied as a forcing function for V_{OH} or V_{OL}.

3/ AC testing at $V_{CC} = 2.0$ V and $V_{CC} = 6.0$ V shall be guaranteed, if not tested, to the specified parameters.

4/ Transition times (t_{THL}, t_{TLH}), if not tested, shall be guaranteed to the specified parameters.

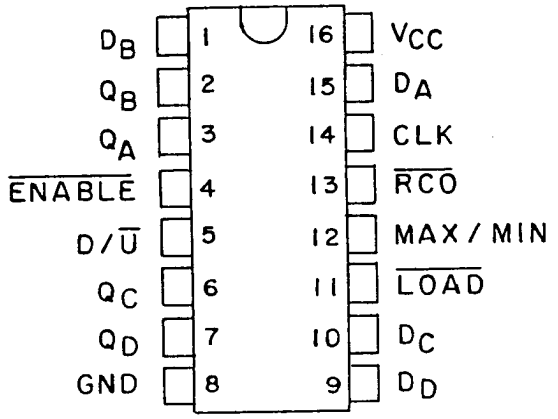
3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

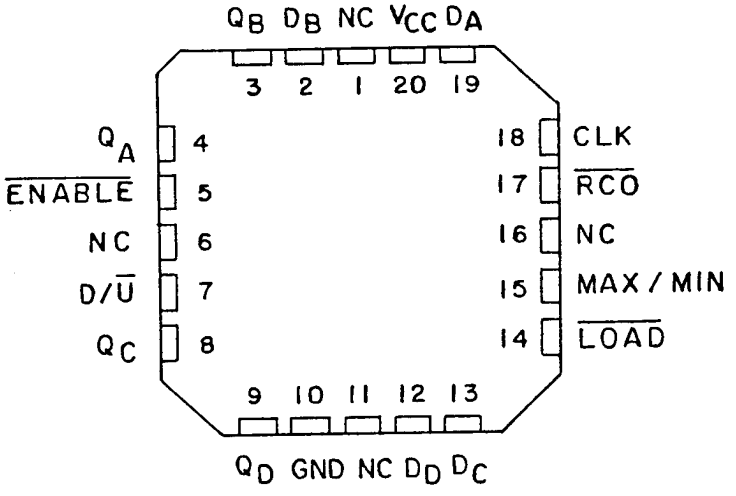
3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

Case E



(TOP VIEW)

Case 2



NC – NO INTERNAL CONNECTION

(TOP VIEW)

FIGURE 1. Terminal connections.

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FEB 86

$\overline{\text{Load}}$	$\overline{\text{Enable}}$	Down/ $\overline{\text{Up}}$	Clock	Function
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Load
H	H	X	X	No Change

Asynchronous inputs Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D

FIGURE 2. Truth table.

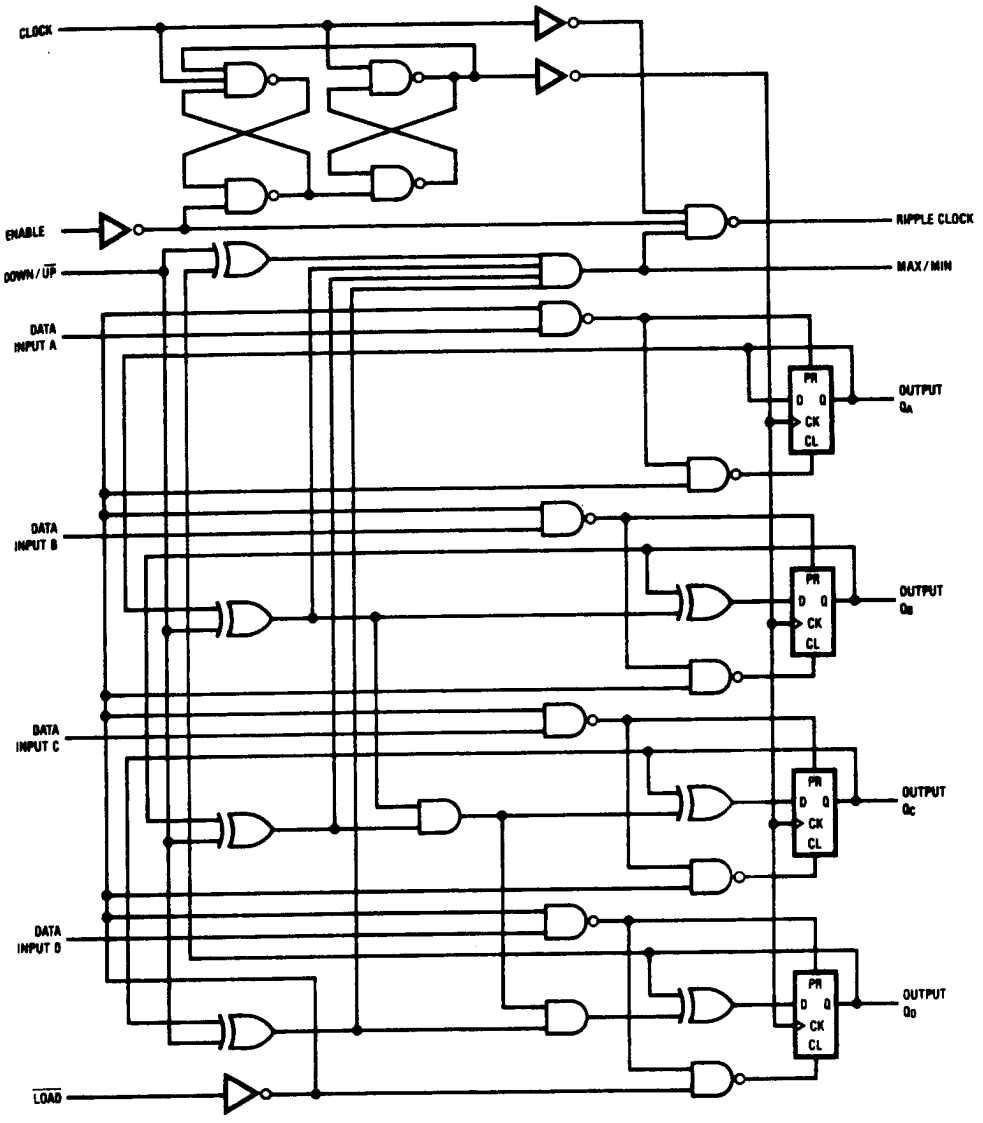
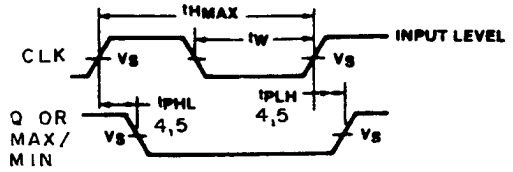
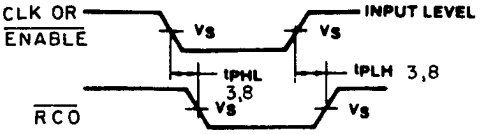


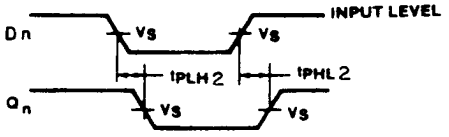
FIGURE 3. Logic diagram.



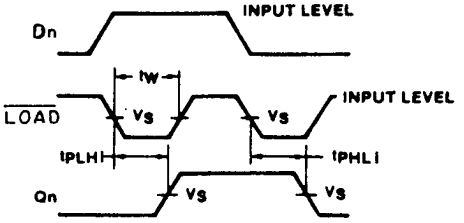
Waveform 1



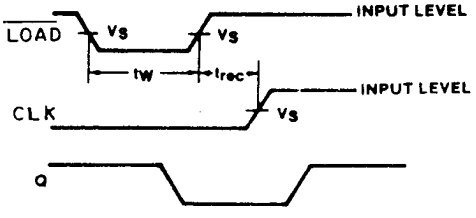
Waveform 2



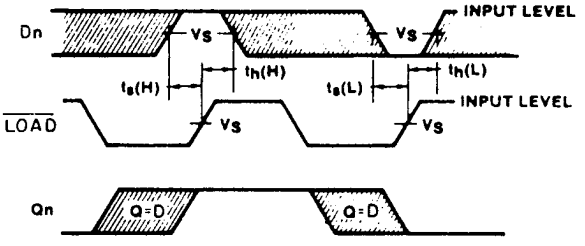
Waveform 3



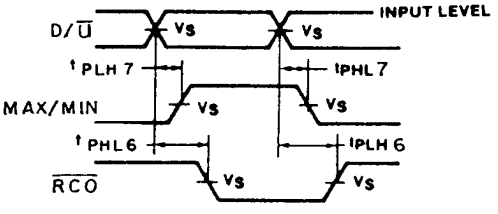
Waveform 4



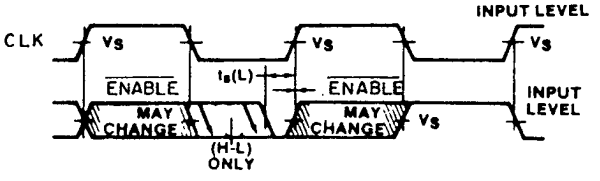
Waveform 5



Waveform 6



Waveform 7

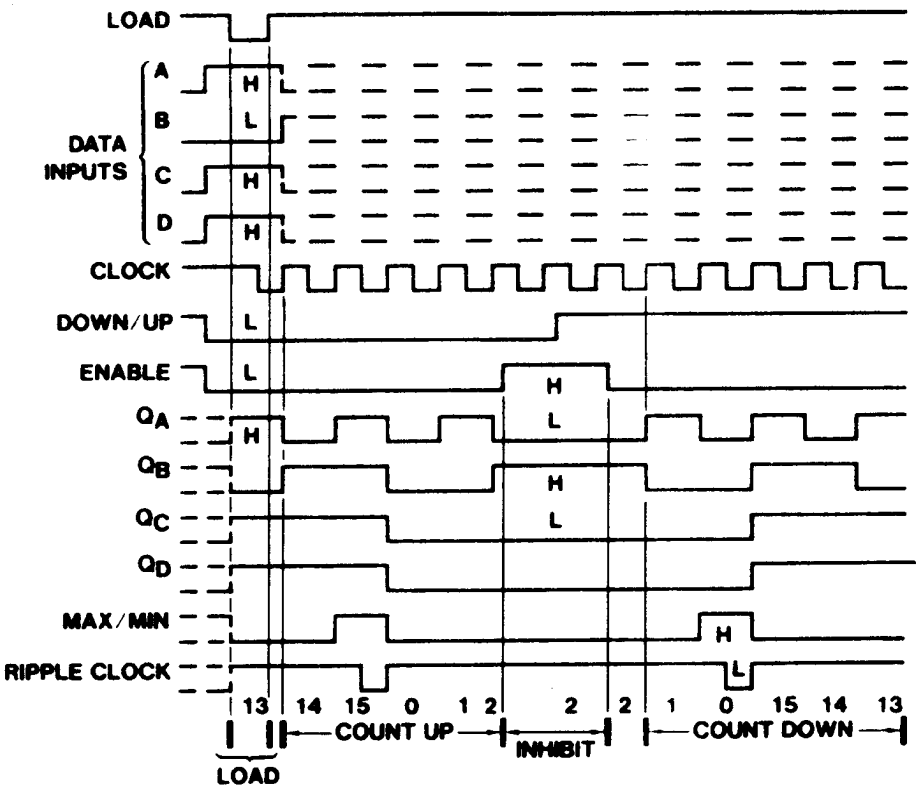


Waveform 8

The shaded areas indicate when the input is permitted to change for predictable output performance.

FIGURE 4. Switching waveforms.

Typical Load, Count, and Inhibit Sequence



Sequence:
(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one, and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen, and thirteen

FIGURE 5. Counting sequence.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test (method 1015 of MIL-STD-883).

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, 6, and 8 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroup 7 tests sufficiently to verify the truth table.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	1
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3
Additional electrical subgroups for group C periodic inspections	

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Replaceability is determined as follows:

a. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

b. When a QPL source is established, the part numbered device specified in this drawing will be replaced by the microcircuit identified as part number M38510/66305.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/	Replacement military specification part number
5962-8689101EX	01295 18714	SNJ54HC191J CD54HC191F/3A	M38510/66305BEX
5962-86891012X	01295	SNJ54HC191FK	M38510/66305B2X

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments, Inc. P. O. Box 6448 Midland, TX. 79701
18714	RCA Solid State Division Route 202 Somerville, NJ. 08876