SP2002

350/400MHz DIRECT FREQUENCY SYNTHESISER

(Supersedes version in May 1991 Professional Products IC Handbook)

The SP2002 is a Direct Frequency Synthesiser (DFS) with square and selectable sine or triangular output waveforms available from on–chip 8–bit D–A converters.

The maximum programmable output frequency and resolution is dependant on the clock frequency. With a clock frequency of 1.074GHz the output frequency can be programmed in 0.5Hz steps from 0.5Hz to 268MHz by means of an externally applied binary word. Inputs are ECL 100k compatible.

The SP2002 is the first in a new range of DFS products.

FEATURES

- 400MHz Output Frequency
- In–Phase (I) and Quadrature (Q) Outputs
- 0.5Hz resolution with 1074MHz Clock
- Sine, Square or Triangle Output

APPLICATIONS

- LO Synthesis in Frequency Agile Radio/Radar
- ECM/ECCm
- Deceptive Countermeasures
- Multi–Function Radio
- Instrumentation

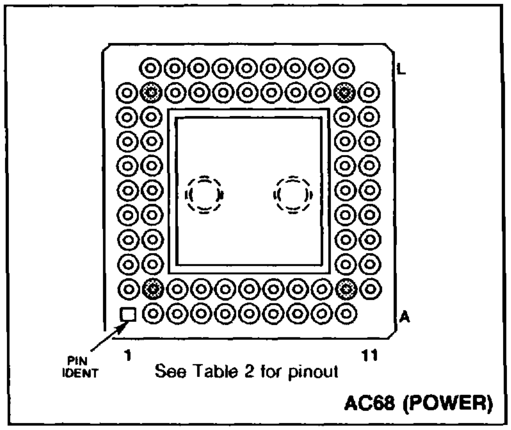


Fig.1 Pin connections - bottom view

ORDERING INFORMATION

SP2002/B/AC Industrial Temperature Range PGA Package
SP2002/A/AC Military Temperature Range PGA Package
SP2002/AA/AC GPS HiRel Level 'A'
SP2002/AB/AC GPS HiRel Level 'B'

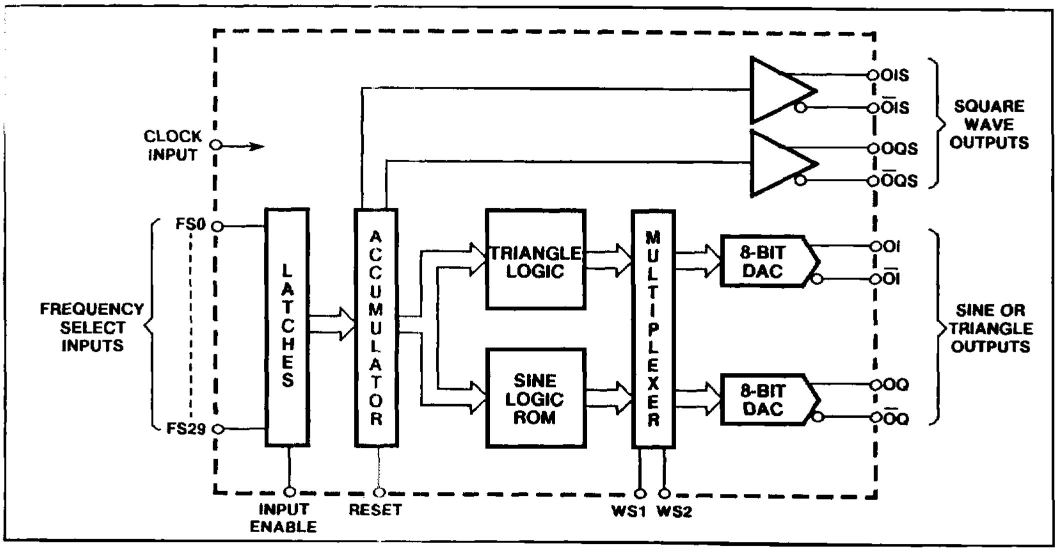


Fig. 2 SP2002 direct frequency synthesiser block diagram

ELECTRICAL CHARACTERISTICS

Guaranteed over the following temperature and supply voltage range.
A grade V_{EE} = - 4.25V to -4.75V, T_{CASE} = -55°C to +125°C Clock input fc = 100MHz to 1.4GHz
B grade V_{EE} = -4.25V to -4.75V, T_{CASE} = -40°C to +85°C, Clock input fc = 100MHz to 1.6GHz

Test conditions (unless otherwise stated)

Supply Voltage: V_{EE} = -4.25V and -4.75V V_{IL} = -1.67V, V_{IH} = -1V
A grade, Temperature T_{CASE} = -55°C and +125°C, fc = 1.4GHz
B grade, Temperature T_{AMB} = 25°C, fc = 1.6GHz

Characteristic	Signal Name	Value			Units	Conditions
		Min	Typ	Max		
Supply current	I_{EE}	0.85	1.1	1.35	A	Note 1
Sine/Triangle Output Current	OQ (bar) OQ OI (bar) OI	14	24	32	mA p-p	See Operating Notes, fOUT = $\frac{fc}{2^9}$
Square Wave Output Current	OQS(bar) OQS OIS(bar) OIS	6	11	16	mA p-p	See Operating Notes fOUT = $\frac{fc}{2^9}$
ECL Input Bias Current, all I/Ps except Clock	FS0-FS29 I/P EN, RESET		150		µA	
Waveform Select Input Current	WS1, WS2		1		mA	V_{IH} = 0V
Waveform Select Input High Voltage	WS1, WS2	-0.5V		0V	V	
Waveform Select Input Low Voltage	WS1, WS2	$-V_{EE}$		$-V_{EE}$ +0.5	V	
Clock Input Current	CLOCK		40		µA	
Output Frequency Range	All Outputs			$\frac{fc}{4}$	Hz	Note 2
Channel Spacing	All Outputs	0.5			Hz	fc = 1.074GHz, Note 2
Close to Carrier Noise			-135		dBc/Hz	10kHz offset, Note 6
Spurious Output levels	Sine Output					In 10kHz Bandwidth
$f_{out} = \frac{fc}{2^9}$			-48	-45	dBc	Note 3 Decimal input code = 8389631
$f_{out} = \frac{fc}{2^4}$			-45	-41	dBc	Note 3 Decimal input code = 167773183
$f_{out} = \frac{fc}{2^3}$			-30	-20		Note 3 Decimal input code = 268436479
1/4 Crossover Spurious	Sine Output		-30	-21	dBc	

ELECTRICAL CHARACTERISTICS (Continued)

Characteristic	Signal Name	Value			Units	Conditions
		Min	Typ	Max		
2nd Harmonic Content $F_{OUT} = \frac{fc}{2^9}$	Sine Output		-55	-40	dBc	
3nd Harmonic Content $F_{OUT} = \frac{fc}{2^9}$	Sine Output		-43	-35	dBc	
5nd Harmonic Content $F_{OUT} = \frac{fc}{2^9}$	Sine Output		-50	-30	dBc	
Frequency Change Range Time		8		40	Clock Cycle	Note 4
Package Thermal Resistance Chip to Case			4		°C/W	Note 5

NOTES
(1) The power taken by the synthesiser depends upon the 'Waveform Select' inputs (see Fig. 2). The I_{EE} current quoted is for the square wave plus sine wave 'I' and 'Q' outputs where all the SP2002 circuitry is powered up. The output waveform options and associated I_{EE} currents are shown in Table 1. (2) The SP2002 will operate at any clock frequency below 1.6 GHz e.g. at f_c=214MHz, output frequency range=0.1Hz to 50MHz in steps of 0.1Hz. (3) Levels refer to the highest rather than total spurious power. A sine wave output and clock frequency of 1.6 GHz is assumed. These figures will degrade by 10 to 20dB for triangle and 20 to 30dB for square wave output. (4) Minimum figure assumes only MSB Frequency Set Input is changed. Maximum figure assumes LSB Frequency Set Input is changed. (5) A suitable heatsink should be attached to the studs on the top of the package. (6) Assuming no spurious output at the offset frequency.

ABSOLUTE MAXIMUM RATINGS

Storage temperature range	-55°C to +150°C
Supply voltage (V_{EE})	-6V
Input voltages	V_{EE} to +0.5V
Junction temperature	+150°C

CIRCUIT DESCRIPTION

The sine, triangle or square wave output frequency is determined by a parallel 30 bit Frequency Set binary input word. With a clock input rate of 1.074GHz, the output frequency can be incremented in 0.5Hz steps from 0.5Hz to 268MHz. In phase ('I') and Quadrature ('Q') outputs are provided for all three waveform options, as are true and complementary phase outputs. Due to the internal organisation of the chip the maximum output frequency is limited to a quarter of the clock frequency.

Referring to the block diagram of Fig. 2, Waveform Select (WS) pins are provided to enable programming of different output waveform combinations by hard-wiring to the supplies as shown (see Table 1). Depending on the output option chosen, unused circuitry on-chip is automatically turned off to conserve power.

A Reset input is provided to initialise the internal circuits and allow the output waveforms to start from a known state as shown in Fig.4. Input Frequency Set data can be latched if required, by holding the Input Enable pin high.

Referring to Fig. 2, the basic operation is as follows. Frequency Set data is entered via the data latches to an accumulator which is incremented by the clock input.

The accumulator MSB output provides the square wave. The 8 MSB outputs are used to generate the sine and triangle functions. The output of the accumulator is effectively a sawtooth which is converted to a triangle by the triangle logic. The sinewave is generated by circuitry including a ROM containing a quadrant of sinewave data which, with the associated logic, produces a complete sinewave in digital form. A multiplexer selects triangle or sine output under the control of the Waveform Select pins. The analog triangle or sine outputs are generated via 8-bit DACs.

OPERATING NOTES

The SP2002 is a very high speed ECL circuit with a maximum clock frequency in excess of 1.6GHz and output frequency capability above 400MHz. In order to achieve correct operation at these frequencies and to ensure output waveform integrity, attention must be paid to the layout of the application board. The use of a ground plane and good RF techniques is recommended. Power supply pins should be well decoupled using high frequency capacitors. All power supply and ground pins must be connected.

The clock input is 100k ECL compatible and if a relatively low frequency clock is required the input may be driven directly from a 100k ECL gate with a 50 Ohm termination resistor to -2V mounted close to the clock pin. At frequencies greater than a few hundred MHz, clock drive from ECL is not practicable and a sinewave drive ac-coupled to the clock input may be used. The application diagram in figure 4 shows a typical arrangement where the 68 Ohm and 160 Ohm resistors set a suitable bias voltage for the clock input and also provide a 50 Ohm termination for the connecting cable or stripline. A suitable drive level is +4dBm or 1V p-p, but at very high clock frequencies this may need to be increased by a few dB to make up for losses.

The frequency set, input enable and reset inputs are 100K ECL compatible, and when very fast frequency hopping is required, for instance when generating chirp waveforms the input data will necessarily come from an ECL source. Many other applications may require much slower data which may be generated from a CMOS source. CMOS data cannot be connected directly to the SP2002 inputs since the high logic is equal to the positive supply which would saturate the input transistors and cause the circuit to malfunction.

A possible interface to CMOS logic is shown in Fig. 3 where the CMOS positive power rail is dropped approximately 0.7V below that feeding the SP2002 by including a diode in series with the CMOS supply.

The low logic level for the SP2002 may be equal to the VEE supply but should not be taken more negative.

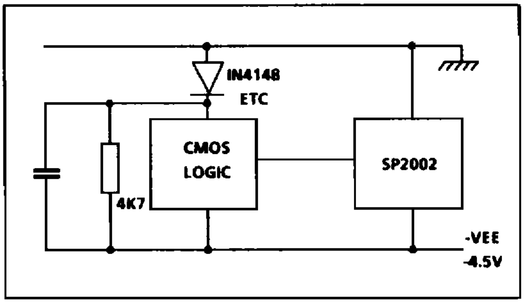


Fig. 3 Interface to CMOS Logic

The output frequency and step size is a function of the clock rate and the frequency select data. The output frequency can be calculated from the formula

$$f_{out} = \frac{Kf_c}{2^N} \text{ where } N=31, \text{ the number}$$

of bits in the accumulator, fc is the clock frequency and K the number on the frequency select inputs.

The minimum output frequency and step size are given by

$$f_{min} = \frac{f_c}{2^N}$$

The reset pin sets the 31 bit accumulator to zero regardless of the state of any other inputs.

The input is active high and when reset, the sine triangle and square wave outputs remain at the level obtained when the accumulator reaches zero in dynamic operation. The effect of the Input enable and Reset inputs is shown diagramatically in figure 4.

All the outputs are current sources, the sine and triangle outputs being obtained from the DAC outputs whilst the square wave outputs are fed from a separate buffer circuit driven direct from the accumulator MSB. Normally the output signal is obtained by loading the output with a 50 Ohm resistor to ground, but in practice the resistor can be any value from zero to 50 Ohms allowing control of the output voltage. If necessary the output load resistor can be returned to an output voltage up to 1V more positive than ground. This feature may be used to produce output signals symmetrical about ground, in the case of the sine triangle outputs, 50 Ohm resistors connected to +0.5V will produce ≈ 1V peak to peak output centred about ground.

A heatsink is required to maintain the chip operating temperature at a safe value. The heatsink should be attached to the studs on the top of the package using M3 nuts. A thermal resistance of 10°C/W is suitable for operation at 25°C.

The frequency select input is positive logic, ie the minimum output frequency is obtained when the LSB is high and all other inputs low.

All frequency select inputs have a nominal 30K input pull down resistor to VEE and will therefore be pulled low if left open circuit.

The waveform select pins WS1 and WS2 are intended to be hard wired to VEE or ground depending on the output waveform requirements. When necessary, the inputs could be switched using external transistors provided the minimum level requirements specified in the table of characteristics are met. The waveform select inputs should not be left open circuit.

The input Enable pin controls entry of input data to the input latches. When the input is low the input latches are transparent and any data change results in a change to the output frequency. When the input is taken high the data present on the frequency select inputs before the low to high transition is retained on the input latches and sets the output frequency.

The frequency select input can be changed without changing the output frequency until the frequency select input is again taken low, and the new data enters the latches. The Input Enable pin has an internal nominally 30K pull down resistor to VEE and will therefore go low if left open circuit.

Waveform Select input		Output waveform selected	I_{EE} (A) TYP	Power (W)
WS1	WS2			
V_{EE}	V_{EE}	Square wave 'I' and 'Q' Triangle 'I' and 'Q'	1.0	4.5
GND	V_{EE}	Square wave 'I' and 'Q' Sine wave 'I'	1.0	4.5
V_{EE}	GND	Square wave 'I and Q'	0.6	2.7
GND	GND	Square wave 'I' and 'Q' Sine wave 'I' and 'Q'	1.1	5.0

Table 1 Output waveform options

Pin No.	Pin name	Pin No.	Pin name
B1	WS2	K11	FS23
B2	WS1	K10	FS24
C1	TDI	J11	FS25
C2	TRC	J10	FS26
D1	RESET	H11	FS27
D2	GND	H10	FS28
E1	GND	G11	FS29
E2	V_{EE}	G10	I PEN
F1	GND	F11	CLOCK
F2	FS0	F10	V_{EE}
G1	FS1	E11	GND
G2	FS2	E10	GND
H1	FS3	D11	GND
H2	FS4	D10	TOQ
J1	FS5	C11	TOI
J2	FS6	C10	$\overline{OQS}$
K1	FS7	B11	OQS
L2	FS8	A10	$\overline{OIS}$
K2	FS9	B10	OIS
L3	FS10	A9	IC
K3	FS11	B9	NC
L4	FS12	A8	$\overline{OQ}$
K4	FS13	B8	OQ
L5	FS14	A7	NC
K5	GND	B7	V_{EE}
L6	V_{EE}	A6	GND
K6	FS15	B6	IC
L7	FS16	A5	NC
K7	FS17	B5	$\overline{OI}$
L8	FS18	A4	OI
K8	FS19	B4	NC
L9	FS20	A3	V_{EE}
K9	FS21	B3	GND
L10	FS22	A2	NC

Table 2 SP2002 pin assignment. IC pins are not required for normal use but should be left open.

Pin name	Function
WS1, WS2	Waveform select, see Table 1.
TDI, TRC, TOQ,TOI	Test pins only. Not required for normal operation. Leave open circuit.
RESET	A logic '1' on this pin resets the accumulator
FS0-FS29	Frequency Select inputs. FS0 is the LSB.
I PEN	Frequency Select Input Enable. A logic '1' on this pin latches data into the accumulator.
CLOCK	Clock input.
OQS, OIS	Square wave outputs.
OQ, OI	Sine or triangle outputs.
GND	0V
V_{EE}	Negative power supply (-4.5V).
NC	Not connected.

Table 3 SP2002 pin descriptions

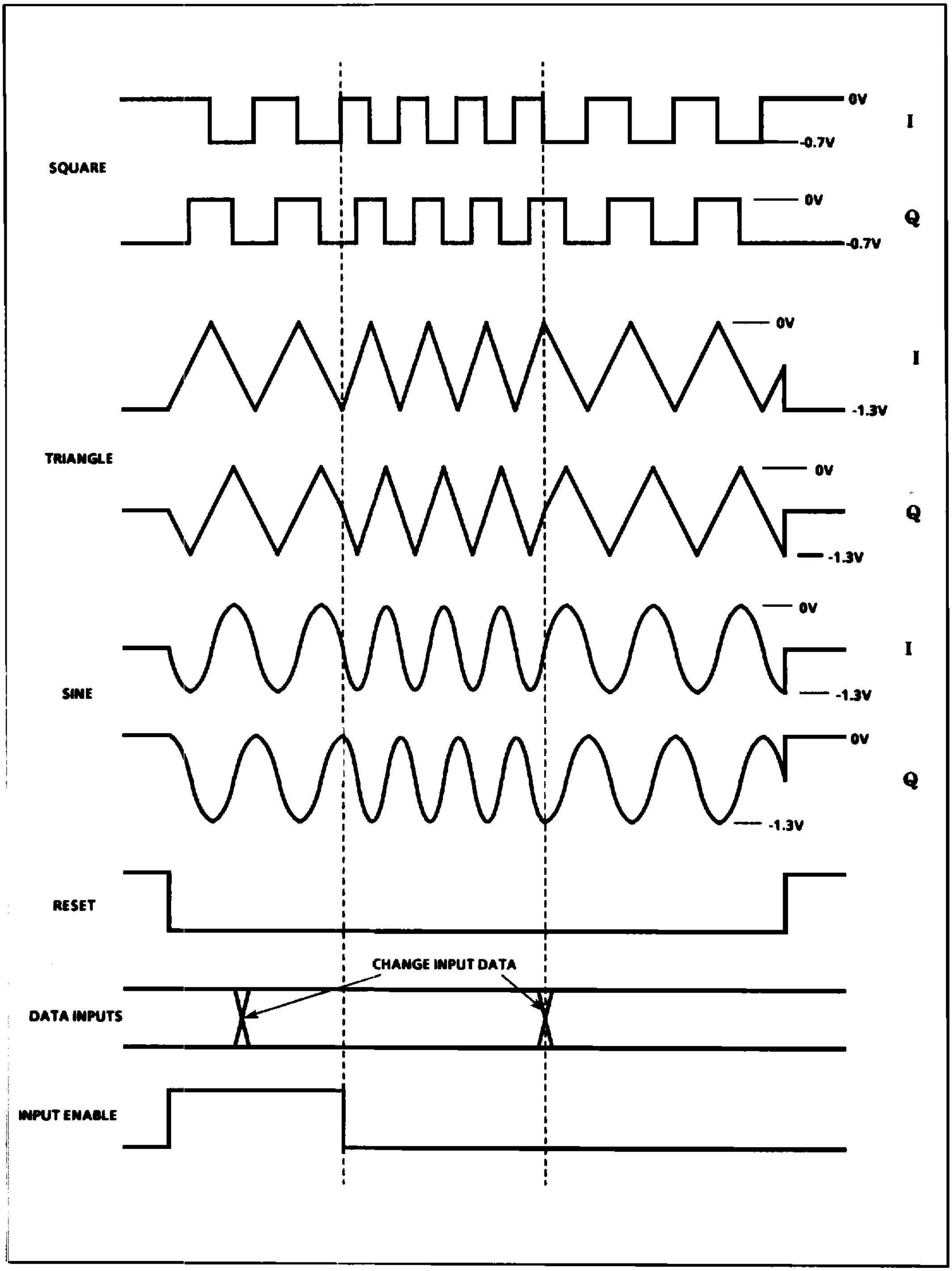
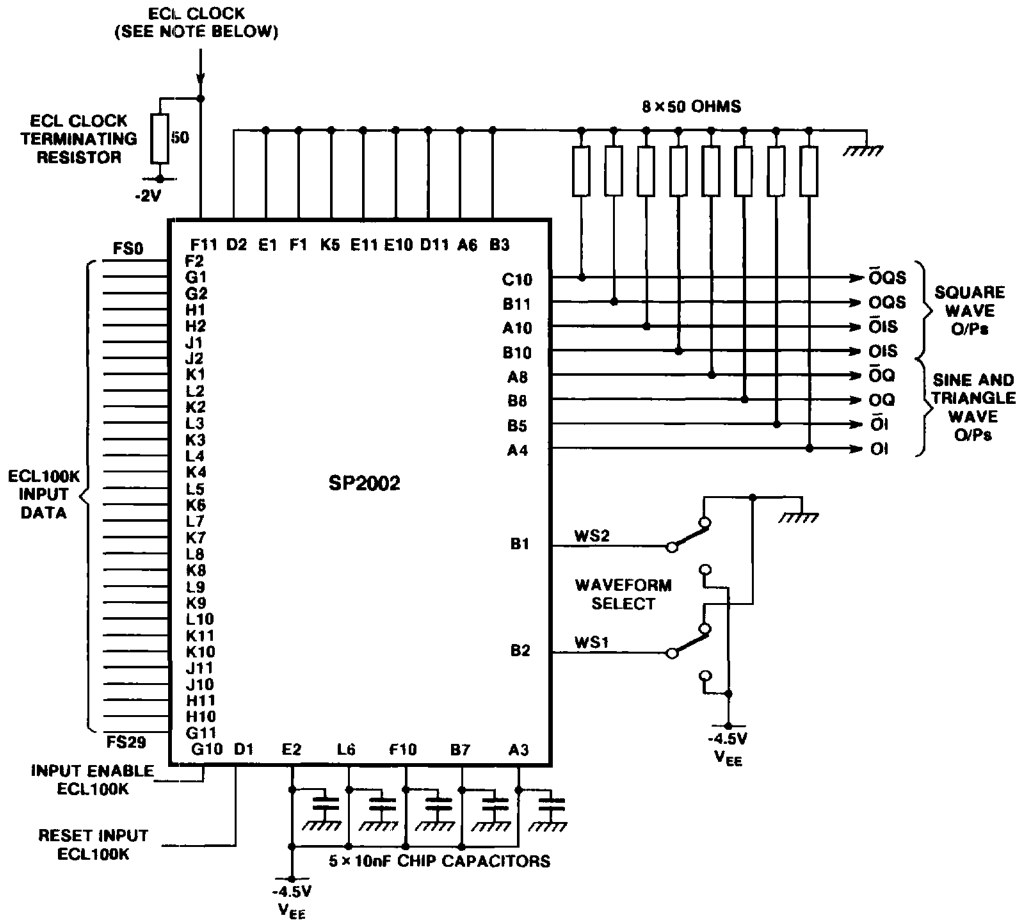
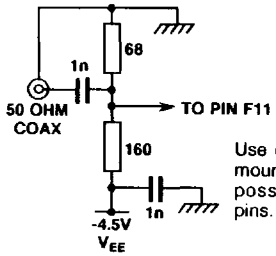


Fig. 4 SP2002 timing and waveform diagram.





Use chip components mounted as close as possible to the IC pins.

Typical sinewave clock bias and termination circuit

NOTE

The clock input may be ECL level DC-coupled as shown above or a sinewave input of 1V peak-to-peak amplitude AC-coupled. When sinewave drive is used the input should be biased to -1.3V and the input cable terminated close to the IC with 50 ohms.

Minimum operating frequency with sinewave drive is 50MHz.

Fig. 5 SP2002 typical application circuit